DOI: 10.71762/sdew-6f75

Research Paper

Fabrication Feasibility of SU8 Waveguides and Gold Electrodes via Lift-Off-Based Micromachining Process

Parisa Mahmoudi[1,2*]
[1]Assistant Professor, Department of Electrical Engineering, Payame Noor University, Tehran, Iran
[2]Microsystem Fabrication Laboratory, Department of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran
[*]Email of Corresponding Author: parisamahmoudi@pnu.ac.ir
Received: June 25, 2025; Revised: August 13, 2025 Accepted: August 14, 2025

Abstract
Brain interfaces are advanced systems designed to combine optical waveguides for neural stimulation with electrodes for recording neural activity. The microfabrication process for developing such compact devices is challenging and critical to their performance and application. However, conventional fabrication techniques often involve stacking layers of different substrates for each of the stimulation and recording components, resulting in bulky designs that increase the risk of invasiveness. This issue makes the implants less practical for neuroscience studies. This research assesses a simple method for assembling SU8 waveguides with Au electrodes on a single substrate. It utilizes the lift-off technique to fabricate electrodes directly onto the waveguide, routing down to the same primary substrate. The introduced method eliminates the need for depositing additional layers as a base for electrode formation. The results demonstrated the successful feasibility and assembly of the structure without relying on a common stacked and thick configuration.

Keywords
Microfabrication, Lift-off, Photolithography, UV Exposure, Deposition, SU8

1. Introduction

Traditional fabrication approaches for neural interfaces often rely on rigid, stacked architectures that pose significant limitations in terms of mechanical flexibility, scalability, and compatibility with dynamic neural environments [1-5]. These multilayered designs not only increase the structural bulk of the final device but also require multiple photolithographic and deposition steps, thereby adding complexity and elevating fabrication costs. Such limitations hinder the development of minimally invasive and adaptable platforms essential for emerging neuroengineering applications, particularly brain-computer interfaces (BCIs) [6-8].

In recent years, there has been growing interest in simplified and versatile microfabrication techniques that can yield integrated neural devices without compromising on precision, performance, or biocompatibility. SU8, a negative photoresist known for its high aspect ratio capabilities and optical transparency, has emerged as a promising candidate for waveguide fabrication, while gold remains a widely used material for electrode formation due to its excellent conductivity and chemical stability [9-12].

In this study, we propose a streamlined fabrication method that integrates SU8-based waveguides with gold electrodes using a lift-off process. This approach minimizes the need for complex layer stacking and reduces overall processing steps, resulting in thinner and more flexible structures that can better conform to neural tissues. Moreover, the lift-off technique allows for high-resolution patterning, facilitating precise electrode alignment and reliable interfacing performance. The results validate the feasibility of this micromachining process as a simplified and effective solution for developing compact, functional BCIs, potentially accelerating innovation in neural interface technologies and their translation to clinical and research settings.

2. Fabrication Process

Figure 1 shows a simple and conceptual schematic of the design. The complete fabrication process is illustrated in Figure 2, as well. In this process, a standard laboratory glass slide is used as a holder (Figure 2a), onto which the Kapton layer is adhered (Figure 2b). Kapton serves as the primary substrate because it is flexible, thin, and biocompatible. This material is a polyimide film available in the market in various thicknesses. Additionally, Kapton is an excellent electrical and thermal insulator.

First, an alignment line is created on the Kapton layer using a cutter to mark the edges and walls for proper mask alignment.

Then, SiO_2 coating is deposited onto the Kapton as the first cladding layer through sputter coating (Figure 2c). The total deposition time is 2 hours. Pre-vacuum pressure, deposition pressure, and power used are 1.1e-4 mbar, 2.2e-2 mbar, and 150 watts, respectively. The resulting thickness is approximately 6nm.

The next step involves SU8 deposition using the spin coating method at a speed of 4000 rpm (Figure 2d), followed by lithography to pattern it as the core material for the waveguide. The negative photoresist SU8 used in this process is SU8:2050. The deposition begins with spin coating for 41 seconds, resulting in a layer thickness of about 40μm. The sample is then subjected to a soft bake step on a hot plate at 95℃ for 3 minutes, followed by a cooling phase. After cooling, the sample is exposed to UV light for 9 seconds at a full intensity of 18 MW/cm^2. This is succeeded by a post-bake step at 95℃ for 5 minutes, followed by another cooling phase. Finally, the SU8 layer is developed using SU8 developer to complete the process (Figure 2e). Since SU8 is the negative photoresist, the regions exposed to light remain intact while the unexposed regions are removed.

Then, an additional SiO_2layer is deposited onto the SU8 waveguide as the second cladding layer, as before (Figure 2f). In the next step, the S1813 positive photoresist layer is deposited via spin coating for 35 seconds at either 3000 rpm or 4000 rpm, ensuring uniform layer formation. The coated layer is baked on a hot plate at 95°C for 2 minutes, followed by a cooling phase (Figure 2g). The layer is then exposed to UV light for 12 seconds at a full intensity of 18 MW/cm^2 Subsequent to the exposure, the development process is carried out using a KOH solution composed of 20cc of water and one tablet. The regions exposed to light are removed, creating openings for the gold electrodes (Figure 2h).

The next step involves depositing titanium and gold layers to form the electrodes (Figure 2i). Since gold does not naturally adhere to any substrate, a titanium underlayer is first deposited to enhance adhesion for the gold layer. Once the deposition process is completed, the entire assembly is immersed in acetone to remove S1813 photoresist. This step not only eliminates the photoresist layer but also lifts off the gold layer where it was deposited over the photoresist (gold development with acetone). Following this, the titanium layer is removed using its specific etchant, leaving behind the final electrode designs (Figure 2j).

However, it is of utmost importance to adequately expose the photoresist on the walls to UV light during the earlier development stage involving the KOH solution, which is performed to create electrode positions. If this is not done, the desired photoresist substance at the edges might be removed. Consequently, the gold in these areas may also be unintentionally removed, causing disconnections in the electrodes.

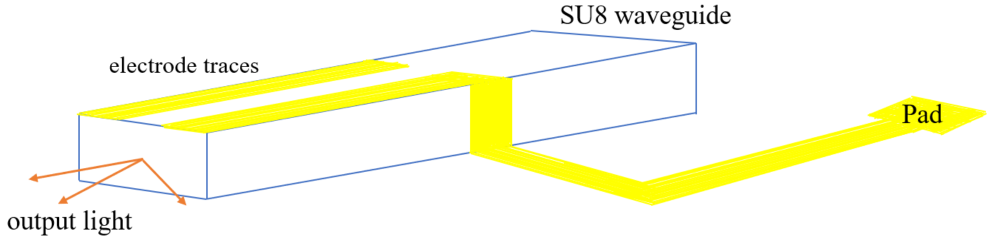


Figure 1. Conceptual illustration of the proposed design

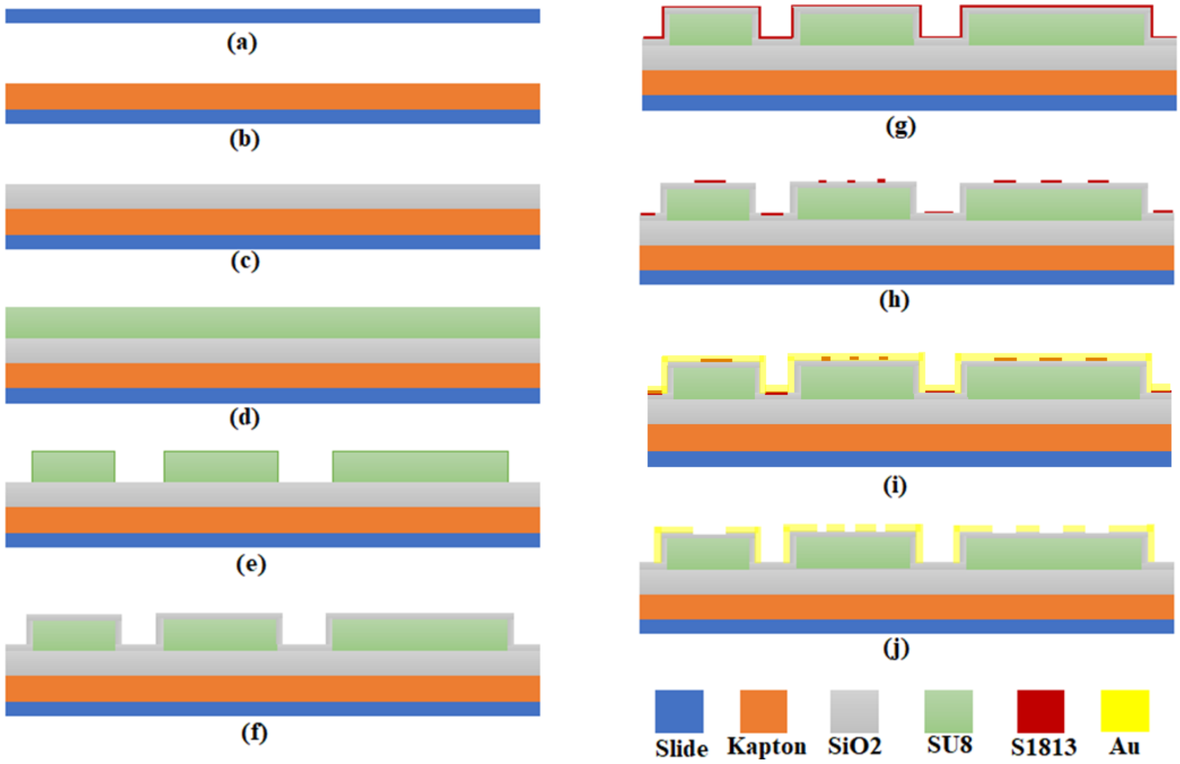
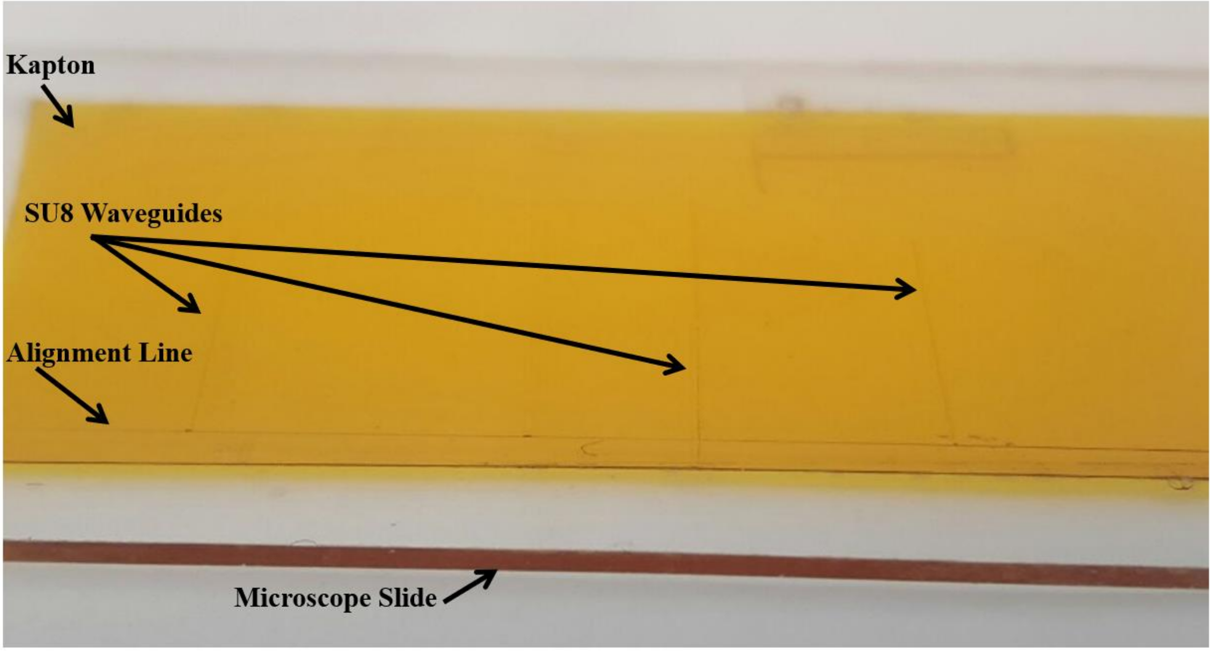


Figure 2. Illustration of the lift-off fabrication process for the device: a) Microscope slide, b) Kapton layer onto the slide, c) SiO_2 deposition, d) SU8 deposition, e) SU8 patterning, f) Second SiO_2 deposition, g) S1813 deposition, h) S1813 patterning, i) Gold deposition, j) Patterning of the electrodes

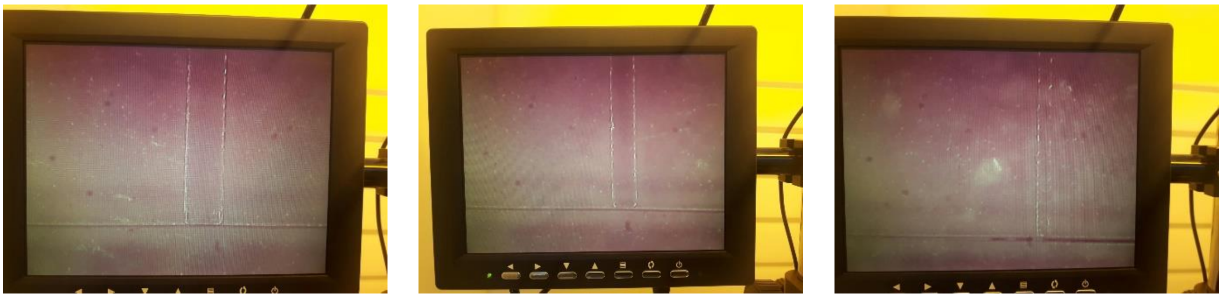
3. Results and Discussion

Figure 3 indicates the fabricated SU8 waveguides in different widths of 250µm, 190µm, and 110µm on a Kapton substrate, and their microscopic images. Also, the alignment line used for the accurate matching of the parts from different steps during the fabrication process is shown.

Figure 4 illustrates the formation of the SiO_2 layer on the waveguides in the sputter coating chamber. Deposition and patterning of S1813 are shown in Figure 5. Also, Figure 6 shows Au deposition and lift-off completion for electrode formation. Figure 7 includes microscopic images of different parts of the final fabricated devices. In order to evaluate the feasibility of the process, three different designs- 110-10/50, 190-10/40, 250-30/40- have been developed for the electrodes with various widths and distances. The first number refers to the waveguide width, the second to the constant spacing between the adjacent electrodes, and the third to the width of each Au trace.



(a)



(b) (c) (d)

Figure 3. a) Illustration of Kapton, microscopic slide, alignment line, and fabricated SU8 waveguides on Kapton, and their microscopic images with different widths of b) 250µm, c) 190µm, d) 110µm

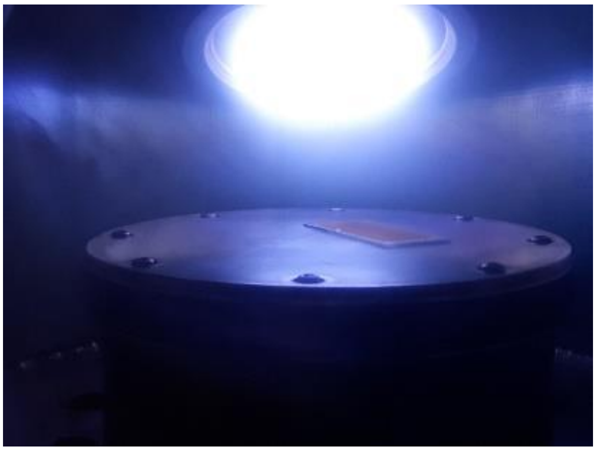
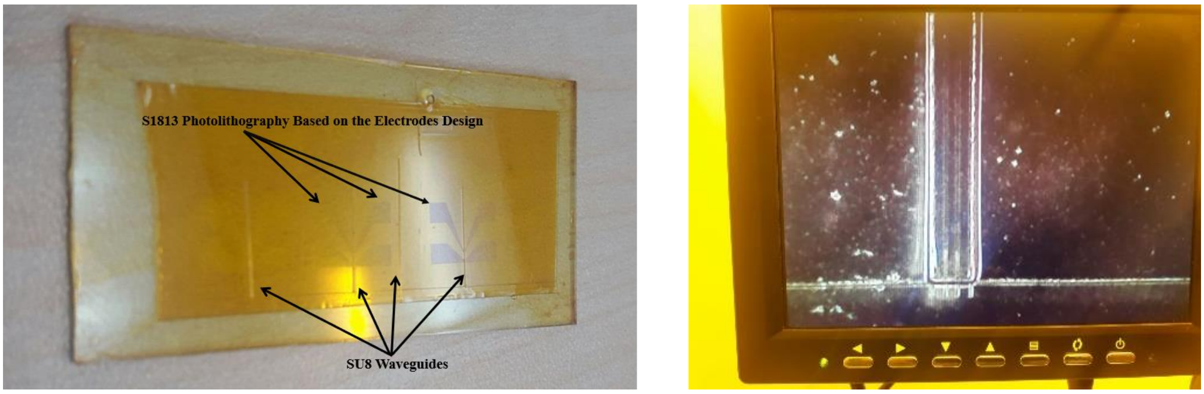
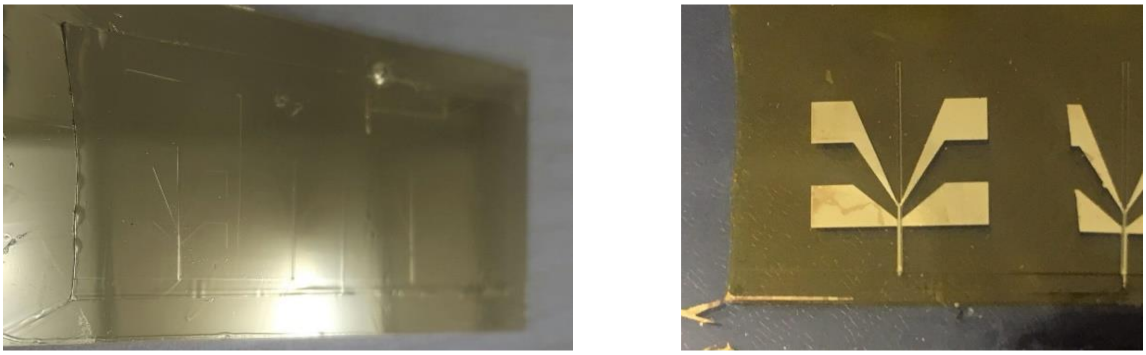


Figure 4. SiO_2 deposition on the fabricated waveguides from the targets into the sputter coating chamber



(a) (b)

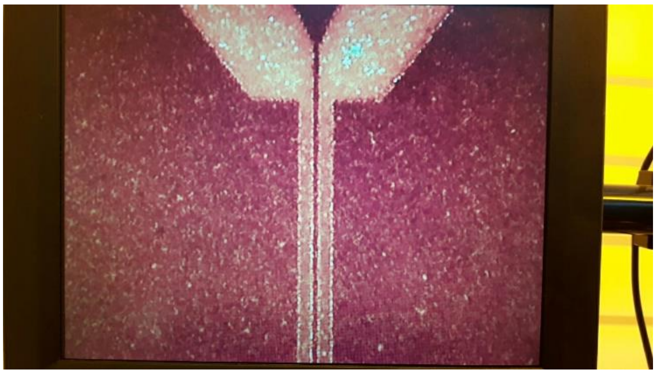
Figure 5. a) S1813 deposition on the waveguides (blue areas) and its photolithography to form electrodes' openings, b) A microscopic image of the waveguide with patterned S1813



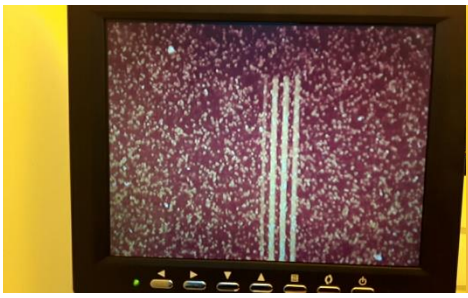
(a) (b)

Figure 6. a) Ti-Au deposition on the whole structure, b) Formation of the electrodes using the lift-off technique and immersing the sample in Acetone for Au development

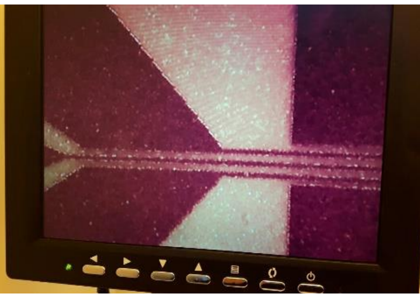
(a)



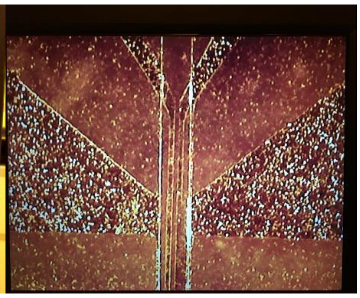
(b)



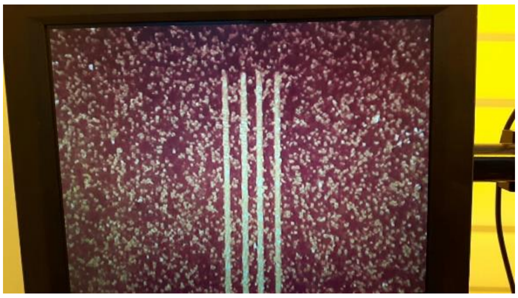
(c)



(d)



(e)



(f)

(g)

Figure 7. a) The optical performance of the SU8 waveguide, and microscopic images of the Au electrodes along the waveguides for b) 110-10/50, c-e) 250-30/40, and f-g) 190-10/40. (The first number is for the waveguide width, the second for the constant distance between the adjacent electrodes, and the third for the width of each Au trace)

4. Direct Photolithography

Direct lithography was also explored as a fabrication route for gold electrode patterning in this study. The full sequence of its fabrication steps is depicted in Figure 8. Unlike the lift-off approach illustrated in Figure 2, the direct method involves depositing the Au layer before applying the sacrificial photoresist (S1813), as shown in Figure 8g. Subsequently, S1813 is spin-coated and photopatterned directly onto the Au surface (Figures 8h and 8i), followed by etching to define the electrode structures (Figure 8j). However, this direct exposure of Au to its etchant during pattern transfer introduced a higher probability of trace discontinuities and electrical cutoffs, particularly along the sidewalls. These regions are highly sensitive to UV dosage, which is critical for ensuring proper connection between upper and lower electrode lines. Incomplete exposure or development at these interfaces often led to misalignments and physical disintegration in the resulting electrode patterns. Furthermore, the direct lithography route involved additional processing steps, increasing overall fabrication time and complexity. Devices fabricated using this method are illustrated in Figure 9, highlighting both the feasibility and limitations of the direct approach compared to the more streamlined and structurally reliable lift-off process adopted in this work.

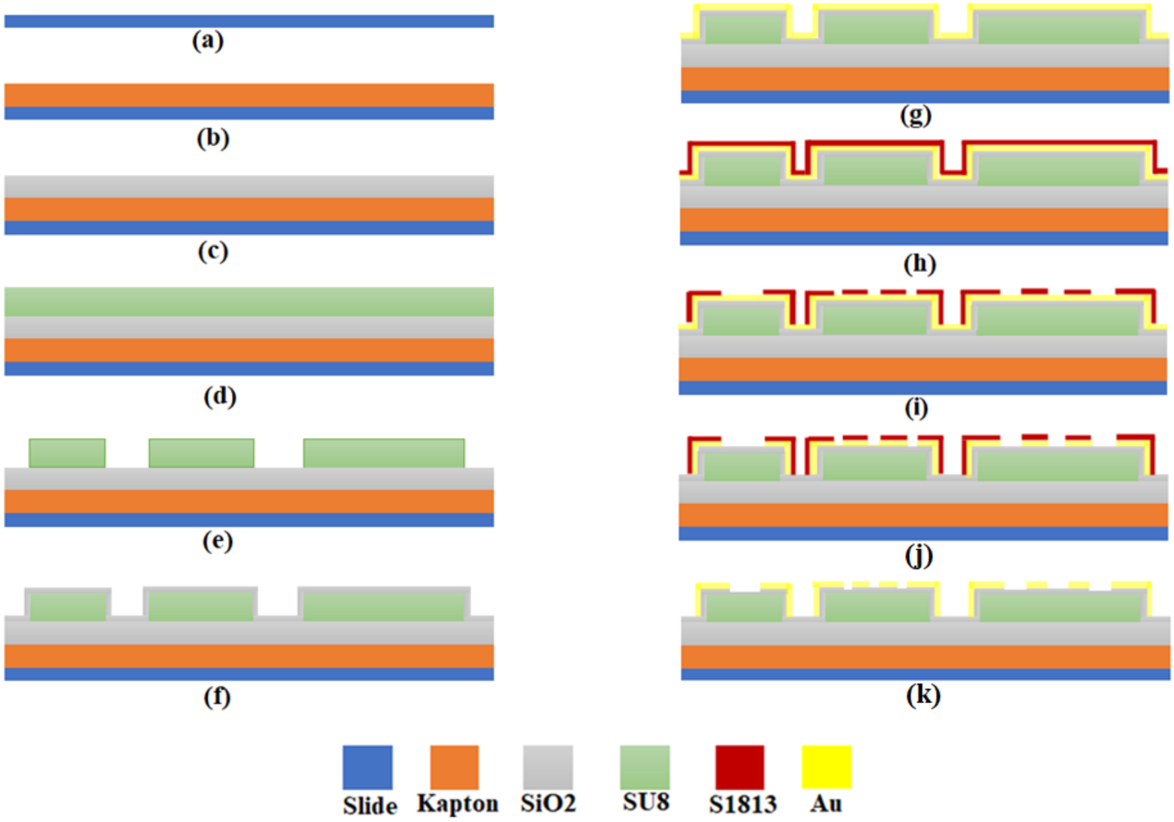


Figure 8. Illustration of the direct photolithography-oriented fabrication process for the device: a) Microscope slide, b) Kapton layer onto the slide, c) SiO_2 deposition, d) SU8 deposition, e) SU8 patterning, f) Second SiO_2 deposition, g) Gold deposition, h) S1813 deposition, i) S1813 patterning, j) Au etching from unwanted areas, k) Removal of S1813 cover and release of the electrodes

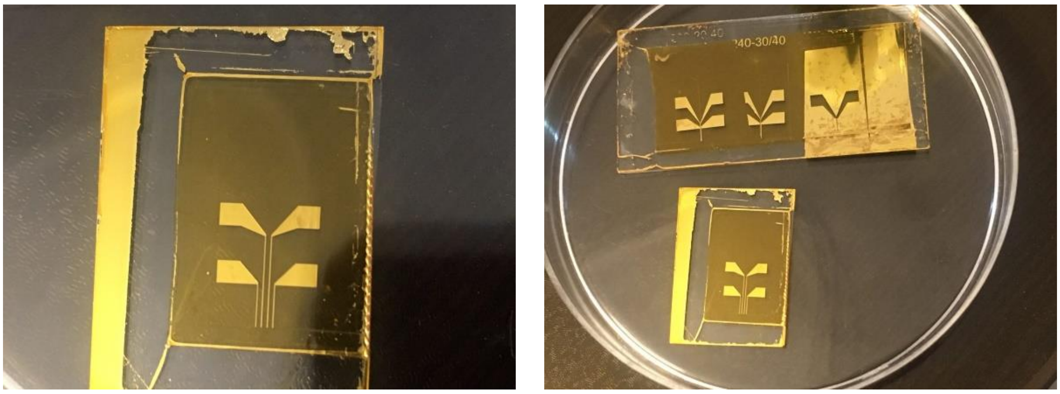


Figure 9. a) The fabricated device from the direct photolithography fabrication process, b) All the devices resulted from both fabrication methods

5. Conclusion

This study presented a streamlined and cost-effective micromachining process for fabricating SU8-based waveguides integrated with gold electrodes, specifically tailored for neural interface applications. By adopting a lift-off approach, gold was deposited directly onto the waveguide substrate, effectively eliminating the need for intermediate base layers and thereby reducing both structural bulkiness and process complexity. This direct deposition strategy not only simplifies fabrication but also enhances alignment precision and trace integrity, addressing challenges commonly associated with conventional multi-step lithographic methods. Furthermore, comparative analysis with direct lithography revealed increased susceptibility to trace discontinuities and longer processing times in the conventional method due to direct exposure of gold to chemical etchants and critical UV patterning conditions. In contrast, the lift-off technique demonstrated superior reliability, reproducibility, and integration capability. The proposed fabrication route offers a promising platform for the development of next-generation brain-computer interface (BCI) devices and related neuroengineering systems, where miniaturization, flexibility, and precise microstructuring are essential. The insights gained from this work not only validate the feasibility of the technique but also contribute to the advancement of scalable, high-performance neural interfaces.

5. References

[1] Cabello, M., Domínguez, I., Macías, C., Perdigones, F., Aracil, C. and Quero, J. M. 2021. Low-cost SU-8 lift-off process to fabricate a Gold/Glass microelectrode array for culturing applications. Microsystem Technologies. 27(7): 3077–3081. doi: 10.1007/s00542-020-05206-9.

[2] Samanta, S., Banerji, P. and Ganguly, P. 2020. Experimental Studies on SU-8 Wire Waveguides. In: Photonic Waveguide Components on Silicon Substrate. SpringerBriefs in Applied Sciences and Technology. Springer, Singapore. doi: 10.1007/978-981-15-1311-4_3.

[3] Chen, Z., Li, X., Tang, Y., Huang, Z., Huang, J., Liu, H. and et al. 2024. Implantation-assistance-free flexible waveguide probe for optogenetic stimulation. Cell Reports Physical Science. 5(10). doi: 10.1016/j.xcrp.2024.102217.

[4] Chen, H.and Fang, Y. 2023. Recent developments in implantable neural probe technologies. MRS Bulletin. 48: 484–494. doi: 10.1557/s43577-023-00535-2.

[5] Luo, J., Xue, N. and Chen, J. 2022. A Review: research progress of neural probes for brain research and brain–computer interface. Biosensors. 12(12): 1167. doi: 10.3390/bios12121167.

[6] Shao, Q., Ma, X., Li, M. and He, J.-J. 2025. Thermo-tuning Fourier transform spectrometer based on SU-8 waveguide. Polymers. 17(3): 261. doi: 10.3390/polym17030261.

[7] Chen, Z. and Lee, J.-B. 2021. Biocompatibility of SU-8 and its biomedical device applications. Micromachines. 12(7): 794. doi: 10.3390/mi12070794.

[8] Lotfi Marchoubeh, M., Cobb, S.J., Abrego Tello, M. and et al. 2021. Miniaturized probe on polymer SU-8 with array of individually addressable microelectrodes for electrochemical analysis in neural and other biological tissues. Anal Bioanal Chem. 413: 6777–6791. doi: 10.1007/s00216-021-03327-2.

[9] Remy, A., Lin, X. and Liu, J. 2024. Materials for flexible and soft brain-computer interfaces, a review. MRS Communications. 14: 827–834. doi: 10.1557/s43579-024-00617-5.

[10] Mahmoudi, P., Veladi, H. and Pakdel, F.G. 2017. Optogenetics, tools and applications in neurobiology. J Med Signals Sens. 7(2):71-79.

[11] Mahmoudi, P., Veladi, H., Ghaderi Pakdel, F. and Frounchi, J. 2023. Low-cost optical splitter for neural stimulations using off-the-shelf ultraviolet adhesives (Erratum). Journal of Micro/Nanopatterning, Materials, and Metrology. 22(2): 029801. doi: 10.1117/1.JMM.22.2.029801.

[12] Mahmoudi, P. 2025. A review of patterned light delivery techniques in optogenetics: Scanning systems, modulators, and implants. Optoelectronic. 7(3): 57–87. doi: 10.30473/jphys.2025.73171.1225.