An Ultra-Low-Power and Full-Swing Full Adder Cell

Soorena Zohoori[1], Mehdi Dolatshahi[1]
1- Department of Electrical Engineering, Najafabad Branch, Islamic Azad University, Najafabad, Iran.
Email: Dolatshahi@iaun.ac.ir (Corresponding Author)

Received: June 2018 Revised: July 2018 Accepted: August 2018

ABSTRACT:
In this paper, a one-bit ultra-low-power full adder cell using GDI structure is proposed. Main objective of this design is not only providing low power consumption, but also providing full swing outputs. In this paper, combination of different logics and stacking technique are used to provide an ultra-low power cell. Also, by using stacked inverters after each function, full swing characteristic for the cell is obtained. These characteristics are obtained in cost of more occupied chip area and higher delay. In order to verify the performance of the proposed cell, simulations are done in HSPICE using 90nm CMOS technology library. Beside Noise immunity, power consumption is also analyzed under different load conditions, different supply voltages and different temperatures. Although delay of the circuit is increased, results show a tremendous reduction in power consumption and an improved power-delay-product for the proposed full adder cell.

KEYWORDS: Ultra-Low-Power, Full Swing, GDI, Full Adder.

1. INTRODUCTION

Full adders are the basic cells of most applications in VLSI. Basic operations such as address calculation, subtraction, division and multiplication are based on performance of the full-adder cells. That is the reason why many researchers have focused on enhancing the performance of a single bit full adder cell in respect to reduction in power consumption or improvement in the speed.

In order to improve an adder's performance, two main ways 'Circuit Design view-point' and 'System level view-point' are of interest. Transistor level design skills are considered in 'circuit design view point' to achieve a high performance core for a full-adder. In 'system level view point' the total critical path delay is reduced by finding the longest critical path in ripple carry adders. Mostly, the carry out signal of the most significant bit (MSB) is the longest signal path [1].

In order to achieve desirable characteristics such as high speed in critical path, low power consumption and reliability at low supply voltages in Nano-meter CMOS technologies, circuit designs need to be optimized. Good driving capability of a full adder cell under different load conditions is also counts as another desirable characteristic for a full adder cell.

Whenever we are to scale down the size of CMOS transistors in VLSI applications, some considerations should be taken into account. First of all, the supply voltage and the threshold voltage should be scaled down in order to avoid hot carrier effect and avoid degradation in speed of the circuits, respectively. However, scaling down the threshold voltage results in an increase in the standby current; and that yields a higher range of power consumption in the circuit [2].

There are different implementations for low power adders. Some of them use different logic styles and some of them use only one logic style. Complementary CMOS (C-CMOS) full adder structures are those which have one logic style [3-4]. These structures are based on pull-up and pull-down networks. These adders provide full swing voltage and have a robust structure against transistor sizing and voltage scaling. The input capacitance in these structures exhibits a large value, due to need of using sized-up PMOS transistors in pull up networks.

Another structure as one logic style full adder is complementary pass transistor logic (CPL). This structure provides a full swing output voltage. Due to use of fast differential stage of cross coupled PMOS transistors and output static inverters, good driving capability is obtained in these structures [3]. Of course, the good driving capability and high speed characteristic in these structures are obtained in cost of more leakage current and hence more static power dissipation.

Transmission gate full adders (TGA) [5,6], which are based on transmission function theory, have no voltage drop, but it is necessary to double the number of transistors in order to design a similar function.

Transmission function full adder (TFA) [6] and TGAs are suitable structures to design XOR and XNOR gates. But these structures do not provide a good driving capability. Their performance significantly degrades when they are used in cascaded structures. So, in order to solve this problem we need to add buffers to these structures.

One of the most important aspects in designing VLSI circuits is their power consumption. [9-12]. Since 1980s, by introducing standard CMOS Logic, many researchers have proposed solutions to decrease power consumption in digital VLSI chips. The challenge of power consumption is always a limiting factor for high performance systems.

GDI structures, which were primarily introduced for fabrication in silicon on insulator and twin-well CMOS processes, were introduced as an alternative to static CMOS logics [13]. By using GDI structure, complex logic functions can be implemented using only two transistors. Compared to standard CMOS implementations, GDI structure reduces the dynamic power in combinational and sequential logics. Although GDI gates suffer from reduced voltage swing at their outputs, which causes degradation in performance, a significant power reduction is the advantage of using these gates. Many researchers are focusing on minimizing the performance penalty of these structures.

Many researchers studied the efficiency of sequential and combinational logic using GDI [13-20]. GDI flip-flops, adders, comparators, multiplexers and counters were implemented using 0.18μm to 65nm CMOS technologies, showing improvements in power consumptions [21].

In this paper, an ultra-low-power full adder is proposed in 90nm CMOS technology which provides full-swing output. Combination of an inherited low power GDI structure and forced stacking technique in implementing different functions, and using stacked inverters after each gate results in an ultra-low-power and full-swing full adder cell. These desirable performances are achieved in cost of more occupied chip area.

So, this paper is organized as follows: Section 2 overviews the GDI structure. In section 3, the proposed full adder is given. Section 4 analyses and discusses the results of simulations and finally, the paper is concluded in section 5.

2. REVIEW of GDI STRUCTURE

The Gate-Diffusion-Input cell, which is shown in figure (1), consists of two transistors. Although the structure is similar to the conventional CMOS inverter, it contains three inputs. The inputs, as it shown in figure (1), are inserted as follow: the 'G' is the common gate input, the 'P' is the source-drain of the PMOS input, and the 'N' is the source-drain of the NMOS input.

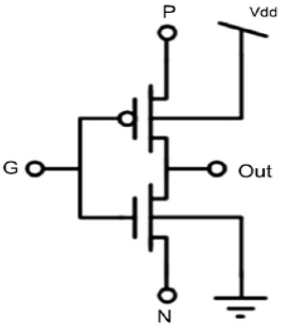


Fig. 1. The Basic GDI Cell

By changing the input configuration of a GDI cell, different Boolean functions can be implemented. So, implementation of complex functions can be achieved using combination of simple structures.

Table (1) demonstrates the Boolean functions synthesized by a GDI structure. The most complex function that can be implemented by GDI structure is the Multiplexer (MUX). This structure is very efficient in compare to conventional CMOS implementations [22].

The GDI structures shown in figure (1) suffer from reduced current drive due to threshold voltage drop across the transistors. This phenomenon also results in increased static power consumption in cascaded inverters. Morgenstein and et al. in [23] proposed a solution using swing restoration buffers. They suggest using low threshold transistors in order to avoid significant voltage drop.

CMOS NOR/NAND gates are vastly used in design of static digital circuits, because these gates are implemented simply by four transistors. GDI MUX/AND/OR gates are also implemented by the same number of transistors. Moreover, GDI provides two more functions named F1 and F2 in table (1). It is shown in [23] that more efficient functions can be synthesized using these two function by GDI. In figure (2), a comparison between number of functions that can be synthesized by NAND gates and F1 is investigated [22].

Table 1. Boolean Functions implemented by a GDI Structure

N	P	G	Out	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	Or
B	0	A	AB	And
C	B	A	$\bar{A}B+AC$	Mux
0	1	A	$\bar{A}$	Not

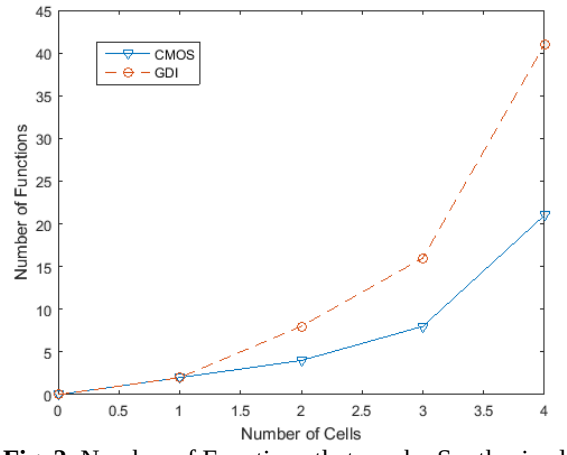


Fig. 2. Number of Functions that can be Synthesized by NAND Gates and F1 [22]

3. The PROPOSED FULL ADDER

In this section, a simple ultra-low-power full adder cell is proposed. By considering the truth table of the full adder, it can be noticed that C_{out} is equal to (A or B) whenever C_{in} is 0, and C_{out} is (A and B) whenever C_{in} is 0. So two AND gates and a multiplexer is required to implement C_{out} at the output. In a same way, SUM can be implemented. Whenever C_{out} is equal to 0, the SUM is equal to (A or B or C_{in}), and whenever C_{out} is equal to 1, the SUM is equal to (A and B and C_{in}). So two multiplexers, two OR gates and two AND gates are required for a one-bit full adder cell, as it is shown in figure (3).

In this paper, we have used the benefits of Basic GDI structure for implementing each gate. The basic GDI cell and its truth table are demonstrated in figure (1) and table (1), respectively.

Figure (4) demonstrates the proposed full adder, and figure (5) shows the structure of the low power drivers used to obtain full swing voltages. Considering figure (1), by connecting N input to V_{dd}, P input to B and G input to A, OR gate can be implemented. Using stacking technique for this configuration leads us to have an ultra-low power OR gates shown in figure (4). Also, considering figure (1), by connecting G to A, N to B and P to ground, and using stacking technique, ultra-low power AND gate can be implemented, and again in a same way implementing ultra-low power multiplexers are done as it is shown in the figure. For producing C_{out}, C_{in} roles as a selector of a multiplexer and is connected to G. (A AND B) and (A OR B) are also connected to P and N, respectively. For producing SUM, C_{out} roles as a selector and (A OR B OR C_{in}) is connected to P and (A AND B AND C_{in}) is connected to N.

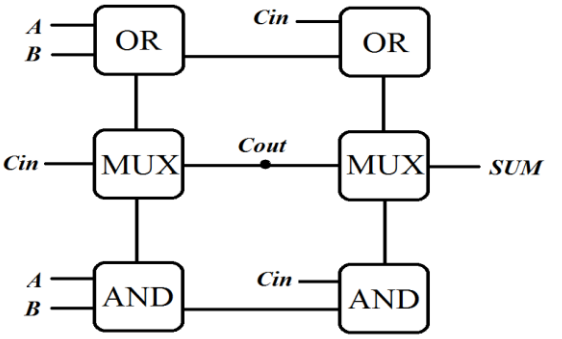


Fig. 3. Logic Scheme of the Proposed Full Adder [1]

As it can be seen, by using series transistor with half the width as one (using stacking technique), leakage power can be reduced. Two buffers are used after each gate in order to provide a full swing voltage. In the structure of each driver, the stacking technique is also used as it is shown in figure (5). In such a way ultra-low power and full swing characteristic for the full adder cell is provided.

4. SIMULATION RESULTS

In this section, the proposed Full Adder cell is simulated in HSPICE using 90nm CMOS technology parameters. The full adder cell is simulated with 50MHz frequency at 27^{O}C. The Inputs and outputs of the proposed full adder are demonstrated in figure (6).

The performance of the proposed full adder is analyzed under different values of supply voltages. Figure (7) shows the power, delay and the power-delay-product (PDP) of the proposed full adder. The delay is measured from when the input reaches 50% of its value till the output reaches its 50% value. The proposed full adder shows a great reduction in consuming power, due to the changes in the structure of each function. Of course, the ultra-low-power characteristic of the full adder is obtained in cost of more delay and larger occupied chip area.

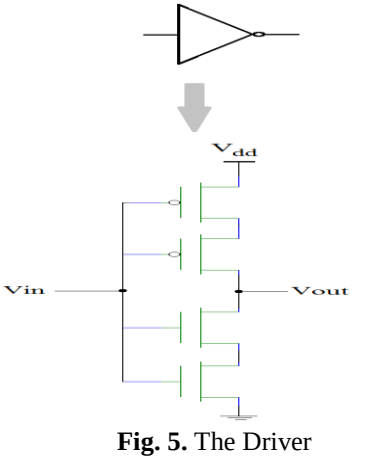


Fig. 5. The Driver

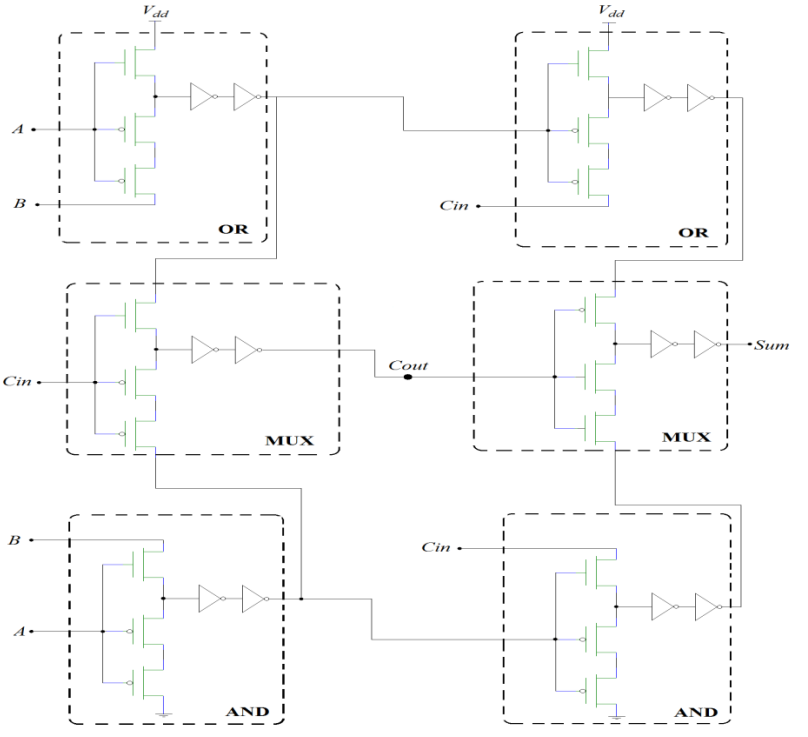


Fig. 4. The Proposed Full Adder

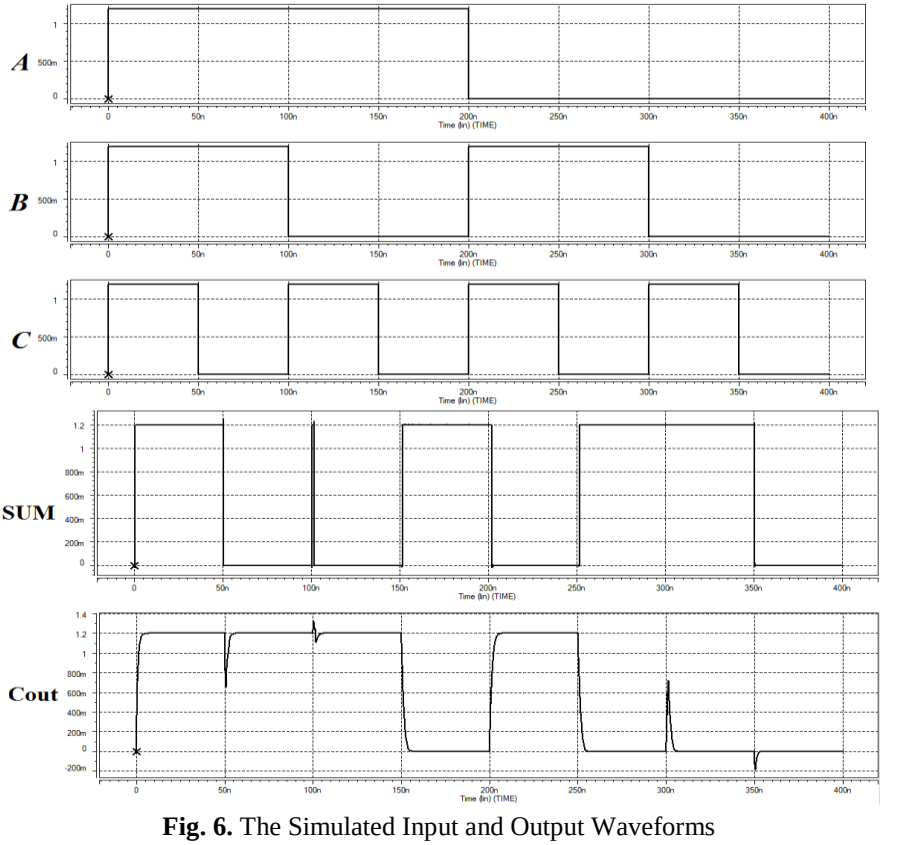
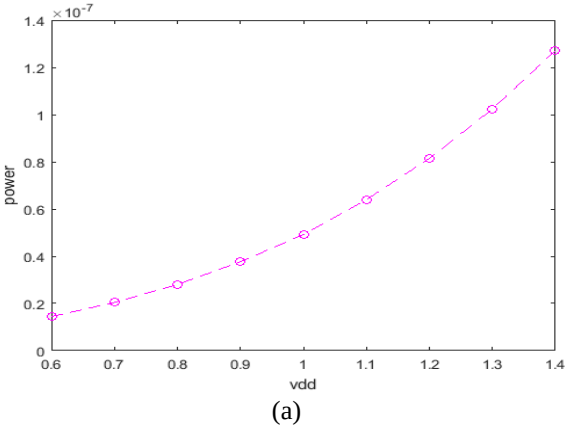
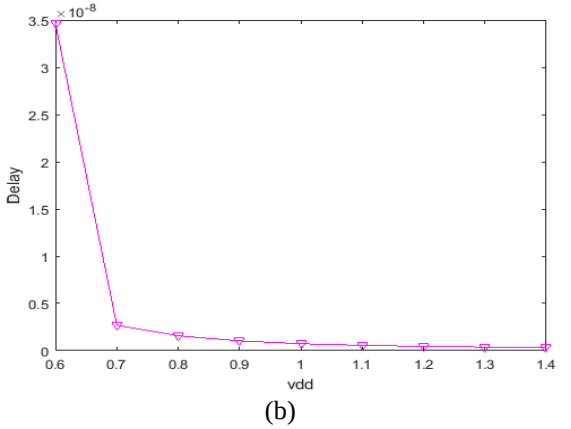


Fig. 6. The Simulated Input and Output Waveforms

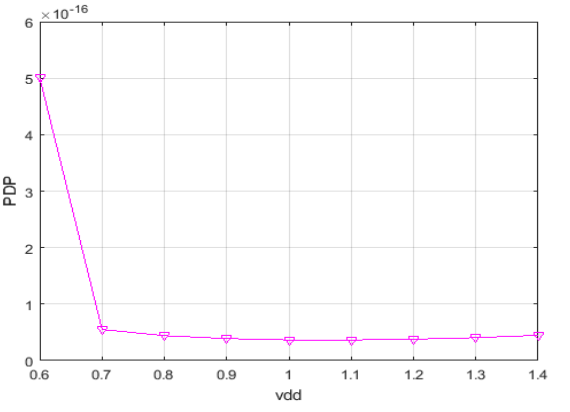
PDP is a quantitative measure which is significant when low power operation is needed. As it is shown in figure (8), the PDP of the proposed full adder is less than other related works for more than 0.95v supply voltage. This indicates the advantage of the proposed full adder over other works. The PDP of the proposed full adder is decreased in compare to [7] (ULPFA) and [1] (GDI-MUX), respectively for 1.2v supply voltage. This reduction in PDP is achieved due to the added transistors which results in reduction of sub threshold current. Hence the power consumption is reduced and delay of the system is increased. Of course, the rate of reduction in power consumption is more than the rate of growth in delay. So, the PDP is improved.



(a)



(b)



(c)

Fig. 7. a) Power, b) Delay and c) PDP of the proposed full adder for Different Supply voltages

Also, simulation of PDP under different load conditions is shown in figure (9). Figure (10) compares the results with other works. As it is shown, the PDP is decreased a lot, due to reduction of power.

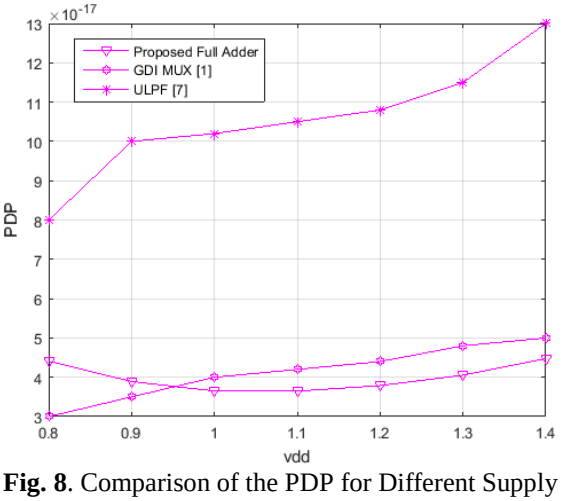


Fig. 8. Comparison of the PDP for Different Supply Voltages

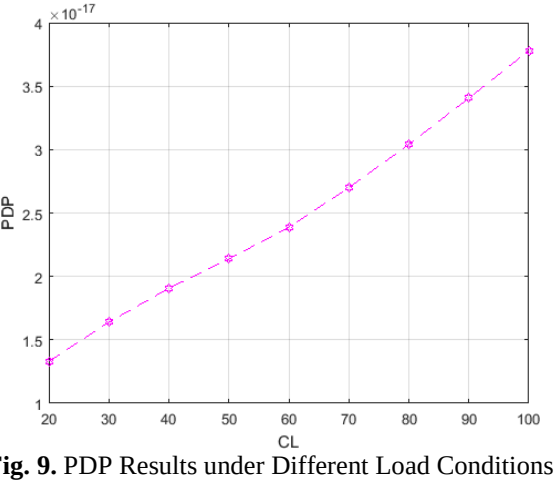


Fig. 9. PDP Results under Different Load Conditions

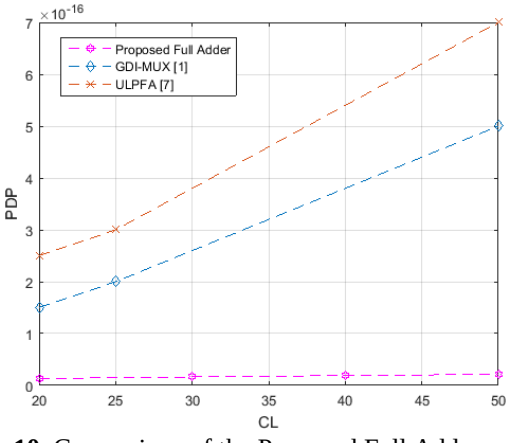


Fig. 10. Comparison of the Proposed Full Adder under Different Load Conditions

Table 2. Simulation Results for 1.2v supply voltage

Design	Power(w)	Delay (s)	PDP (j)
ULPFA [7]	1.65×10^{-6}	3.86×10^{-11}	6.38×10^{-17}
Hybrid [1]	1.34×10^{-6}	3.04×10^{-11}	4.11×10^{-17}
GDI-MUX	1.03×10^{-6}	3.67×10^{-11}	3.81×10^{-17}
Proposed Full Adder	81.47×10^{-9}	4.64×10^{-10}	3.78×10^{-17}

Table (2) compares the results of the proposed full adder cell with other works. As the table exhibits, the power consumption is decreased by order of 2, and the delay is increased only by order of 1. Results indicate that the proposed full adder has some superiors over the other ones.

In order to analyze the noise tolerance performance of the proposed full adder, noise immunity curve (NIC) is used. A sufficiently long duration and high amplitude is needed for a noise pulse to cause logic errors. Figure (11) shows the noise injection circuit, introduced in [1]. This circuit provides a noise pulse with desired amplitude and width. By varying V_P and V_T the amplitude and the width of the signal is under control. Whenever a glitch appears in the output and causes unrecoverable logic errors, we say the noise affects the output. Figure (12) shows the NIC results and compares it with results in [1]. Each point under the NIC is in the safe zone.

Also, effect of temperature variation on power consumption, delay and PDP of the proposed full adder is simulated. Results are stated in table (3). Figure (13) demonstrates the effect of temperature variation on delay and power, and figure (14) compares the effect of temperature variation on PDP with other reported works in [1].

Table 3. Effect of Temperature variation on Delay, Power and PDP of the Proposed Full-Adder

Temp.	Delay (s)	Power (w)	PDP (J)
0^{O}C	1.5748×10^{-10}	24.7n	3.88×10^{-18}
25^{O}C	1.622×10^{-10}	81.47n	1.32×10^{-17}
50^{O}C	1.6704×10^{-10}	225.0n	3.75×10^{-17}
75^{O}C	1.7102×10^{-10}	538.17n	9.2×10^{-17}

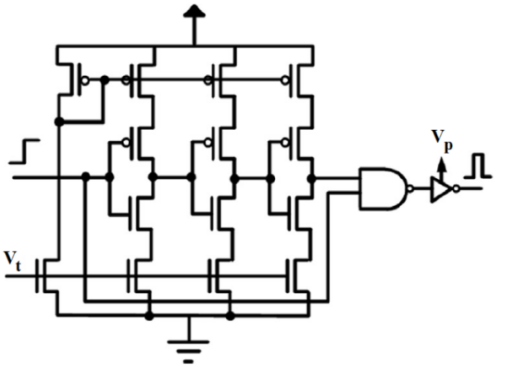


Fig. 11. Noise Injection Circuit introduced in [1]

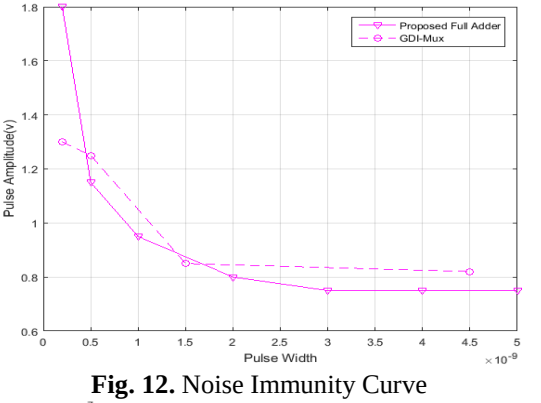
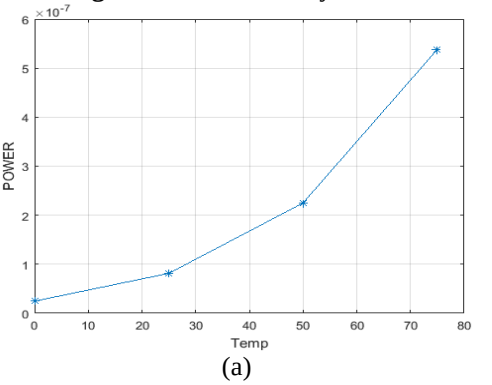
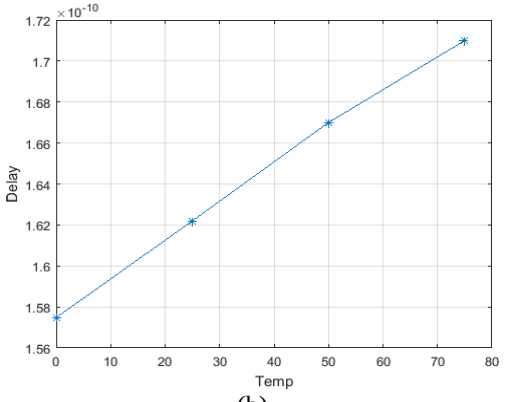


Fig. 12. Noise Immunity Curve



(a)



(b)

Fig. 13. Effect of Temperature variation on A) Power and B) Delay

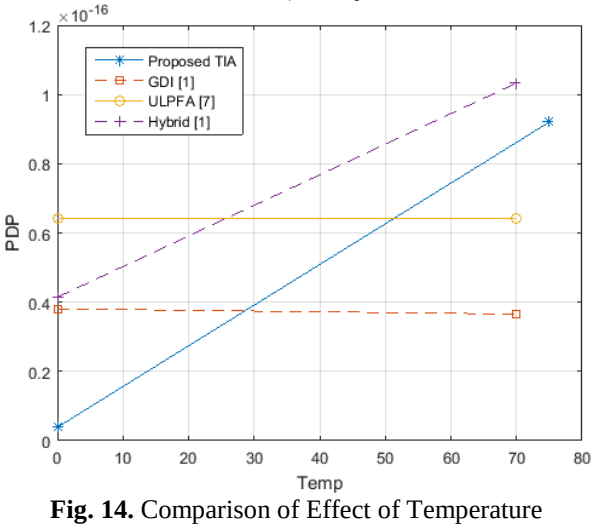


Fig. 14. Comparison of Effect of Temperature Variation on PDP

5. CONCLUSIONS

In this paper, a GDI structure is used to provide different functions to obtain a full adder cell. The idea is to reach an ultra-low-power cell. So, stacking technique is used in different functions which results in more delay and imperfect output voltages. To solve this problem, two inverters with stacking technique are used after each function to obtain full swing outputs besides achieving low power characteristics. These characteristic are obtained in cost of more occupied chip area and higher delay, But the PDP of the proposed full adder is improved in compare to other works. Results of simulations using 90nm CMOS technology library in HSPICE indicate proper performance of the proposed cell as an ultra-low-power full adder.

REFRENCES

[1] V. Foroutan, M. Taheri, Keivan Navi, A. Azizi Mazreah, **"Design of two Low-power full adder cells Using GDI structure and Hybrid CMOS Logic Style"**, *INTEGRATIN: the VLSI Journal (Elsevier)*, Vol. 47, pp. 48-61, 2014.

[2] R. Gu, M. Elmasry, **"Power dissipation analysis and optimization of deep submicron CMOS digital Circuits"**, *IEEE Journal of Solid-State Circuits*, Vol. 31 (5), pp. 707-713, 1996.

[3] C.H. Chang, G.M. Zhang, **"A review of 0.18um full-adder performance for tree structure arithmetic circuits"**, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 13 (6), 2005.

[4] Y. Jiang, A. Sheraidah, Y. Wang, E. sha, J. Chung, **"A novel multiplexer based low power full adder",** *IEEE Transactions on circuits and systems II*, Vol. 51 (7), 2004.

[5] M. Vai, **"VLSI Design",** *CRC Press, Boca Raton*, FL, 2001.

[6] V. Dessard, **" SOI Specific Analog Techniques for low noise, high performance or Ultra low power Circuits"**, *Ph.D. Thesis*, UCL, Louvain, Belgium, 2001.

[7] D. Hassoune, I. Flandre, Connor, J. legat, **"ULPFA: a new efficient design of a power aware full adder"**, *IEEE Transaction on Circuits and Systems*, Vol. 57 (8), 2010.

[8] D. Levacq, C. Liber, V. Dessard, D. Flandre, **"Composite ULP diode fabrication modeling and applications in multi-FD SOI CMOS technology",** *Solid State Electronics*, Vol. 48 (6), pp. 1017-1025, 2010.

[9] M. Alioto, **"Ultra low power VLSI Circuit design demystified and explained"**, *IEEE Transactions on Circuits and Systems on Circuits and Systems*, Vol. 59 (1), pp. 3-29, 2012.

[10] D. Bol, **"Robust and energy efficient ultra-low voltage circuit design under timing constraints in 65/45nm CMOS"**, *Journal of Low Power Electronics and Applications*, Vol. 1(1), pp. 1-19, 2011.

[11] G. Chen, M. Fojtik, D. Kim, and etc., **"Millimeter scale nearly perpetual sensor system with stacked battery and solar cells"**, *In Proceedings of IEEE International Solid State Circuits Conference digest of technical papers (ISSCC)*, 2010, pp. 288-289.

[12] I. Vaisband, E. G. Friedman, r. Ginosar, A. Kolodny, **"Low-power Clock network design"**, *Journal of Low Power Electronics and Applications*, pp. 219-246, 2011.

[13] A. Morgenshtein, A. Fish, I. Wagner, **"Gate Diffusion input (GDI)- a power efficient method for digital combinatorial circuits"**, *IEEE Transactions on VLSI systems*, Vol. 10 (5), 2002.

[14] M. Kumar, M. A. Hussain, L.L.K. Singh, **"Design of a low power high speed ALU in 45nm Using GDI technique and its performance comparison communications in computer and information science**'', 142 (part 3), pp. 458-463, 2011.

[15] K. Chaddha, R. Chandel, **"Design and analysis of a modified low power CMOS full adder using gate-diffusion input technique"**, *Journal of low power electronics*, Vol. 6 (4), pp. 482-490, 2010.

[16] O.P. Hari, A. Mai, **"Low power and area efficient implantation of N-phase non overlapping clock generator using GDI technique"**, *in Proceedings of IEEE International Conference on Electronics Computer Technology (ICECT)*, 2011.

[17] P.M. Lee, C. Hsu, Y. Hung, **"Novel 10-T full adders realized by GDI structure"**, *in: proceeding of the IEEE International Symposium on integrated Circuits*, 2007.

[18] F. Moradi, D.T. Wisland, D.T.H Mahmoodi, H. Aunet, T.V. Cao, A. Peiravi, **"Ultra Low power full adder topologies"**, *in: proceedings of ISCAS'04, Taipei, Taiwan*, 2009.

[19] A. Morgenshtein, A. Fish, I.A. Wagner, **"An efficient implementation of D-Flip flop using the GDI technique"**, *in: proceedings of ISCAS'04 Conference, Canada*, pp. 673-676, 2004.

[20] R. Uma, P. Dhavachelvan, **"Modified gate diffusion input technique",** *a new technique for enhancing performance in full adder circuits, proceeding of ICCCS6*, pp. 74-81, 2012.

[21] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, A. Fish, **"Full-swing Gate Diffusion Input Logic-case-study of low Power CLA adder design",** *INTEGRATION: the VLSI Journal (Elsevier)*, Vol. 47, pp. 62-70, 2014.

[22] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, A. Fish, **"Full-Swing Gate Diffusion Logic-Case-Study of low-Power CLA adder design",** *INTEGRATION the VLSI Journal (Elsevier)*, Vol. 47, pp. 62-70, 2014.

[23] A. Morgenstein, I. Shwartz, A. Fish, **"Gate diffusion input (GDI)-a power efficient method for digital combinatorial circuits**", *IEEE Transactions on VLSI Systems*, Vol. 10 (5), 2002.

[24] M.G. Priya, K. Baskaran, D. Krishnaveni, " **Leakage power Reduction technique in deep Submicron Technologies for VLSI Applications"**, *International Conference on Communication technology and System Design*, pp. 1163-1170, 2012.