ΔΣ Fractional-N Synthesizer for GSM-E-900 Frequency Standard

AliReza Bagherzadeh[1], Mostafa Yargholi[2]
1. Department of Electrical Engineering, University of Zanjan, Zanjan, Iran,
Alireza.bagherzadeh@znu.ac.ir
2. Department of Electrical Engineering, University of Zanjan, Zanjan, Iran.
yargholi@znu.ac.ir

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ABSTRACT:
This paper presents an integrated phase-locked loop (PLL) frequency synthesizer for wireless communication application in standard 0.18 µm CMOS process. Delta sigma modulator used for reducing phase noise. The use of ΔΣ modulation concepts results in a beneficial noise shaping of the phase noise (jitter) introduced by fractional-N division. The this technique has the potential to provide low phase noise, fast settling time, and reduced impact of spurious frequencies when compared with existing fractional−N PLL techniques. Simulation results show that the phase noise of frequency synthesizer is -108 $\frac{dBC}{Hz}$@1MHz offset, and the PLL synthesizer provides output frequencies 880-915 MHz in uplink and 925-960 MHz in downlink. F_{ref} is 26 MHz and channel spicing is 700 KHz. Moreover, benefiting from the combination of current-mode-logic (CML) the PLL consumes a total power dissipation of only 24.35 mW with a single 1.8 V supply including all the buffers. Although prescaler increases settling time (ts), it decreases power consumptions. Settling time in uplink is 425 ns and in downlink about 475 ns.

KEYWORDS: Frequency Synthesizer, Sigma-Delta, Phase noise, Settling time, GSM-E, PLL.

1. INTRODUCTION

Today's mobile communication systems require a higher quality of communication, higher data rates, more increased frequency operation, low power dissipation, and more channels per unit bandwidth [1-4]. Phase-Lock loops (PLLs) have been one of the basic building blocks in modem electronic systems. They have been widely used in communications, multimedia and many other applications among which may include wireless telecommunication networks such as GSM, DCS, NADC, CDMA, DECT. In this article, we are interested in the GSM-E. The objective of this work is the design and simulation of a frequency synthesizer which capable of generating different frequencies used by GSM-E operating in one of its band [880-915] MHz for transmission and [925-960] MHz for receiving with a channel spacing of 700 KHz.

2. THEORY AND DESIGN

The frequency synthesizer is shown in Fig.1 is the most form of PLL used in RF communications applications. In this architecture, the PFD compares the phase of the signal at the output of the frequency divider (F_c) with a reference signal (F_{ref}) generated by a crystal oscillator and it generates a signal Up and Down. when F_{ref} is in the phase advance compared to Fc called Up signal and when F_{ref} is in the phase delay compared to Fc called Down signal. The charge pump consists of a source and a current sink for injecting or withdrawing a current I_{cp} in the low pass filter which converts it into a control voltage for setting the oscillation frequency of the VCO. The VCO generates a sinusoidal signal whose frequency F_{out} varies around this oscillation frequency and the frequency divider divides by N allowing to compare it with the reference signal of lower frequency [5].

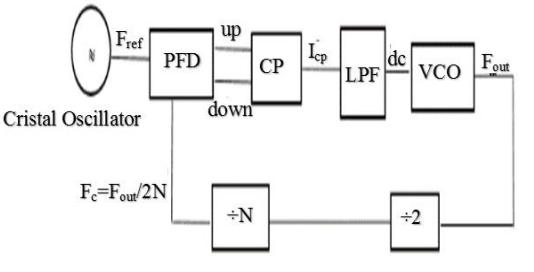

Fig. 1. PLL-Frequency synthesizer

Generally for estimation behavior of PLL and calculate the values of resistors and capacitors in low

pass filter, it is necessary to use the Transfer Function of the PLL. So first step is modeling Transfer Function of each block that used in PLL (Fig. 2). The loop filter has used in this work is first order low pass filter with resistor (R1) and capacitor (C1). The transfer function of PFD and CP and loop filter is F(s) [6]. At the end, VCO has a gain of Kvco (Hz/V). So H(s) as closed loop transfer function is:

$$F(s)= \frac{I_{cp}}{2\pi}\left(\frac{1}{C_1 s}+R_1\right) \quad (1)$$

$$M=2\times N \quad (2)$$

$$H(s)=\frac{\frac{I_{cp}K_{VCO}}{2\pi C_1}(R_1C_1s+1)}{s^2+\frac{I_{cp}}{2\pi M}K_{VCO}R_1s+\frac{I_{cp}}{2\pi C_1 M}K_{VCO}} \quad (3)$$

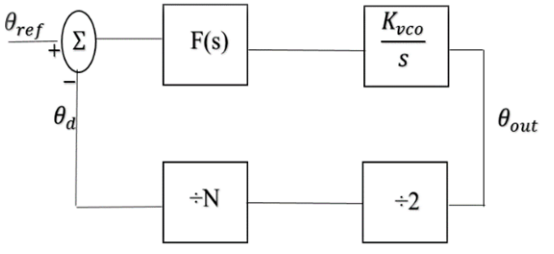

Fig. 2. Linear model of PLL

Writing denominator ass $s^2+2\xi\omega_n s+\omega_n^2$:

$$\omega_n=\sqrt{\frac{I_{cp}K_{VCO}}{2\pi C_1 M}} \rightarrow C_1=\frac{I_{cp}K_{VCO}}{2\pi\omega_n^2 M} \quad (4)$$

$$\xi=\frac{R_1}{2}\sqrt{\frac{I_{cp}C_1K_{VCO}}{2\pi M}} \rightarrow R_1=\frac{2\xi}{\sqrt{\frac{I_{cp}C_1K_{VCO}}{2\pi M}}} \quad (5)$$

$$C_2=\frac{C_1}{5} \quad (6)$$

$C_1 = 3.2$ pF $R_1 = 180$ kΩ $C_2 = 640$ fF

In the frequency synthesizers, N is changeable and according to provide final frequency N in selected.

3. SYNTHESIZER ARCHITECTURE

DELTA-SIGMA modulator based fractional-phase locked loops (PLLs) is illustrated in Fig. 3 are widely used as local oscillator frequency synthesizers in wireless communication systems because they offer excellent spectral purity with virtually unlimited frequency tuning resolution.

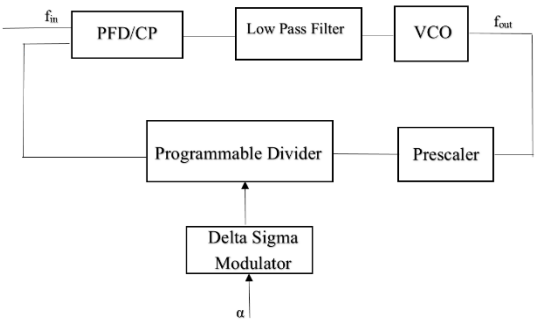

Figure. 3. Delta sigma frequency synthesizer

3.1. Phase/Frequency Detector (PFD)

Commonly used Phase/frequency detector (PFD) is employed in the synthesizer (Fig. 4) and D flipflop that used in PFD (Fig. 5). The circuit employs sequential logic to create three states and responds to the rising (or falling) edges of the two inputs. If initially $Q_A = Q_B = 0$, then a rising transition on A leads to $Q_A = 1$, $Q_B = 0$. The circuit remains in this state until B goes high, at which point Q_A returns to zero. In other words, if a rising edge on A is followed by a rising edge on B, then Q_A goes high and returns to low. The behavior is similar to the B input [7].

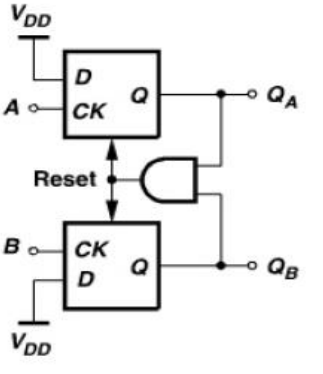

Fig. 4. The structure of the PFD

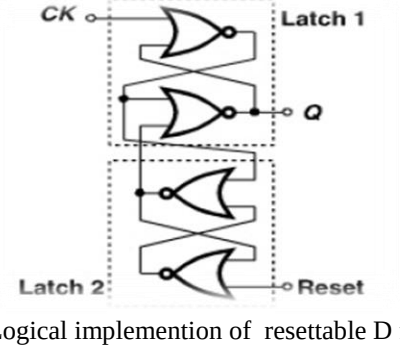

Fig. 5. Logical implemention of resettable D flipflop

3.2. Charge Pump and Loop Filter

The charge pump (Fig. 6) is responsible for converting the digital output of the PFD to a corresponding analog signal which will be filtered by a LPF. A charge pump consists of two switched current sources that pump charge into or out of the loop filter according to two logical inputs. The circuit has three states. If $Q_A = Q_B = 0$, then S_1 and S_2 are off and V_{out} remains constant. If Q_A is high and Q_B is low, then I_1 charges CP. Conversely, if Q_A is low and Q_B is high, then I_2 discharges CP. Thus, if, for example, A leads B, then Q_A continues to produce pulses and Vout rises steadily. Called UP and DOWN currents, respectively, I_1 and I_2 are nominally equal.When the loop is turned on, ω_{out} may be far from ω_{in}, and the PFD and the charge pump adjust the control voltage such that ω_{out} approaches ω_{in}. When the input and output frequencies are sufficiently close, the PFD operates as a phase detector, performing phase lock. The loop locks when the phase difference drops to zero and the charge pump remains relatively idle. A CP used in this paper is shown in Fig.7. The reference current of the designed charge pump is only 100uA.

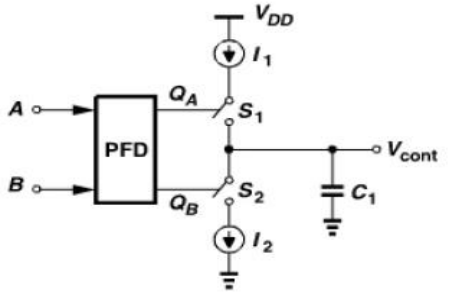

Fig. 6. PFD with charge pump

3.3. Voltage Controlled Oscillator (VCO)

In next operation, LPF converts these signals to a control voltage that is used to control the VCO. Therefore, the principle of operation is as follow: if the PFD generates an UP signal, then the VCO frequency increases; a DN signal decreases the VCO frequency. The VCO stabilizes only when F_{REF} and F_{DIV} frequency and phase coincides. Under these conditions, the PLL is locked. Thus, the VCO is the key component that controls the frequency of the PLL [8]. In this paper, we have two frequency range, so we used two VCO. The one for uplink and other for downlink.

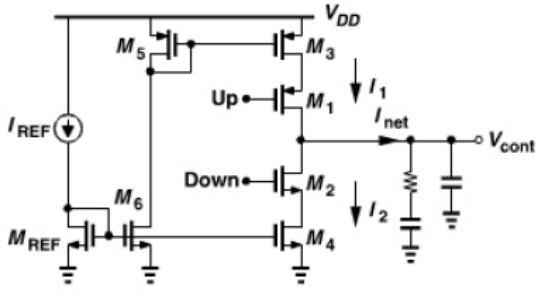

Fig. 7 The circuit for the designed charge pump

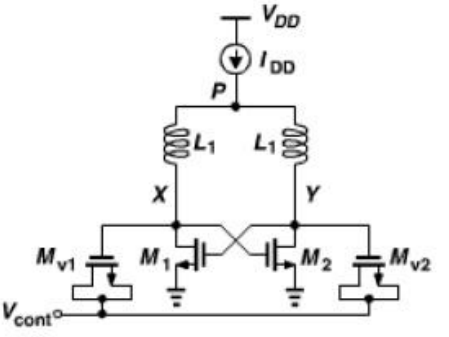

Fig. 8. A cross-coupled VCO

3.4. Prescaler and Frequency Divider

Prescaler is used for reduce power consumptions of circuit. We used CML latches with negative loops for provide divided two [9]. This circuit (shown in Fig.9) is suitable for high frequency dividing. The "basic" programmable prescaler architecture is depicted in Fig. 10. The modular structure consists of a chain of 2/3 divider cells connected like a ripple counter. The structure of Fig. 10 is characterized by the absence of long delay loops, as feedback lines are only present between adjacent cells. This "local feedback" enables simple optimization of power dissipation. Another advantage is that the topology of the different cells in the prescaler is the same, therefore facilitating layout work. Yet there are two fundamental differences. First, in all cells operate at the same (high) current level. Second, this leads to high power dissipation, because of high requirements on the slope of the strobe signal, in combination with the high load presentedby all cells in parallel [10].

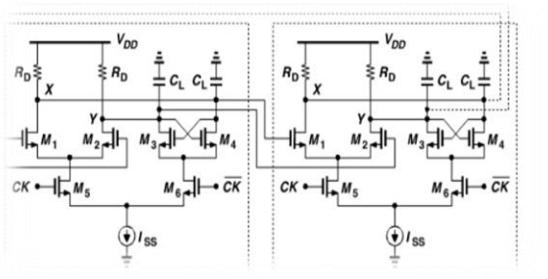

Fig. 9. CML-Prescaler

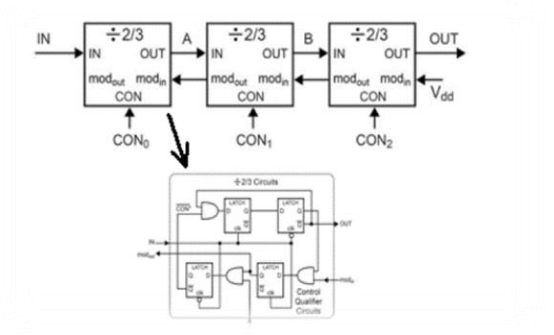

Fig. 10. A typical 3-modulus frequency divider

3.5. Delta Sigma Modulator (DSM)

The principles and fundamentals of SDMs are well described in [11]. In the following, we mention some of the points in brief [12]. 1) The utilized SDM should be as tone free as possible 2) SDMs should have a stable Direct Current input range 3) it is better for SDMs to have as few levels as possible to reduce the bad effects of the noises 4) it should be able to operate in high frequencies 5) as simple as possible to save the power and area.

Delta sigma modulator (Fig. 11) is a circuit which is able to generate sequence of 0 and 1 randomly. Making use of DSM gives the possibility of producing fractional parts of the fractional division ratios with noising shape that cause lower phase noise [13].

Shown in Fig. 12., the system incorporates an input adder (#1) (in fact a subtractor) and an integrator ("accumulator") consisting of a digital adder (#2) and a register (delay element). The first adder receives two n-bit inputs, producing an (m + 1)-bit output. Similarly, the integrator produces an (n + 2)-bit output. Since the feedback path from Y drops the two least significant bits of the integrator output, we say it introduces quantization noise, which is modeled by an additive term, Q.

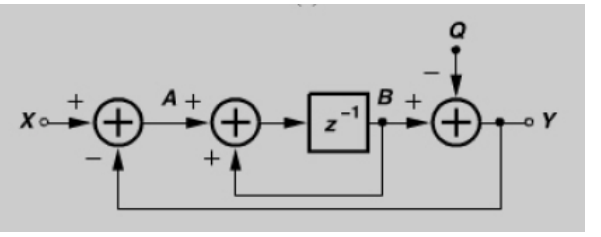

Fig. 11. First order single loop DSM

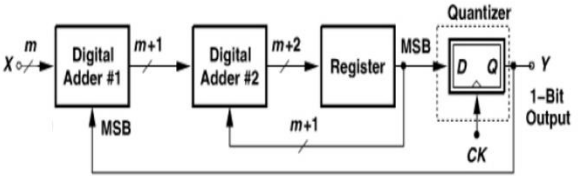

Fig. 12. Feedback system with an n-bit input

4. SIMULATION RESULT

We used ‘‘ADS2009’’ to simulate the proposed circuit. The ADS model used in the simulation is TSMC 0.18. The circuit is biased at a 1.8 V supply voltage. Transient behavior of PLL is shown in Fig.13 In the uplink frequency range, output frequency starts in 880 MHz and wants to go 915 MHz but it takes a long time to lock frequency (Fig. 13. a). Then settling time in uplink is about 425 ns.

In the downlink frequency range, output frequency starts in 925 MHz and wants to go 960 MHz but it takes a long time to lock frequency (Fig. 13. b). Then settling time in downlink is about 475 ns.

Since phase noise of downlink is important for us, it is simulated. Phase noise of the synthesizer is demonstrated Fig. 14. The total phase noise of the PLL-synthesizer is about -108 $\frac{dBC}{Hz}$@1MHz offset frequency. It is clear that if we used second order delta sigma, total phase noise will be more than -108 $\frac{dBC}{Hz}$@1MHz. Power consumptions of the circuit is 24.35 mW.

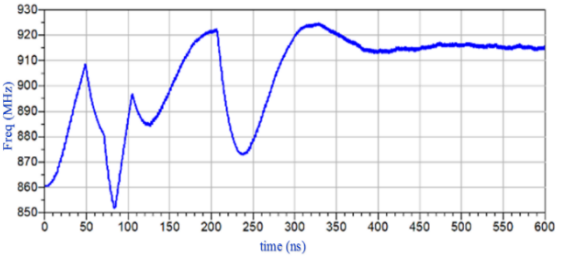

Fig. 13.a. Receiver simulation for downlink

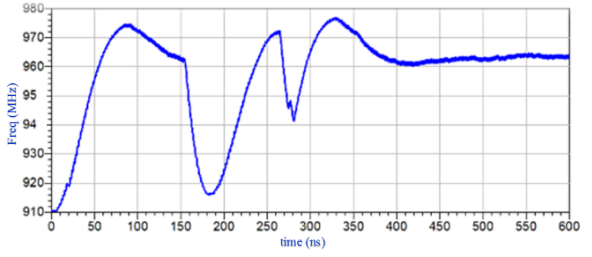

Fig. 13.b. Transient simulation for downlink

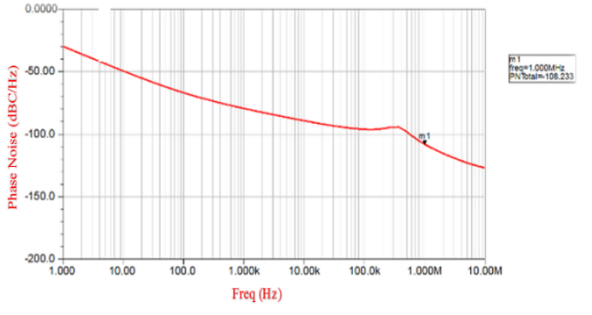

Fig. 14. Phase noise (dBC/Hertz)

5. CONCLUSION

In this paper a Delta-Sigma Fractional-N synthesizer for GSM-E-900 applications is designed and verified using ADS2009 with TSMC 0.18 µm Delta-Sigma Fractional N synthesizer is particularly well suited to integrated circuit applications. This technique allows very narrow channel spacing relative to the output frequency, large bandwidth in the PLL relative to the channel spacing, and high output frequency relative to the processing technology used in the IC. Consequently, the availability of a low-noise, low-spurious-frequency form of fractional-N division have a significant impact on the performance of low-cost frequency synthesizers for use in consumer products.

The total phase noise of frequency synthesizer is -108 $\frac{dBC}{Hz}$ @1MHz offset and power consumptions is 24.35 mW. Setteling time for uplink frequency is 425 ns and for downlink frequency is 475 ns.

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