# A 2.7 to 10.6 GHz High-Flat-Gain CMOS Low-Noise Amplifier for UWB Applications

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**ABSTRACT:**
In this paper, a low-power ultra wideband (UWB) low-noise amplifier (LNA) with high and flat gain is proposed. By using an input common-gate stage, an input matching from 3.1 to 10.6 GHz is achieved. The output matching is obtained by using the output matching network including output buffer, capacitor and inductor. In proposed LNA, current-reused technique is adopted in order to reduce the power dissipation. The proposed LNA provides high gain with excellent flatness and low noise figure over the broadband while it has very good stability too. The LNA was simulated with a TSMC 0.18-µm CMOS technology. The input and output reflection coefficients are less than -11 dB from 3 to 11GHz and -10 from 2.3 to 12 GHz, respectively. The noise figure of the proposed LNA remained under 4.3 dB from 2.2 to 10.7 GHz with minimum value of 3.12 dB. Additionally, high and flat gain of 13±1.8 dB is achieved for whole the ultra band. The linearity of input third-order intercept point is -7.76 dBm and $P_{-1dB}$ compression is -17 dBm. The power consumption at 1.5-V supply voltage without an output buffer is only 11 mW.

**KEYWORDS:** CMOS; low-noise amplifier (LNA); ultra-wideband (UWB); common-gate; noise figure (NF).

## 1. INTRODUCTION

Ultra-wideband (UWB) systems are wireless systems that transmit data over a wide spectrum of frequency bands. UWB standards have been defined by the U.S. Federal Communications Commission (FFC), since 2002. UWB systems are approved to be used in bandwidth from 3.1 to 10.6 GHz [1]. Since UWB systems could include several frequency bands, so it can be used for different applications on one chip. As a result, the costs will be reduced. In UWB front-end receivers design, the UWB low-noise amplifier (LNA) is a critical block that receives signals from the whole UWB band (3.1-10.6 GHz) and amplifies them with a good signal-to-noise ratio property. In addition, high and flat power gain $S_{21}$, good input and output impedance matching (i.e., low $S_{11}$ and $S_{22}$), and low noise figure are required for whole the frequency band. A number of UWB LNAs based on CMOS technology have been studied [2]. The distributed amplifier (DA) is one of the most popular structures for providing broadband input matching and gain [13], [14]. The major drawbacks of DAs are the large chip area and high power consumption.

The common-gate amplifier provides wideband input matching, but the input-transistor transconductance increases, so the current dissipation will be increased [15-17]. Using resistive feedback is a good solution for achieving wide bandwidth and flat power gain [18], [19]; however, the use of a resistor in the feedback path reduces the power gain and increases the NF. The reactive-feedback LNA provides broadband input matching, while introduces low noise [20]. The extra area required by the transformer-feedback network is a drawback for the overall chip size.

The proposed UWB LNA includes two stages. The first stage is a common-gate (CG) amplifier that provides wideband input matching. Since the power gain of the CG amplifier is insufficient, the common-source (CS) amplifier is employed as a second stage to amplify the weak RF signals. In order to lower power consumption, current-reused technique is used [1]. In addition, shunt peaking technique is utilized to achieve gain flatness over wideband range [3].

## 2. CIRCUIT DESCRIPTION

The proposed UWB low power LNA is shown in Fig. 1. The LNA consists of a common-gate stage $M_1$, and a common-source stage $M_2$. The input common-gate stage provides an input impedance matching and

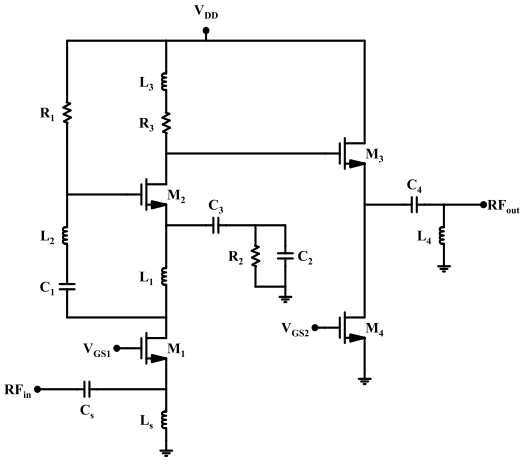


**Fig. 1.** Proposed high-flat gain LNA.

common-source stage improves gain. Using current-reused technique, cascaded topology, reduces power consumption. An output buffer is cascaded with the second stage which combines gain of lower frequencies and higher frequencies to extend ultra-wide bandwidth. $M_4$ is a current source, which provides a biasing current for $M_3$. $C_S$ and $L_S$ are parts of the input matching network. AC signal by $C_1$ and $L_2$ couples into $M_2$. $R_1$ provides a dc bias for $M_2$. $C_2$ is obtained ground for $M_2$. By adding $R_2$ in $M_2$ source, the output impedance of $M_1$ is increased, hence first stage gain is decreased and noise is amplified less. $C_3$ prevents current flow into $R_2$ and thus power consumption isn't increased. $L_3$ provides flat gain by resonating at higher frequencies. The voltage gain of $M_1$ becomes [1]

$$A_{v1} = (g_{m1}/1 + g_{m1}R_S).Z_{out1} \quad (1)$$

where $Z_{out1}$ is the output impedance of $M_1$, $R_S$ is the source impedance and $g_{m1}$ is the transconductance of $M_1$.

By using shunt peaking technique, common-source stage gain increases at lower frequencies and decreases at higher frequencies. As a result, a good gain flatness is achieved. Also, $R_3$ affects the output matching impedance and improves it strongly. The voltage gain of $M_2$ becomes [1]

$$A_{v2} = g_{m2}Z_{out2} \quad (2)$$

where $g_{m2}$ is the transconductance of $M_2$ and $Z_{out2}$ is the output impedance of $M_2$ that can be calculated as

$$Z_{out2} = Z_L \| R_T \| (1/C_T) \quad (3)$$

$$A_{v2} = g_{m2}Z_{out2} \quad (4)$$

where $R_T$ and $C_T$ are the total parasitic resistance and capacitance obtained from the drain node of $M_2$, respectively.

The noise figure (NF) of the proposed LNA is affected by the input CG stage. Noise factor F can be given by [1]

$$F \approx 1 + (g_{d0}/g_{m1}) \quad (5)$$

where $\gamma$ is the coefficient of the channel thermal noise and $g_{d0}$ is the zero-bias drain conductance.

It is shown from (5) that by increasing the $g_{m1}$, the NF reduces. Since the increase of current makes the $g_{m1}$ increase; thus, there is a trade-off between NF and power consumption. In addition, for decreasing the thermal noise of gate resistance, the multi-fingers transistors are used. In this design, the NF is achieved below 4.3 dB within the entire UWB band.

The other important characteristic of LNAs is stability. In general, to represent stability of the LNA, stability factor is used that is given by [12]

$$K = \left(1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2\right) \Big/ \left(2|S_{12}S_{21}|\right) \quad (6)$$

The necessary and sufficient condition for unconditional stability is $K > 1$. Also, the other representation of stability is given by [12]

$$\mu = \left(1 - |S_{11}|^2\right) \Big/ \left(\left|S_{22} - S_{11}^{*}\Delta\right| + |S_{12}S_{21}|\right) \quad (7)$$

and

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \quad (8)$$

If $\mu > 1$, the LNA is stable unconditionally.

## 3. SIMULATED RESULTS

The proposed high-flat gain LNA is simulated by advanced design system (ADS) using TSMC 0.18-µm RF CMOS model. The LNA consumes only 11 mW from a 1.5 V supply voltage without output buffer.

Fig. 2 shows the input and output reflection coefficients. $S_{11}$ and $S_{22}$ are less than -11 dB and -10 dB, respectively. The simulated power gain $S_{21}$ of the overall stage and the voltage gain of each stage are shown in Fig. 3. Fig. 4 shows power gain $S_{21}$, and isolation $S_{12}$. The LNA achieves 11~14.8 dB gain within the full operation band. The isolation is less than -52.5 dB over the bandwidth.

As shown in Fig. 5, the noise figure of the proposed LNA is 3.12 to 4.3 dB. The NF over the bandwidth is less than 4.3 dB. The simulated $P_{-1dB}$, -1dB compression point, at 6 GHz is -17 dBm, as shown in Fig. 6. The input third-order intercept point, IIP3, at 6 GHz is -7.76 dBm. Fig. 7 and Fig. 8 show that the proposed LNA is stable over wideband range.

A figure of merit (FOM) for evaluating the erformance of a wideband LNA, usually is used in papers, is defined as (9) [7]

$$FOM_1 = \frac{S_{21}.BW[GHz]}{(NF - 1).P_D[mW]} \quad (9)$$

Since in LNA design the noise figure and the input matching impedance have more importance, the other FOM is defined as (10)

$$FOM_2 = \frac{|S_{11}|.S_{21}.BW[GHz]}{(NF)^2.P_D[mW]} \quad (10)$$

where $NF_{max}$ is used in both (9) and (10).

The performance of the proposed high-flat-gain LNA is compared with other works, which is summarized in Table 1. Since, more other works are implemented on chip and their results are measured, for a correct comparison of the proposed LNA with other works, some of them are simulated by advance design system. It is found that the proposed LNA achieves a low noise figure, good gain flatness and good input and output matching. Also, stability of the LNA is very good. In addition, the LNA power consumption with its biasing circuit losses is low.

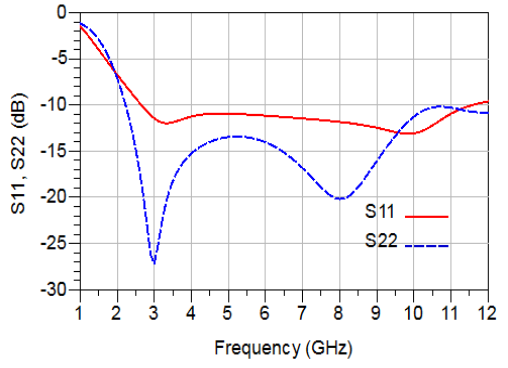


**Fig. 2.** Input and output reflection coefficients of proposed UWB LNA.

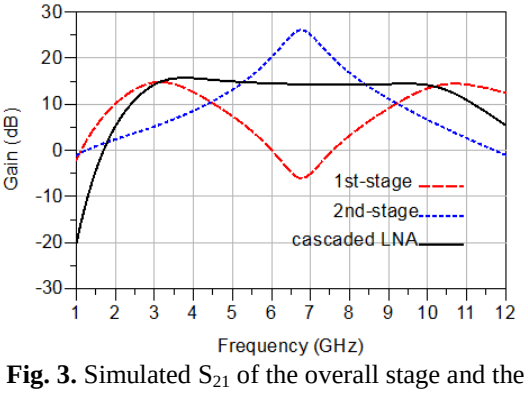


**Fig. 3.** Simulated $S_{21}$ of the overall stage and the voltage gain of each stage.

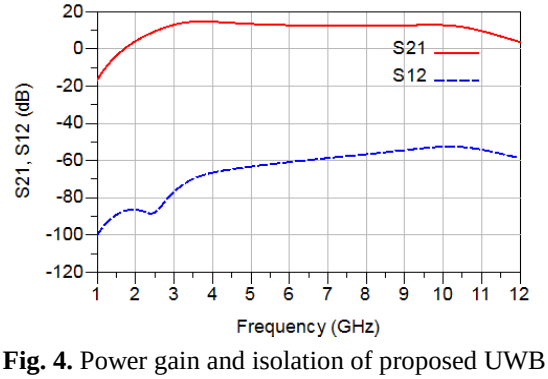


**Fig. 4.** Power gain and isolation of proposed UWB LNA.

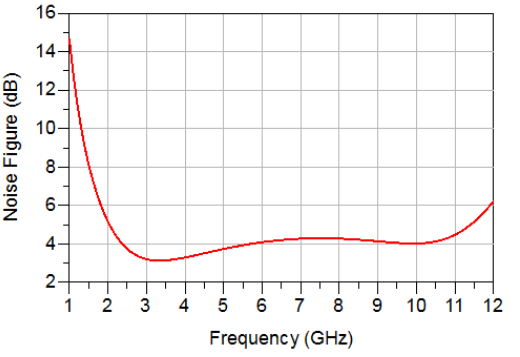


**Fig. 5.** NF of proposed UWB LNA.

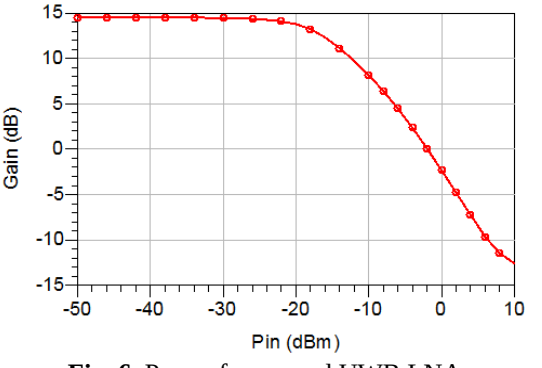


**Fig. 6.** $P_{-1\ dB}$ of proposed UWB LNA.

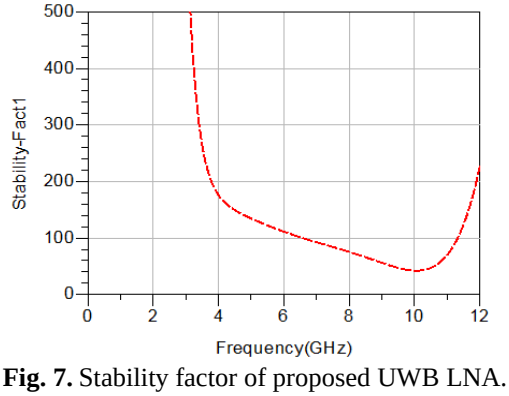


**Fig. 7.** Stability factor of proposed UWB LNA.

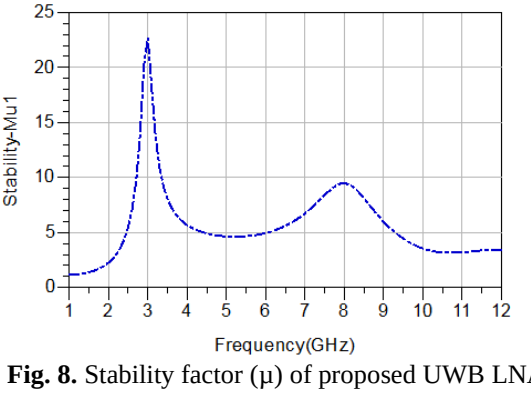


**Fig. 8.** Stability factor (μ) of proposed UWB LNA.

**Table 1.** Performance summary and comparsion to other CMOS UWB LNAs.

| Reference | [1] | [2] | [5] | [6] | [10] | This work |
|---|---|---|---|---|---|---|
| Data | Simul. | Measu. | Simul. | Measu. | Simul. | Simul. |
| Process(nm) | 180 | 90 | 180 | 180 | 180 | 180 |
| SupplyVoltage(V) | 1.5 | 1.2 | 2.25 | - | 1.8 | 1.5 |
| BW(GHz) | 3.1-10.6 | 2.6-10.2 | 3-10 | 0.5-11 | 3.1-10.6 | 2.7-10.6 |
| Power(mW) | 8.2 | 7.2 | 15.5 | 14.4 | 33.2 | 11 |
| $S_{11}$ (dB) | < -10 | < -9 | < -10 | < -9 | < -9 | < -10.24 |
| $S_{22}$ (dB) | < -10.3 | - | - | - | < -13 | < -10.21 |
| $S_{21}$ (dB) | 8.5-17.4 | 12.5 | 6-13.7 | 10.2 | 15.9-17.5 | 11.2-14.8 |
| $S_{12}$ (dB) | < -59 | < -45 | < -41.3 | - | < -70 | < -53 |
| NF (dB) | 4.1-5.8 | 3-7 | 2.8-5.5 | 3.9-4.5 | 3.1-5.7 | 3.12-4.3 |
| $P_{-1dB}$(dBm) | -18 | -12 | -5.75 | - | - | -17 |
| IIP3(dBm) | -6.97 | - | 2.59 | -9.1 | - | -7.76 |
| $FOM_1$(GHz.mW$^{-1}$) | 2.46 | 2.19 | 0.98 | 2.12 | 0.8 | 2.83 |
| $FOM_2$(GHz.mW$^{-1}$) | 3.52 | 2.42 | 1.47 | 3.3 | 1.04 | 5.17 |

## 4. CONCLUSION

This paper has proposed a two-stage LNA topology for 3-10 GHz UWB applications. The proposed LNA is designed with TSMC 0.18-µm CMOS technology. By using the input stage, a wideband input matching is achieved.

The low NF is obtained by using multi-finger transistors and resistance $R_2$. By using $R_3$, high and flat gain is achieved. The simulated maximum power gain is 14.8 dB and $NF_{min}$ is 3.12 dB. The $P_{-1dB}$ and IIP3 are -17 dBm and -7.76 dBm at 6 GHz, respectively. The total power consumption, including the buffer, is 20.73 mW with 1.5 V supply voltage. The proposed UWB LNA that is compared with other LNAs has low noise figure over the whole UWB, high gain, excellent gain flatness, very good stability, high bandwidth, and highest amount of figure of merits.

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