Wide Tuning Range and High Quality Factor MEMS Variable Capacitor with Two Movable Plates in 0.18μm CMOS Technology

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ABSTRACT:
This article introduces the reader to the performance limitations of micro electro mechanical gap-tuning capacitors fabricated in the commercially PolyMUMPs (Polysilicon Multi-user MEMS Process) foundry. And the advantages of the CMOS technology to fabrication of MEMS tunable capacitors are discussed. Also to increase the both of tuning range and quality factor, a three-plate MEMS tunable capacitor with two movable plates is designed and simulated. The simulation of the capacitor was done using the EM3DS software which is demonstrated wide tuning range (300 percent), that is 6 times higher than tuning range of the conventional parallel plate capacitor. The proposed capacitor are designed by using the ALCU metal layers of TSMC 0.18 μm CMOS technology that have caused decreasing the series resistance and increasing the quality factor to 300 in 1 GHZ.

KEYWORDS: Three-Parallel Plate MEMS Tunable Capacitor, Electro Mechanical Gap-Tuning Capacitors.

1. INTRODUCTION

The increasing market demand for low-cost radio frequency integrated circuits (RFICs) with smaller size, lower loss, higher tuning range, higher linearity, and low power consumption has generated great interest in on-chip passive components. In recent years, micro electromechanical systems (MEMS) has become an emerging technology for radio frequency (RF) and wireless communications. In particular, MEMS tunable capacitors are desired elements for microwave and wireless circuits as phase shifters, tunable filters and voltage-controlled oscillators (VCO) [1]. In general, the capacitance of the capacitor with two electrodes of area A, separated by a gap d and the dielectric constant ε, can be written as

$$C = \frac{\varepsilon A}{d} \quad (1)$$

Thus the MEMS tunable capacitors can be classified based on their tuning schemes such as gap tuning [2], area tuning [3] and dielectric tuning [4]. The tunable capacitor can be made by one of the electrodes suspended on the top of a fixed electrode. The suspended electrode, supported by micromachined springs, that is movable in the vertical direction normal to the substrate. The gap between the movable and the fixed electrodes can be adjusted electrostatically by applying a tuning voltage, resulting in a change in its capacitance. The electrostatic actuation is preferred over the other actuation mechanisms such as thermal [5] or piezoelectric actuations [6], because of its low power consumption. This article is intended as a comprehensive survey to the design of RF MEMS electrostatically gap tuning varactors and every configurations are discussed to improve the electrical parameters of these varactors, such as the tuning range and the quality factor.

In the past decade, PolyMUMPs process is widely used for MEMS tunable capacitors fabrication. This article discusses the design of tunable parallel plate capacitors (varactors) fabricated in the commercially Poly-MUMPs process. And, to increase the both of tuning range and quality factor of conventional two parallel plate capacitor, a new three-plate capacitor using the 0.18μm CMOS technology is proposed that it has two movable plates and one fixed plate. The design and fabrication issues are discussed and the simulation results are presented.

CMOS technology is fast, reliable, repeatable, cheap and it has proven itself over the years to be a universally accepted manufacturing process for integrated circuits. The fabrication of MEMS variable capacitor in commercially CMOS technology, with a

minimum feature size can push MEMS technology to higher integration which it improves performance of RF integrated circuits (RFICs) and results in the elimination of bulky off-chip components.

2. GAP-TUNING MEMS CAPACITORS IN POLYMUMS PROCESS

In the past decade, PolyMUMPs process is widely used for building varactors. Figure 1 shows the features of the Poly-MUMPs process along with a limited set of the material properties for each layer of the process. The silicon nitride is the first layer, which provides electrical isolation between the substrate and the surface micromachined structure being built on top of the substrate. This process contain three layers of polysilicon (Poly0, Poly1 and Poly2), which constitute the main structural layers. And one metal gold layer is available, on top of Poly2. Also the process provides two sacrificial layers of oxide that can be etched away to releasing the micromechanically movable structures.
Traditional electro-mechanically gap-tuning MEMS capacitors are made up of two parallel plates. Figure 2 shows a simplified model of this MEMS capacitor. The top plate of the capacitor is movable and suspended by a spring with spring constant, *k*, while the bottom plate is fixed mechanically. The process provides one metal layer, but a tunable capacitor is formed using two conducting parallel layers separated by a dielectric region. Therefore, the fixed plate can be created using the conducting Poly0 layer, or by using a stacked configuration of the Poly0 and 1 layers. The suspended plate can only be formed by etching away one or more of the oxide layers to allow vertical movement. The suspended plate can be formed by depositing gold on top of the Poly2 layer, or it can be formed by a stacked configuration of the gold, Poly2 and Poly1 layers. Therefore, there are three layer configurations possible for building MEMS tunable capacitors in the PolyMUMPs process.
The capacitance are mechanically tuned by changing the distance separating of the plates. When a bias voltage $V_1(t)$ is applied across the capacitor plates, the movable plate is attracted to the bottom plate due to the resulting electrostatic force and thus increases the capacitance of the structure. The suspended plate moves toward the fixed bottom plate until an equilibrium between the spring and the electrostatic forces is reached. The equilibrium between the forces can be written mathematically by the following equation [7] that under steady state conditions, $x(t) = x$ and $V_1(t) = V_1$.

$$E = \frac{1}{2}\frac{\varepsilon_d A V_1^2}{(d_1 + x)} \qquad (2)$$

In this equation ε_d is the permittivity of air ($\varepsilon_d = \varepsilon_{air}\varepsilon_0$ where $\varepsilon_{air} = 1.00054$ and $\varepsilon_0 = 8.85415 \times 10^{-12}$ F/m), A is the area of the capacitor plates, and d_1 is the distance of the capacitor plates when the spring is in its relaxed state. By neglecting the fringing effect, the capacitance of the tunable capacitor, which has been formed between the two parallel plates, can be written as:

$$C_D(V_1) = \frac{\varepsilon_d A}{d_1 + x(V_1)} \qquad (3)$$

And the spring constant (*k*) for a beam is given by the following equation:

$$k = \frac{3E_y I}{l^3} \qquad (4)$$

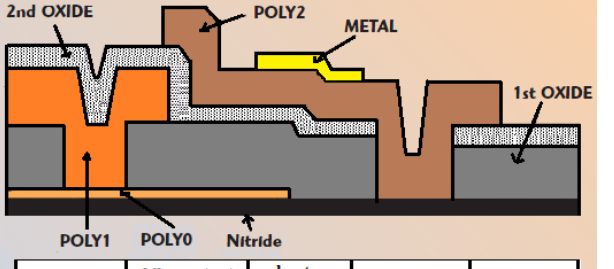
Where E is the Young's module, I is the moment of inertia for the beam and l is the beam's length.

2.1. The Tuning Range

The tuning range for a capacitor is the ratio of the difference between the maximum and minimum capacitance to its minimum capacitance that is expressed in percentage.

$$Tuning\ \ range = \frac{C_{\max} - C_{\min}}{C_{\min}} \times 100 \qquad (۵)$$

When a bias voltage is applied across the capacitor plates, the movable plate is attracted to the bottom plate but the tuning range of a gap-tuning capacitor is limited by pull-in instability that is equilibrium between the



	thikness(um) thikness(um)	sheet resistance	resistivity	conductivity
metal(gold)	0.5	0.06	$3*10^{-8}$	33333333.3
poly2	1.5	20.0	$3*10^{-5}$	33333.3
2nd oxide	0.75	N/A	N/A	N/A
poly1	2.0	10.0	$2*10^{-5}$	50000.0
1st oxide	2.0	N/A	N/A	N/A
poly0	0.5	30.0	$1.5*10^{-5}$	66666.6

Fig. 1. Description of the PolyMUMPs process

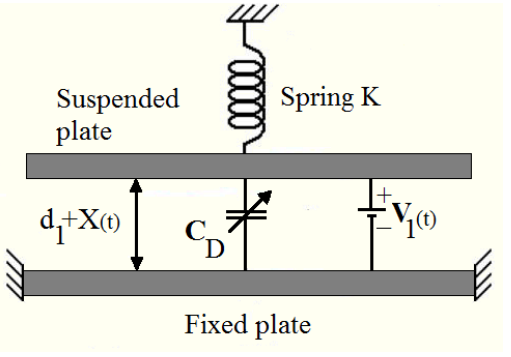


Fig. 2. A two parallel- plate capacitor

spring and the electrostatic forces exists only for displacements less than $d_1/3$. Therefore, the maximum capacitance that such a tunable capacitor can be tuned to is $3C_D/2$ and theoretically, the maximum tuning range of a gap tuning capacitor is 50 percent.

If we eliminate or delay in pull-in effect, the tuning range will be increase. In fact, more methods are used for increasing the tuning range, are brought delay in pull-in effect. One method to increase the tuning range is based on the idea of using separate electrodes for the actuation [8] or adding the restoring force of the beams [9]. Also by using two movable plates capacitor, it is possible that the plates attract toward each other before the pull-in voltage occurs [10]. Authors in [11] to increase the tuning range, have introduced a MEMS variable capacitor configuration with vertical comb actuator.

2.2. The quality factor

The quality factor is one of the key electrical aspects of a tunable capacitor, which embodies the nature of the loss in a microwave circuit and is defined as a division of average energy stored in to the energy loss. Now it is equally important to understand how the materials of construction affect the Q of a tunable capacitor. A tunable capacitor can be modeled as a series model (Fig. 3) that the impedance of the discrete tunable capacitor can be calculated according to the following equation;

$$Z = R_{\text{series}} + j(\omega \text{L}_{\text{series}} - \frac{1}{\omega C_D}) \quad (6)$$

In which the quality factor of the capacitor is given by

$$Q = \frac{|\,\text{Im}(Z)\,|}{\text{Re}(Z)} = \frac{1}{\omega C_D R_{\text{series}}} \quad (7)$$

In general, the quality factor is determined by the series resistance of the suspension beams (R_{series}). The suspension beams must be made long to attain stiffness values low enough to insure sufficiently low actuation voltages that is also increases the series resistance and decreases the quality factor of a tunable capacitor ($Q \propto 1/R_{series}$).

Wider or shorter suspensions could be minimized this effect and maximized the Q that will probably trade off with the need for higher actuation voltages. Therefore one way to increase the quality factor of tunable capacitor is eliminate the need to exist the suspension beams for the tunable capacitors or using movable dielectric between the capacitor plates [12-14].

And much better Q-factor is achieved by the elimination of suspension beams in the RF signal pathway (i.e. RF signal does not pass through the springs) and hence, allows the higher quality factor from the conventional tunable capacitor [15].

As a earlier discussed, the MUMPs process contains three layers of polysilicon and one metal layer. The quality factor of MEMS tunable capacitors were fabricated using the PolyMUMPs process were limited by the absence of a second metal layer. And the polysilicon plates of the capacitor result a relatively high series resistance. Also the low conductivity of the polysilicon aggravates the skin-effect, which results further loss of power and Q is decreased. Implementing these tunable capacitors in a technology offering more than one metal layer such as CMOS technology, can improve the quality factor. Currently, several MEMS capacitors have been fabricated in CMOS technology [8, 9 and 16]. These MEMS tunable capacitors exhibit high quality factor by using metal interconnect layers of CMOS process as the main material for the electrodes, keeping the series resistance low.

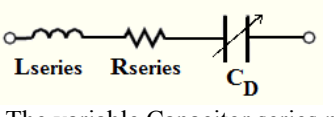


Fig. 3. The variable Capacitor series model

3. CMOS PROCESS

The complementary MOS (CMOS) devices that are consist of both n-type and p-type transistors were introduced in middle of 1960 and become a universally accepted manufacturing process for integrated circuits. This technology involve more than 200 processing steps such as wafer processing to produce the substrate; photolithography to define each region; oxidation, deposition and ion implantation to add the desirable materials to the substrate and etching to remove materials from the substrate.

Photolithography is the first step that is involve of three steps: cover the wafer with photoresist; align the mask and expose to light; etch to remove exposed photoresist. Oxidation step is used to produce the thick layer of sio_2. The silicon dioxide can act as a protective coating in another steps of fabrication. Also, the device fabrication requires the deposition of various materials, such as chemical vapor deposition (CVD) which in this method, wafers are placed in a furnace filled with a gas that produces the desired material through a chemical

reaction. And while the dopants must be selectively introduced into the wafer, ion implantation will be used. And to remove the materials from the substrate, there are two types of etching; wet etching (placing wafer in a chemical liquid); dry etching such as plasma etching (bombarding the wafer with a plasma gas) or reactive ion etching (RIE), that ions produced in a gas bombard the wafer [17].

Using CMOS technology it is possible to produce the MEMS variable capacitors with high quality factor. Reliable, fast, repeatable and cheap are some of the numerous advantages of CMOS technology, moreover using this technology can push the MEMS technology to higher integration.

4. DESIGN OF THREE-PLATE MEMS VARIABLE CAPACITOR

In this paper, to increase the both of tuning range and quality factor of conventional two parallel plate capacitor, a new three-plate capacitor using the 0.18μm CMOS technology is proposed that the theoretical limit for the running ratio would be increased from 50 to 300 percent. The fabrication and design issues are discussed and the simulation results are presented. As shown in Figure. 4 in the three-plate MEMS variable capacitor, under zero bias condition the distances between parallel plates are d_1 and d_2, respectively. The bottom plate of the capacitor is fixed and Both top and middle plates of the capacitor move toward each other according to bias voltages.

The top and middle plates are suspended by two springs with a spring constant k / 2 each. If a bias voltage $V_1(t) = V_1$ is applied and $V_2(t) = 0V$, the electrostatic force causes the suspended plates to move toward each other and the capacitance is increased. Similarly, if a bias voltage $V_2(t) = V_2$ is applied and $V_1(t) = 0V$, the middle plate moves toward the bottom plate and the capacitance is decreased. Under direct contact conditions, $x(t) = x$, $V_1(t) = V_1$, $V_2(t) = V_2$, and the equilibrium between the electrostatic and spring forces can be expressed as a following equation;

$$kx = \frac{1}{2}\frac{dC_D}{dx}V_1^2 + \frac{1}{2}\frac{dC_P}{dx}V_2^2 \quad (8)$$

And with replacing the capacitance in the following equation, the equilibrium can be written as:

$$kx = -\frac{1}{2}\frac{\varepsilon_d A V_1^2}{(d_1 + x)^2} + \frac{1}{2}\frac{\varepsilon_d A V_2^2}{(d_2 - x)^2} \quad (9)$$

Due to the oxide layers, the equivalent dielectric constant ($\varepsilon_{air} = 1.00054$, $\varepsilon_{IMDa} = 3.7$ and $\varepsilon_{IMDb} = 4.2$) at each subarea can be calculated. If distances d_1 and d_2 are equal, the maximum capacitance that this capacitor can be tuned to is $3C_D$ that is two times higher than the original value. However, the minimum capacitance that this capacitor can be tuned to is $3C_D$ / 4 that is smaller than the original value. Hence the maximum theoretical tuning range is 300 percent which is higher than that of a conventional parallel-plate capacitor.

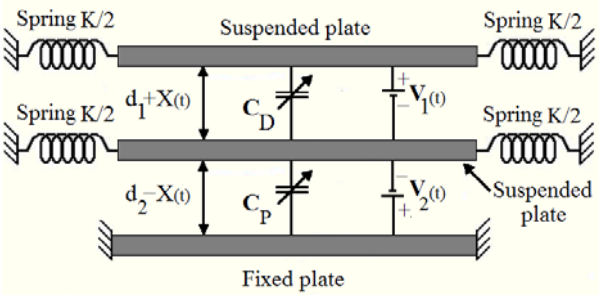


Fig. 4. A three-plate MEMS tunable capacitor with two movable plates

For this design, the middle plate of the tunable capacitor must be connected to a small-signal ground in a practical circuit application so that only the desired capacitance C_D plays a role in the actual circuit. To increase the quality factor, the proposed MEMS variable capacitor is designed by using metal interconnect layers of 0.18 μ*m* CMOS technology. The three plates of capacitor consists of metal #5, metal #3 and metal #1 layers, respectively. The total distance between the middle and top and bottom plates is typically 2.23 μ*m*, including two 0.35 μ*m* of oxide layers on both plates and 1.53 μ*m* air gap between each both plates. The capacitor's dimensions are: $d_1 = d_2 =$ 2.23 μ*m*, A = 400×400 μm^2. High Q value (about 300 in 1GHz) is achieved by using metal as the main material for the electrodes, keeping the series resistance low.

5. FABRICATION PROCESS

In this article, a CMOS-MEMS post-processing technique is proposed to release the MEMS three-plate capacitor that is the same as the technique previously was reported by the authors in [8, 10, 11, 16 and 18].

The CMOS-MEMS post-processing of tunable capacitors starts with a chip fabricated using the TSMC 0.18μm CMOS technology. There are six AlCu metal layers available through this process. The top, middle and bottom plates are made of M5, M3 and M1 layers, respectively and the other metal layers (M2 and M4) are used as sacrificial layers which will be removed after post-processing in order to create two air gaps between the plates. And a trench in the silicon substrate is used to decrease the parasitic capacitance and improve the quality factor of the MEMS capacitors. The chip in 0.18 μm standard CMOS process is presented in Fig. 5.

Three maskless post-processing steps are required to manufacture the integrated three-plate MEMS variable capacitor. As shown in Fig. 5(b) the first processing

stage involves the removal of silicon dioxide around the MEMS structure. This can be done using the last metal layer (M6) as a mask to protect the other parts of the CMOS chip and reactive ion etching (RIE) of the oxide layer [1], [7].

The main purposes of this step are exposing the sacrificial M2 and M4 layers that will be etched during the next post-processing step and creating windows through the oxide down to the silicon substrate, which are used to form a trench under the capacitors improving their quality factor. It is important to keep an oxide layer around the structural metal layers (M1, M3 and M5) to protect them during the removal of the sacrificial layers by the wet etchants. This is accomplished by extending the masking metal layer (M6) on top of the structural layers by 2 μm, an extension sufficient. However, the M4 and M2 metal layers respectively, which are required to be exposed after the RIE step, should be extended further than M6 and M4 by 5 μm, an extension sufficient. As shown in Fig. 5(c) the second post-processing step involves the etching of the sacrificial layers and substrate using wet etching techniques which is conducted by a phosphoricacetic-nitric (PAN) acids etch [8]. The second RIE is required to remove the protecting oxide layer on top of the capacitor's top plate for electrical connection (Fig. 5(d)). After this three steps, the middle and bottom plates consist of three layers (oxide–AlCu metal–oxide) and top plate consists of two layers (AlCu metal–oxide).

6. SIMULATION RESULTS

The EM3DS software from MEM Research is used to simulate the three-plate MEMS variable capacitor. As shown in Fig. 6. the scattering parameters (S_{11}, S_{12}) are extracted from the EM simulation and presented on the Smith chart in the frequency range from 1 GHz to 5 GHz. And the capacitance can be calculated by using the Y parameters;

$$C_D = -\frac{\mathrm{Im}(y_{12})}{2\pi f} \qquad (10)$$

The capacitance of the varactor varies from 1 to 4 pF, corresponding to change of 300 percent. Figure 7 shows, respectively, the EM simulated quality factor of the three-plate MEMS variable capacitor that is about 300 in 1GHz, which is sufficient for almost every communication application. The C-V responses of the tunable capacitor with two movable parallel plates is presented in Fig. 8.

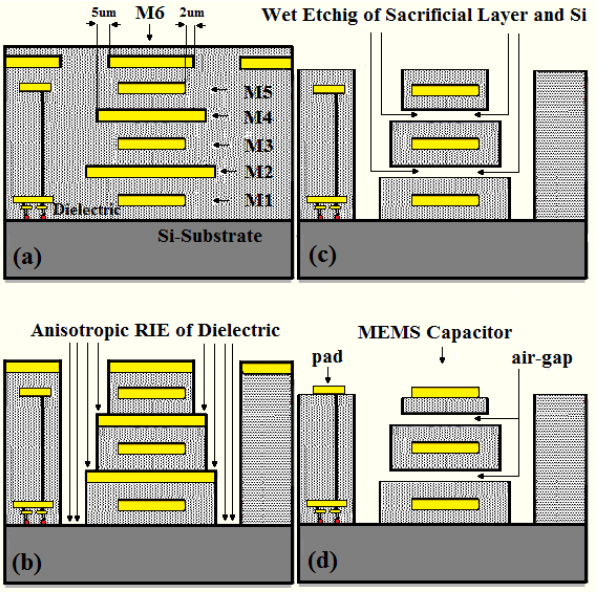


Fig. 5. The CMOS-MEMS post-processing steps, (a) RIE oxide removal, (b) wet etching and CPD, and (c) RIE

Under zero bias conditions ($V1 = 0V$ and $V2 = 0V$), the measured capacitance (C_D) is 1.33 pF. As the actuation voltage is increased ($V1 = 1.36V$ and $V2 = 0V$), the top and middle plates moves toward each other and the measured capacitance is approximately 4 pF. When $V1 = 0V$ and $V2 = 1.36V$ are set, the middle plate moves toward the bottom plate and the measured capacitance is 1pF. Thus the proposed capacitor exhibited measured tuning range of 300% which is in good agreement with the theoretical calculations. Table 1 summarizes the characteristics of simulated three-plate MEMS variable capacitor with Comparison of the conventional two parallel plates capacitor, including their simulated tuning range and quality factor when the polysilicon or metal layers are used as the material for the electrodes.

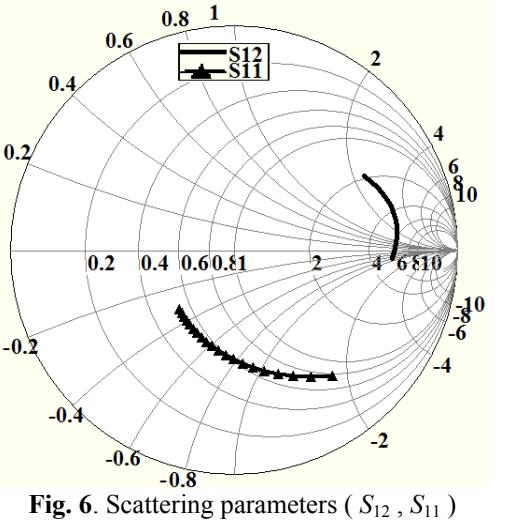


Fig. 6. Scattering parameters (S_{12} , S_{11})

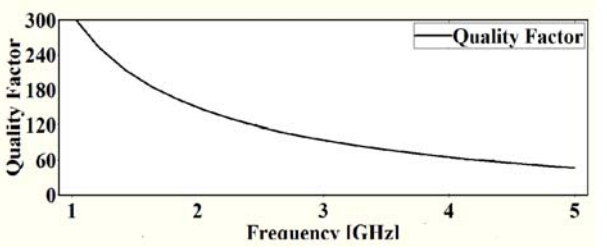


Fig. 7. The quality Factor

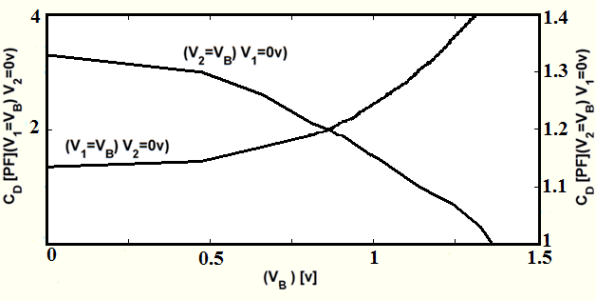


Fig. 8. The C-V responses of the three-plate variable capacitor

7. CONCLUSION

The RF-MEMS varactors fabricated in the PolyMUMPs foundry have been reported and the capacitance variation and Q limitations for devices fabricated in this foundry have been identified. A new three-plate MEMS variable capacitor has been designed and electromagnetically simulated with performance exhibiting very wide tuning ranges (300 percent) and high quality factor (Q = 300) values at 1 GHz. The proposed capacitor is designed by using metal as the main material for the electrodes, keeping the series resistance low. Thus the high *Q* value is achieved.

Table1. The Comparison results for simulated three-plate MEMS tunable capacitor with the conventional two plates capacitor.

configuration	conventional two-parallel plate capacitor	Two movable plates capacitor
Area	400×400 μm2	400×400 μm2
Air gap	d1=0.75 μm	d1= d2=2.23 μm
Tuning range	50%	300%
Quality factor	147	300
Electrode Layers	polysilicon	ALCU metal

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