Electromagnetic Compatibility Requirements of Printed Circuit Boards Design

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ABSTRACT:
The design and layout of a printed circuit board is crucial to the functionality and electromagnetic compatibility (EMC) performance of the product. The proper layout in printed circuit boards must satisfy EMC requirements in board level and system level. Some of these requirements is about placement of components, board partitioning, trace routing and return path continuity. Designers must have strict control on these mentioned requirements. In this paper we study these cases and present their relevant design notes. Also we provide design points about electromagnetic compatibility requirements of the power and supply system, shielding, digital and analog circuits on printed circuit boards. They are all must be considered to meet emission and susceptibility requirements of the PCB.

KEYWORDS: Electromagnetic Compatibility, Printed Circuits Boards, Partitioning, Shielding, Layout.

1. INTRODUCTION

Circuits technology has progressed rapidly and design techniques that already exist from several years ago have no capability in modern high speed systems now. On the other hand electromagnetic compatibility issues are fewer academic courses and are limited to articles. Accordingly, it is necessary that these important issues which have a critical role in functioning properly of complex systems to be developed nowadays. The used method of designing PCB causes differences in electromagnetic compatibility performance of the system. The board design techniques help us according to requirements of electromagnetic compatibility so that electromagnetic emission from circuits and components is minimized. In these methods, both of emission and susceptibility aspects will be important. Electromagnetic emission is defined as electromagnetic interference propagation from incompatible components; also, radio frequency radiative and conductive emissions are more important than others. Electromagnetic susceptibility, in addition, means effects of electromagnetic interferences on the components [1, 2].

It has lower cost if interferences on the board could be attenuated in comparison with designing a shield. Furthermore, installation of the shield may have harmful effects on function of the circuits. In accordance with importance of mentioned issues in this paper, basic requirements and techniques used for designing boards Will be discussed. If application and performance of designs are different, the basic fundamentals of designs change rarely. The necessary requirements for each of the applications are represented in this report.

2. PCB DESIGN REQUIREMENTS AND TECHNIQUES

The following part represents the requirements for each step of PCB design, which has no problem in viewpoint of electromagnetic compatibility.

2.1. Board Partitioning

Components placement is important, however ignored, aspect of board layout that can have a significant impact on the board's EMC performance. The components have to be divided into several groups. Some of these groups are: 1) high speed logics, 2) memories, 3) logic circuits with low and medium speed, 4) high speed circuits, 5) low frequency and audio circuits, 6) input and output drivers, 7) input and output connectors, and common mode filters as depicted in Figure. 1 [1, 3].

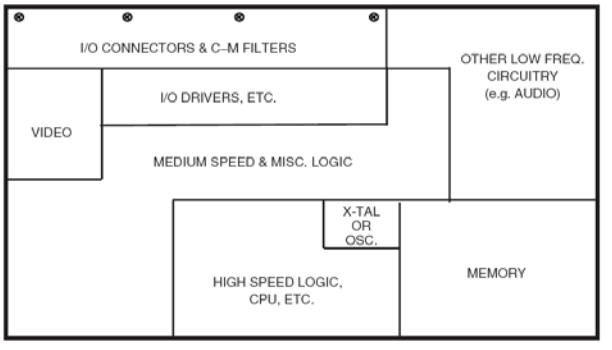

Fig. 1. A proper board partitioning

Partitioning design can be divided into two main sections:

Physical partitioning associated with components placemat, their orientation and shielding.

Electrical partitioning which the circuits with regard to their electrical performance are placed in same part. First the components related to RF directly, should be placed in spaces which the length of RF paths is minimum for physical partitioning. Furthermore, input and output should be far from each other, and low power circuit must be far from the high power circuits as far it is possible [4].

In the good partitioned circuit, high-speed circuits and memories are not placed in the proximity of I/O parts. Crystal and high frequency oscillator must be close to the circuits using them and away from the I/O parts. The I/O drivers must be close to the connectors; high and low frequency analog circuits should have access to the I/O parts without crossing the high frequency digital circuit part [4].

Placing of blocks with respect to frequency behavior of the components is important. High frequency blocks have to close the I/O ports for the purpose that inductive losses might be avoided due to long paths. In Figure. 1, one PCB with basic placing plan is depicted. The following issues should be considered when the designers want to placing components [1, 4-6]:

1) RF high power amplifiers must be away from low noise amplifiers as far as possible. RF buffers and VCOs are considered as high power parts.
2) Designer must place minimum a fully ground sheet at least.
3) The most of RF integrated circuits are sensitive to power supply noise. So decupling of supply and ICs are important. Here, capacitors are placed with regards to their capacity; that is, the smaller capacitance the closer to the IC pins.
4) It is recommended that RF outputs should be far from RF outputs.
5) Analog sensitive signals have to be placed far from high speed digital and RF signals.

The most effective and best method of stacking up is to place the main ground sheet immediately after the surface layer; also RF paths should be placed on the surface layer. Minimizing number of used vias in the RF path results in minimizing the inductance and unwanted RF coupling which can be couple on the other parts of the circuit. Good partitioning minimizes the length of paths and parasitic couplings; furthermore, it can be improving signal quality; it decreases emission and susceptibility of the board [4-6].

It is worth to mention those oscillators, crystals and each kind of high frequency circuit must be away the I/O ports. These circuits can generate electromagnetic fields so that these fields can couple on the I/O ports, connectors and other parts of circuit easily and directly (Figure. 2). Based on the experience, if size of the board does not provide any problem, placing the mentioned components at the minimum distance of 0.5 in (13 mm) from the I/O ports, can minimize the effect of parasitic couplings [1].

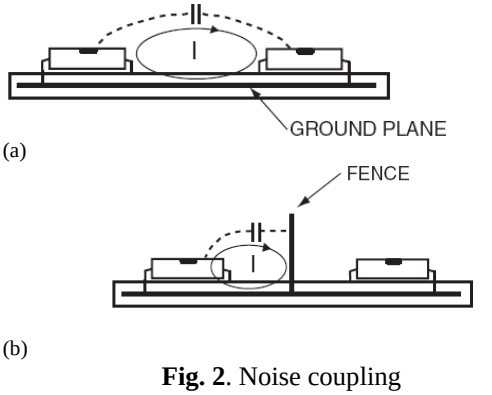

Fig. 2. Noise coupling

All of the vital signals have to be far from the edges of the board in the hope that return current can be spread under the path. As a thumb of nail, it is better to define the forbidden region that is from the edge of circuit to 20 times of board thickness around the periphery of the circuit. The vital signals must no cross these forbid regions (Figure. 3) [7].

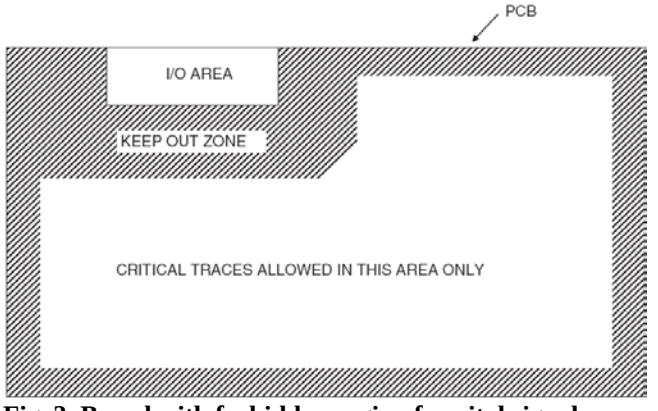

Fig. 3. Board with forbidden region for vital signals

2.2. Systems Clock Pulses

Clock pulses and high frequency signal paths should be short as possible. Also, routing of them must be performed firstly. Crystals, oscillators and resonators have to be near as possible to the circuits using them. A ground sheet is placed under the used crystals, oscillators and pulse driver. This ground must be connected to the main ground through several vias. This is a termination for fringing capacitors due to crystals and oscillators. Thus, this work blocks routing of other signals on the upper layer and under the crystal. If crystal or oscillator has metal body, this body has to be connected to the ground at the component layer; and a shield space has to be assigned on the board for it. A low value of series damping resistor or ferrite beads must be connected to output of clock pulses paths that work with frequency more than 20 MHz [8-11].

2.3. Connection of Ground to the Chassis

A major source of radiation due to electronic systems is common mode electric currents on the cables placed out of the board. From antenna perspective, a cable can be considered as a monopole antenna. Voltage which drives the antenna is the common mode voltage between cable and chassis; as a result, reference of cable radiation is chassis [1].

Ground of inner circuit must be terminated at the nearest point that cable terminated on the board, to the chassis. It is essential to minimize voltage difference between them; this connection at RF must have low impedance. Each impedance between the ground and chassis generates voltage drop; hence, cables are excited by common mode voltage and radiates [12].

Often, connection of the ground to the chassis is implemented by inappropriate metal tools at incorrect places; therefore, it can have considerable high frequency impedance. This connection rarely is optimized for the EMC approach. Designing of this connection is important for the product EMC performance. It should be short and have several paths for the purpose that parallel inductances decrease RF impedance. The Figure. 4 depict an example of connection of circuit ground to the chassis at places near I/O. It points out advantage of placing all of I/Os at one area [1, 12].

If metal layer connectors are used, they must be connected to structure with direct electrical connection of 360 degrees (through EMC gaskets). These connectors can be part of low impedance connection of reference ground plane to the structure. This is illustrated in Figure. 4 [1].

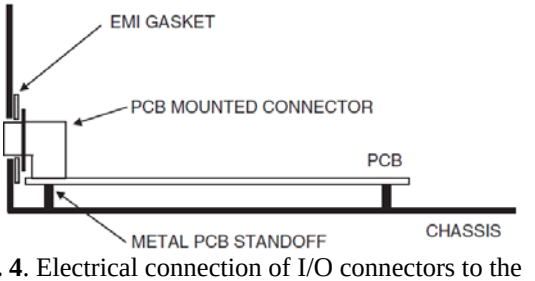

Fig. 4. Electrical connection of I/O connectors to the chassis.

2.4. Necessity of Continuity of Return Signal Path

One of the important key points in optimum determining of board layout is to know feasibly how and where the return currents pass. Major problem of EMC and signal integrity, happens when a discontinuity is occurred at the return path. Discontinuities cause return current flows in large loop, then path inductance and radiation from board increase. Crosstalk between the near paths is increased, also it distorts waves. In addition, discontinuity of the return plane on the board with constant impedance, changes characteristic impedance and results in reflections. Three common return path discontinuities that should be considered by designer are as following [4-6, 13]:

- Slot on the ground or power plane
- Layer change at signal path which causes return currents change the reference planes.
- Fuse of ground plane near connectors or under ICs.

A ground or power plane containing return currents must not have slotted as depicted in Figure. 5. According with this simple law, a lot of EMC problems do not occur. If slot placing is inevitable, slots at close layers must not cut paths. The slot on the ground plane increases the radiation more than 20 dB [12].

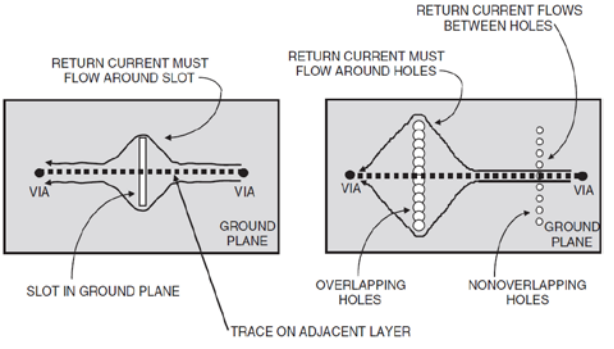

Fig. 5. Slots and holes in ground plane

Figure. 6. Represents simulation of a transmission line with ground plane in three different situations. These situations are a common transmission line with integrated ground plane, ground plane with aligned slot and ground with vertical slot. In accordance with the presence of slots, performance of transmission line is perturbed. Also more than perturbation in transmission line performance, part of energy is radiates due to the slots which can be coupled on the other components and causes EMI.

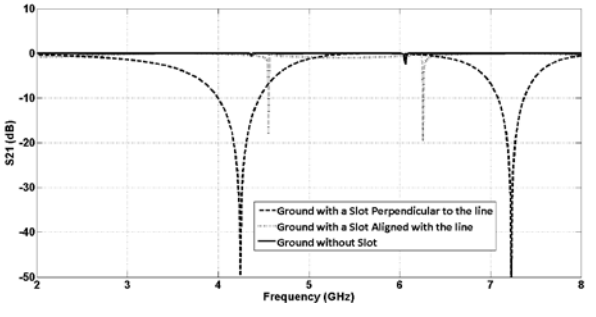

Fig. 6. Transmission line performance at the presence of slot in its ground plane

Most of the modern systems demand several levels of DC voltage to function properly. As a result, separating supply planes is a common situation. It is worth to note that to avoid crossing of paths on the slots, routing constraints have to be applied on separated planes. The methods of overcoming problems due to separating power supplies are providing supply with different planes, Power Island, supply lines and using junction capacitors among these planes. Each of these methods has advantages and disadvantages. When a DC voltage is applicable for one or several ICs which placed near each other, using the method of power islands is more useful.

Another place that is possible to have discontinuity for current path is around the connectors. As depicted in Figure. 7 (a), when the copper is removed from the ground under the connector, the current has to pass around the discontinuity; thus, these causes a huge loop and generates noisy place on the board. The bigger the connectors are, the larger problem occurs. To overcome this kind of problems, only the copper layer around of each connector must be removed according to Figure. 7 (b). Current loop will be small by doing that.

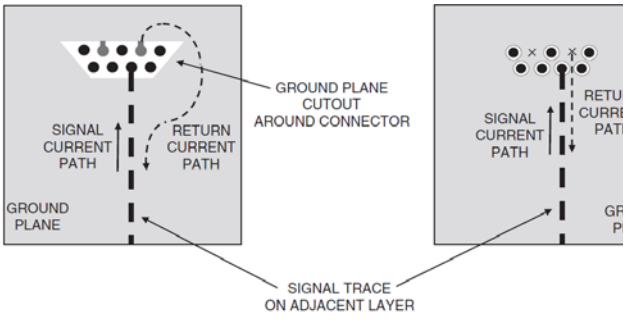

Fig. 7. An area around boards' connectors (a) all of the copper around connectors is removed and (b) smaller copper area around the connectors is removed.

2.5. Grounds Fill

Grounds fill or ground pour is a technique that copper is placed on the areas of board on which there is no any path or strip. The aim is that the emission and susceptibility can be decreased by cutting fringing fields from signal strips and providing some degree of shielding on the board. To do it, ground fill must be connected to the ground structure at a lot of points. If this connection does not apply correctly, this kind of ground can cause increment of emission, susceptibility and crosstalk among lines. Small ground fill area and narrow area are problematic; as a result, they must be avoided. Filled copper that is not grounded properly can generate electrostatic discharge. Thus, the copper area must not be remained ungrounded. Grounded filled copper is not suggested for high speed digital circuits, for it can cause impedance discontinuity and distorts circuit function [1].

2.6. Requirements Related to Digital Circuits on the Board

Clock paths are the first section that must be routed. They have to be on one PCB layer and close to the ground sheet. All of the clock address and data bus connections should be straight and short as it is possible. Also they should be near of ground sheet or guard ground strips. Wires, stubs and ribbon cable cannot be used to distribute clock. In addition to previous requirements, high speed digital signals such as data, address and control line of microprocessors must be grouped and placed away from the I/O connectors. Signal path and its ground return path should be close to each other for the purpose that loop area surrounded by current loop is minimized. Strips and paths except ground are never being routed close or under crystals

and noisy circuits. The required maximum rise and fall time and minimum frequency of clock which satisfy the requirements, always must be considered. All of critical circuit networks such as clock and data must be routed near the ground paths or ground sheet.

Placing RF filters aligned with diodes, transistors and ICs can avoid from conversion of RF to DC or low frequency interference signals.

At long buses, strips related to high speed and low speed signals should be away from each other by adding distance between them. High frequency signals also are near of ground path. Differential signal paths should be close to each other, so we can use advantage of magnetic field elimination completely. Ground guard paths are placed in two side of total differential signal length. To minimize crosstalk, signal paths placed near layers of PCB must be orthogonal to each other. Controlling of rise and fall time, duty cycles and fundamental frequency of switched signals result in minimizing of harmonic generation. Furthermore, all of unused pins of ICs must be terminated because of the fact that it can avoid unwanted random switching and noise generation [14-16].

2.7. Requirements Related to Analog Circuits on the Board

Analog circuits, as it is possible, must be placed near I/O connectors and away from high speed digital circuits, high current circuits and circuits with switching power supply.

Routing of analog signals with low level must be limited only at one section of PCB. Low pass filters must be used for all of analog inputs. PCB strips terminated to connectors must be decoupled from RF strips. Ground guard paths have to be routed near analog signals; in addition, these paths at their ends must be connected to ground through vias. Paths transferring high currents, as it is possible, must be wide in the hope that voltage drop is minimized. Several vias should be used for changing layer of these signals to have low level of loss [1].

2.8. Shielding on the Board

It cannot be possible sometimes to create required isolation among circuit blocks. One metallic shield in these cases should be used to limit RF energy at generator section. All of the system metallic shield must be connected to each other and grounded. Each shield has at least two points, connections with ground to avoid noise coupling to systems placed inside the shield. If the shield is not grounded, it has variable potential based on its place and time conditions; thus, coupled noise into the systems is variable. Placing shield on bunch of wires can limit radio frequency emission. To reduce crosstalk and susceptibility among high impedance lines in bunch of wires, individual shields must be used owing to the fact that in general, shielding is the most efficient and cheapest way to attenuate electromagnetic interferences. To have effective shield, it must surround electronic systems completely and have not any hole such as cavity, slot or other cable connection. Each hole which is not considered correctly on shield can reduce shield effectiveness dramatically. Placing a metallic enclosure as a shield on components is necessary on the following cases [17, 18]:

- Circuits are very close to each other; as a result, noise coupling can occur.
- Electromagnetic interference is intensive and cannot be limited.
- Circuits are very sensitive; hence, performance of circuits is affected by existing electromagnetic interferences.

Using the shield can cause some problems such as occupying of limited and valuable space on the board, having high cost and being hard to fix and troubleshoot. Solution of these problems is to use discrete connection at each $\lambda/20$ other than continuous connection to ground (Figure. 8). A shield causes some problems; however, they are effective way to isolate critical circuits, and sometimes they are only solution to mentioned problems. Outside paths placed outside of shielded regions should be shielded in interior layers. When routing must be done from shielded region at same shielded layer, the smallest gap is used to do it. To shield cables existed main shield, 360 degree connection to metallic enclosure must be used. Also, placing other holes except mentioned holes must be avoided [6, 17, and 18].

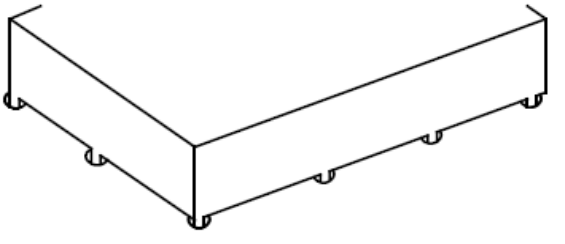

Fig. 8. Discrete connection of shield at each $\lambda/20$

CONCLUSION

In this paper, ways of board design to improve EMC are introduced. These solutions include overall titles such as: board partitioning, layout, strips routing, return path continuity, regions isolation, requirements related to analog and digital circuits and shielding. At each of these titles, required requirements by considering aim of project and accessible components are examined.

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