Design and Simulation of High Tuning Range and High Quality Factor MEMS Variable Capacitor in Standard CMOS Technology

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ABSTRACT:
This article is organized to represent the work specifications of micro electro mechanical gap-tuning capacitors and to increase the both of tuning range and quality factor, a three-plate capacitor which can be fabricated in standard 0.18 μm CMOS technology is designed and simulated. The simulation of the capacitor was done using the EM3DS software and the simulation results show tuning range of 100%, that is 2 times higher than tuning range of the conventional parallel plate capacitor. The plates of this capacitor are designed by using the available metal layers in the TSMC 0.18 μm CMOS technology that have caused decreasing the series resistance and increasing the quality factor to 300 in 1 GHZ.

KEYWORDS: Three-parallel plate MEMS variable capacitor, Electro mechanical gap-tuning capacitors.

1. INTRODUCTION

Microelectromechanical Systems (MEMS) have developed recently but the development of MEMS variable capacitors has not progressed at the pace of MEMS switches. Because there are plenty of discrete high quality factor silicon and GaAs variable capacitors up to 30 GHz. Moreover the low tuning range of this variable capacitors (1.2–2.5) is another reason for this limited development, while standard solid-state variable capacitors have a highly tuning range (4–6) [1].

In recent years, the MEMS variable capacitor are widely developed. The capacitance of MEMS variable capacitors can be tuned by the gap tuning [2], area tuning [3] and dielectric tuning [4]. The conventional gap tuning tunable capacitors are made up of two parallel plates. The top plate of the capacitor is suspended by a spring while the bottom plate is fixed mechanically. The suspended plate can be moved to the bottom plate by using the electrostatic force or electrothermal [5] and piezoelectric actuation mechanism[6]. The electrostatic actuation is mostly used over the other actuation mechanisms because this actuation mechanism has low power consumption. During the past two decades, several new fabrication techniques have been employed which are widely used for micro electro mechanical systems (MEMS) fabrication, such as Bulk micromachining, surface micromachining, and LIGA. However micromachined devices fabricated by standard IC technology such as complementary metal–oxide–semiconductor (CMOS) processes are attractive, because there are many advantages to leveraging conventional CMOS processing for MEMS. CMOS technology has proven itself over the years to be a universally accepted manufacturing process for integrated circuits, driven primarily by the tremendous demand for computers and digital electronics. This process Fabrication is fast, reliable, repeatable and cheap, moreover using this technology, it is possible to integrate high-performance onchip signal conditioning circuits with digital readouts, expected multivendor accessibility and short design cycle times. Currently, several MEMS capacitors have been reported in CMOS technology. In this paper, a new three-plate capacitor using the 0.18μm CMOS technology is proposed. The fabrication and design issues are discussed and the simulation results are presented.

2. CAPACITOR DESIGNING

Traditional electro-mechanically tunable capacitors are made up of two parallel plates. Fig. 1 shows a simplified model of the gap-tuning MEMS capacitor. The top plate of the capacitor is suspended by a spring with spring constant, *k*, while the bottom plate is fixed mechanically. When a bias voltage $V_1(t)$ is applied across the capacitor plates, the suspended plate is attracted to the bottom plate due to the resulting electrostatic force and thus increases the capacitance of the structure. The suspended plate moves toward the fixed bottom plate until an equilibrium between the electrostatic and the spring forces is reached. The equilibrium between the forces can be written mathematically as follows [7], which under steady state conditions, $x(t) = x$ and $V_1(t) = V_1$.

$$E = \frac{1}{2}\frac{\varepsilon_d A V_1^2}{(d_1 + x)} \quad (1)$$

Where ε_d is the permittivity of air ($\varepsilon_d = \varepsilon_{air}\varepsilon_0$ where $\varepsilon_{air} = 1.00054$ and $\varepsilon_0 = 8.85415 \times 10^{-12}$ F/m), A is the area of the capacitor plates, and d_1 is the separation of the capacitor plates when the spring is in its relaxed state. By neglecting the fringing effect, the capacitance of the capacitor, which has been formed between the two plates, can be written as:

$$C_D(V_1) = \frac{\varepsilon_d A}{d_1 + x(V_1)} \quad (2)$$

And the spring constant for a beam is given by the following equation:

$$k = \frac{3E_y I}{l^3} \quad (3)$$

Where E is the Young's module, l is the beam's length and I is the moment of inertia for the beam, which could be calculated According to the following equation;

$$I = \frac{\mathrm{w}t^3}{3} \quad (4)$$

In which w is the beam width and t stands for its thickness.

The capacitance tuning range of a gap-tuning capacitor is limited by pull-in instability that is equilibrium between the spring and the electrostatic forces exists only for displacements less than $d_1/3$.

The maximum capacitance that such a tunable capacitor can be tuned to is $3C_D / 2$ and therefore, theoretically, the maximum tuning range of a gap tuning capacitor is 50 percent.

In order to increase the tuning range, a three-plate capacitor is proposed that the theoretical limit for the running ratio would be increased from 50 to 100 percent. As a shown in Figure. 2 in the three-plate electromechanically tunable capacitor, under zero bias condition the distances between parallel plates are d_1 and d_2 , respectively. Both top and bottom plates of the capacitor are fixed and the middle plate moves toward the bottom and top fixed plates according to bias voltages.

The middle plate is suspended by two springs with a spring constant $k / 2$ each. If a bias voltage $V_1(t) = V_1$ is applied and $V_2(t) = 0V$, the electrostatic force causes the suspended plate to move toward the top plate. Similarly, if a bias voltage $V_2(t) = V_2$ is applied and $V_1(t) = 0V$, the suspended plate moves toward the bottom plate. Under directcontact conditions, $x(t) = x$, $V_1(t) = V_1$, $V_2(t) = V_2$, and the equilibrium between the electrostatic and spring forces can be expressed as;

$$kx = \frac{1}{2}\frac{dC_D}{dx}V_1^2 + \frac{1}{2}\frac{dC_P}{dx}V_2^2 \quad (5)$$

And with replacing the capacitance in the following equation the equilibrium can be written as:

$$kx = -\frac{1}{2}\frac{\varepsilon_d A V_1^2}{(d_1 + x)^2} + \frac{1}{2}\frac{\varepsilon_d A V_2^2}{(d_2 - x)^2} \quad (6)$$

Due to the oxide layers, the equivalent dielectric constant ($\varepsilon_{air} = 1.00054$, $\varepsilon_{IMDa} = 3.7$ and $\varepsilon_{IMDb} = 4.2$) at each subarea is used to obtain the simulated capacitance. If distances d_1 and d_2 are equal, the maximum capacitance that this capacitor can be tuned to is still $3C_D / 2$. However, the minimum capacitance

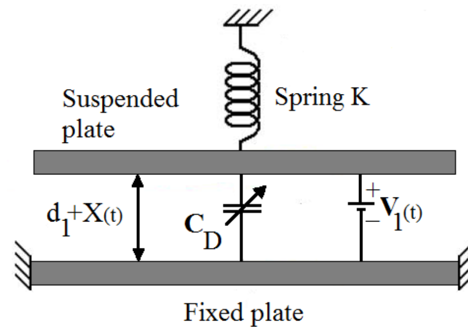

Fig. 1. A simplified model of a two parallel- plate capacitor

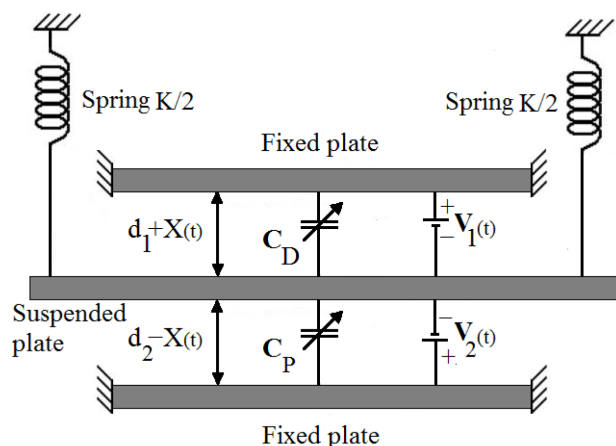

Fig. 2. A simplified model of a three-plate tunable capacitor

that this capacitor can be tuned to is $3C_D / 4$ (which means the capacitance can be tuned smaller than the original value). Hence the maximum theoretical tuning range is 100 percent which is higher than that of a conventional parallel-plate capacitor. For this design, the middle plate of the tunable capacitor must be connected to a small-signal ground in a practical circuit application so that only the desired capacitance C_D plays a role in the actual circuit. The proposed MEMS variable capacitor is designed for fabrication in 0.18 μm CMOS technology. The capacitor is designed by using metal interconnect layers. The top, middle and bottom plates of the three-plate capacitor consists of metal #5, metal #3 and metal #1 layers, respectively. The total distance between the middle and top and bottom plates is typically 2.23 μm, including 0.85 μm of oxide on both plates and 0.53 μm air gap between each both plates.

The capacitor's dimensions are: A = 400×400 μm^2, d_1 = 2.23 μm and d_2 = 2.23 μm. The results of the extracted capacitances from electromagnetic simulations are in good agreement with the theoretical calculations. The proposed capacitor exhibited simulated Capacitances C_{max} = 2 pF when d_1 = 1.9μm and d_2 = 2.56 μm and C_{min} =1PF when d_1 = 2.56μm and d_2 = 1.9μm with tuning range of 100 %.

The design parameters such as d_1 and d_2 could be optimised for increasing the tunability of the capacitor, however the fabrication rules limit these variations. A tunable capacitor may be integrated in a circuit where different CMOS devices are fabricated on the same chip and it is not necessary to customize the process for each device.

3. QUALITY FACTOR

The quality factor is a measure of the loss of a microwave circuit and is defined as a division of average energy stored in to the energy loss. A discrete capacitor can be modeled as a series model (Fig. 3) that the impedance of the discrete capacitor can be calculated according to the following equation;

$$Z = R_{\text{series}} + j(\omega L_{\text{series}} - \frac{1}{\omega C_D}) \quad (7)$$

In which the capacitor quality factor, Q, is given by

$$Q = \frac{|\text{Im}(Z)|}{\text{Re}(Z)} = \frac{1}{\omega C_D R_{\text{series}}} \quad (8)$$

The Q is determined by the series resistance of the suspension beams (Rseries). Since $Q \propto$ 1/Rseries, the quality factor of a tunable capacitor is decreased by the series resistance of the suspension beams that must be made long to attain stiffness values low enough to insure sufficiently low actuation voltages. And the longer signal path resulting from this shape of the suspension beams also increases the series resistance losses. Wider or shorter suspensions could be used to minimize this effect and maximize the Q. This will probably trade off with the need for higher actuation voltages. One way to increase the quality factor of tunable capacitor is eliminate the need to exist the suspension beams for structures [17-19].

And another way to provide much better Q-factor is reducing series resistance by the elimination of suspension beams in the RF signal pathway (i.e. RF signal does not pass through the mechanical spring), and hence, allows the higher Q-factor from the conventional tunable-gap capacitor [20].

During the past decade, PolyMUMPs foundry is widely used for MEMS tunable capacitors fabrication. The MUMPs process contain three layers of polysilicon and one metal layer. The Q values for MEMS tunable capacitors fabricated using the PolyMUMPs foundry were limited by the absence of a second metal layer. And the plates of capacitor are made of polysilicon, which results in a relatively high series resistance. The low conductivity of the polysilicon also aggravates the skin-effect, resulting in further loss of power and Q is decreased. High Q values can be achieved by using metal as the main material for the electrode to minimize the ohmic and skin-effect loss mechanisms for the varactor, as presented by the authors in [21]. Implementing these varactors in a technology offering more than one metal layer such as CMOS technology, can improve the quality factor. Currently, several MEMS capacitors have been reported in CMOS technology [12, 13 and 22].

These MEMS capacitors exhibit very high quality factor by using metal interconnect layers of CMOS technology as the main material for the electrodes, keeping the series resistance low.

4. FABRICATION PROCESS

In this paper, a CMOS-MEMS post-processing technique is proposed to release the MEMS three-plate

capacitor that is the same as the technique previously presented by the authors in [12-16]. Three steps are required to manufacture the integrated three-plate MEMS variable capacitor:

1) Dry etching;
2) Wet etching;
3) The second dry etching;

There are six AlCu metal layers available in the TSMC 0.18 μm CMOS technology. The three-plate MEMS variable capacitor consist of three-parallel plate with two air-gap in between plates which are created by removing two of the interconnect metal layers (M4,

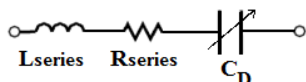

Fig. 3. The Capacitor series model

M2) within the CMOS chip. A trench in the silicon substrate underneath the capacitor is used to decrease the parasitic capacitance and improve the quality factor (*Q*) of the fabricated MEMS capacitors. Fig. 4(a) shows the chip in 0.18 μm standard CMOS process.

Three maskless post-processing steps are shown in Fig. 4(b), (c) and (d) to construct the three-plate tunable capacitors. The first processing stage involves the removal of the dielectric around the MEMS structure by anisotropic reactive ion etching (RIE) as presented in Fig. 4(b). In this stage last metal layer (M6) is used as a mask to protect the other parts of the CMOS chip and only the oxide layer is removed as presented in [1], [7]. The main purpose of this step is creating the open windows in the dielectric layer to expose the sacrificial M2 , M4 layers that will be etched during the next post-processing step. Since the wet etchants are not selective regarding Si and AlCu, it is critical to keep an oxide layer around the structural metal layers (metals #1, 3 and 5) to protect the AlCu metal layers from being etched by the wet etchants. This is accomplished by extending metal #6 over the top of the structural metal layers by 2 μm, an extension sufficient. Therefore, metal #4, which must be exposed after the RIE step, should be extended beyond metal #6 layer and metal #2 must be extended beyond metal #4 by 5 μm, an extension sufficient. Then wet etching is followed to remove the sacrificial metal layers (M2, M4) and the silicon substrate under the MEMS device as presented in Fig. 4(c). This stage is conducted by a phosphoricacetic-nitric (PAN) acids etch [12].

After wet etching, a critical-point-dryer (CPD) system are required to dry the chip. The second RIE is used to remove the dielectric layer on top of the capacitor's top plate for electrical connection. Fig. 4(d) shows the final post-processing step, that is the second RIE. After the post-processing technique and the release process, the bottom and middle plates consist of three layers (oxide–AlCu metal–oxide) and top plate consists of two layers (AlCu metal–oxide).

5. SIMULATION RESULTS

The EM3DS software from MEM Research is used to calculate the Scattering parameters associated with the three-plate MEMS variable capacitor. The straight result of the EM3DS software simulations is calculation of the current density profile in various layers of the structure. By using integral calculation from current density upon the area of each port, current port, is calculated.

And the current ports, are used to calculate the two terminals network parameters. The scattering parameters (S_{11}, S_{12}) are extracted from the EM simulation and presented on the Smith chart for $d_1 = 1.9\mu m$ and $d_2 = 2.56\ \mu m$. Fig. 5. represents these results in the frequency range from 1 GHz to 5 GHz.

Some elements such as capacitance between plates, capacitance leakage, the parasitic capacitance of the structure and the power dissipation at the input port can be calculated by Y parameters. The Y parameters can be calculated according to the following equation;

$$Y_i = I_i \mid V_k = \{^{1 \rightarrow if\ (k=j)}_{0 \rightarrow otherwise} \quad (10)$$

And the capacitance can be calculated by using the following equation;

$$C_D = -\frac{\mathrm{Im}(y_{12})}{2\pi f} \quad (11)$$

The quality factor of the three-plate MEMS variable capacitor have been calculated. Figure 6 shows, respectively, the EM simulated quality factor of the

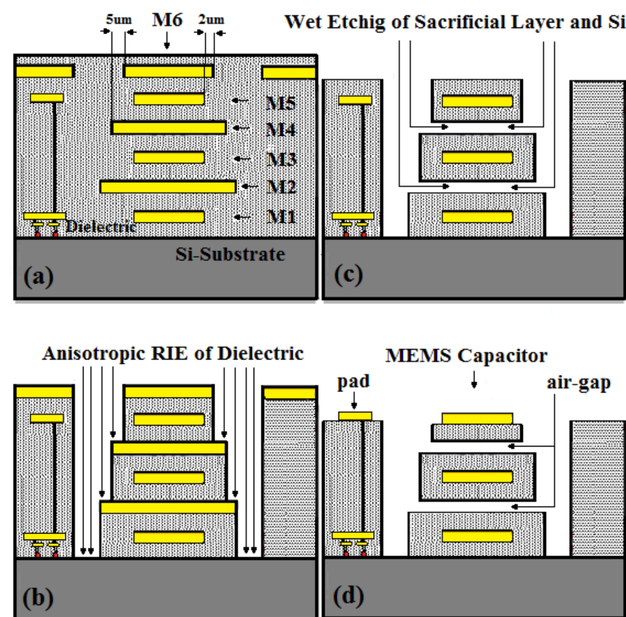

Fig. 4. CMOS-MEMS post-processing steps, (a) RIE oxide removal, (b) wet etching and CPD, and (c) second RIE

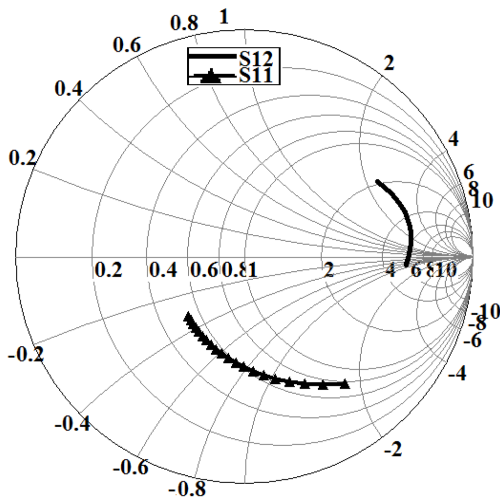

Fig. 5. Scattering parameters (S_{11} , S_{12})

structure with $d_1 = 1.9\mu m$ and $d_2 = 2.56\ \mu m$ between the three plates. The quality factor is about 300 in 1GHz, which is sufficient for almost every communication application. Figure 7 shows the C-V responses of the tunable capacitor with three parallel plates. Under zero bias conditions ($V_1 = 0V$ and $V_2 = 0V$), the measured capacitance (the desired capacitance C_D) is 1.33 pF. The measured capacitance is approximately 2 pF when $V_1 = 1.36V$ and $V_2 = 0V$ are applied. When $V_1 = 0V$ and $V_2 = 1.36V$ are set, the measured capacitance is 1pF. The proposed capacitor exhibited measured tuning range of 100 % and the measurement results are in good agreement with the theoretical calculations.

Finally the Comparison results for simulated three-plate MEMS variable capacitor with the conventional two parallel plates capacitor are summarized in the Table. I. The conventional two parallel plates capacitor is simulated by using polysilicon layers.

6. CONCLUSION

A new three-plate MEMS variable capacitor has been designed and electromagnetically simulated. This structure is compatible with standard CMOS technology thus is promising to be practical in system integration. The proposed capacitor exhibited simulated tuning range of 100 %, that is 2 times higher than tuning range of the conventional parallel plate capacitor. High Q value is achieved by using metal as the main material for the electrodes, keeping the series resistance low. These MEMS capacitors exhibit the high quality factor, that is 300 in 1GHz.

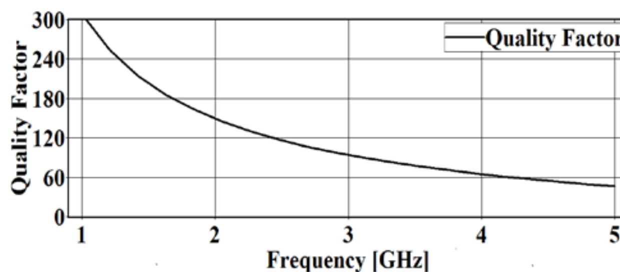

Fig. 6. Quality Factor

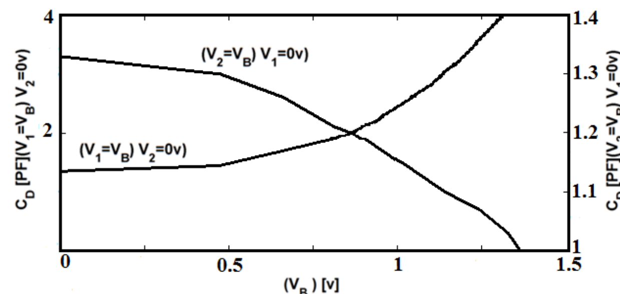

Fig. 7. The C-V responses of the three-plate tunable capacitor

Table1. The Comparison results for simulated three-plate MEMS variable capacitor with the conventional two parallel plates capacitor.

configuration	conventional two- plate capacitor	three-plate capacitor
Area	400×400 μm2	400×400 μm2
Air gap	d1=0.75 μm	d1= d2=2.23 μm
Tuning range	50%	100%
Quality factor	147	300
Layers	polysilicon	metal

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