Design of a novel hybrid-CMOS full adder with low power consumption, high speed and full swing outputs

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ABSTRACT:
In this paper a novel 1-bit full adder using hybrid-CMOS logic style is proposed. Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adder with desired performance. The new proposed full adder is based on differential cascode voltage switch logic (DCVSL) XOR-XNOR gate which generate full-swing outputs. The complementary pass-transistor logic (CPL) is used to have minimum propagation delay and stability against noise in *Sum* signal. Also the transmission-gate logic (TG) is used to have high speed and full-swing in C_{out} signal. The circuit that consists of 16 transistors is simulated with HSPICE in 0.18 μm CMOS process by varying supply voltages from 1 V to 1.8 V with 0.2 V steps. The simulation results show that the proposed circuit has less power consumption and is faster in comparison to other circuits.

KEYWORDS: Full adder, Differential cascode voltage switch logic, complementary pass-transistor logic, transmission-gate logic, DCVSL, CPL, TG, Power consumption, Delay, Power delay product, PDP.

1. INTRODUCTION

Most of the very large scale integration applications such as digital signal processing, image and video processing and microprocessors are common use calculation operations. In addition, subtraction and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of all these modules. Therefore, improvement its performance is acute for enhancing the overall module efficiency. Also recently with the ever increasing applications in mobile communications and portable equipment, the demand for low-power very large scale integration (VLSI) systems is steadily increasing.

Generally, hybrid-CMOS full adders are classified in three groups depending upon their structure and logical expression of the *Sum* output. The first classify of full adders is based on XOR gates and second one is based on XNOR gates. In Third category, the *Sum* and C_{out} are produced by XOR-XNOR intermediate signals. In this paper for design full adder the third category is utilized [1].

The full adder operation equations can be stated as follows: given the three 1-bit inputs A, B and C_{in} which calculate two 1-bit outputs *Sum*, for sum and C_{out}, for carry out. The relations between the inputs and the outputs are expressed as:

$$Sum = (A \oplus B) \oplus C_{in} \quad (1)$$

$$C_{out} = (A.B) + C_{in}.(A \oplus B) \quad (2)$$

In third category, the *Sum* and C_{out} are generated by the following expression, where H is the XOR of A and B, and $\overline{H}$ is the complement of H (XNOR),

$$Sum = (H \oplus C_{in}) = H.\overline{C_{in}} + \overline{H}.C_{in} \quad (3)$$

$$C_{out} = A.\overline{H} + C_{in}.H \quad (4)$$

Generally, this category is divided to three modules. Module 1 is a XOR–XNOR circuit producing H and $\overline{H}$ signals. Module 2 and 3 produce *Sum* and C_{out} as outputs, respectively.

A gate is evaluated by three basic parameters, area, delay time (propagation delay) and power consumption. Depending on the application, the emphasis will be on different parameters. The delay time depends on the size and number of transistors, the parasitic capacitance including intrinsic capacitance and capacitance due to routing and the number of logic gates. The power consumption depends on the switching activity, size and number of transistors, glitch, leakage current of transistors and sub-threshold current [2], [3].

Power consumption in CMOS digital circuits is divided into three main parts as follows [4]:

$$P_{Total} = P_{Dynamic} + P_{Short-circuit} + P_{Static} \quad (5)$$

$P_{Dynamic}$: Due to charging and discharging capacitances.

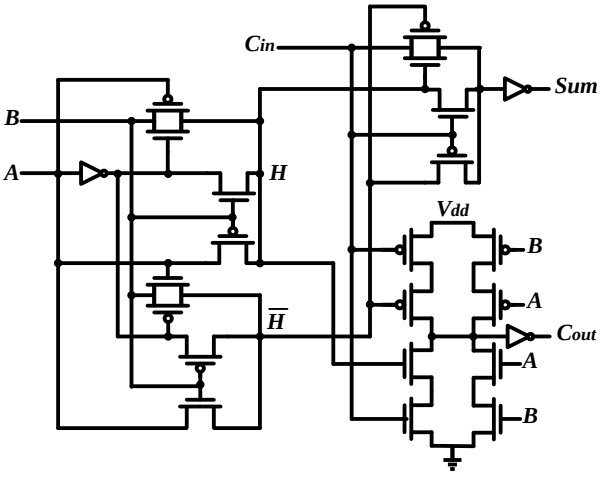
$P_{Short-circuit}$: Due to the current between power supply and ground during a transistor switching.

P_{Static} : Due to the leakage current and static current [3], [5].

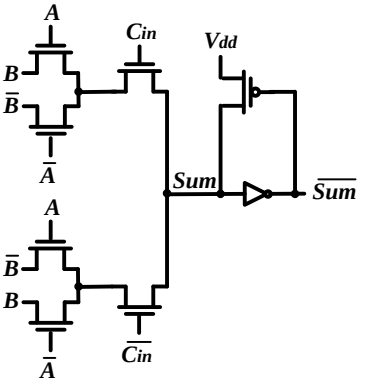
Many design considerations including the minimum transistor counts, low power consumption, less delay in critical path, full-swing output and chip area are focused recently. However, design of low-power high-speed adder has become one of the essential researches [1].

Several logic styles have been used to design full adder cells. Each design style has its own advantages and disadvantages. Classical designs of full adders normally use only one logic style for the whole full-adder design. Standard static CMOS, complementary pass-transistor logic, dynamic CMOS logic and transmission-gate are the most important logic design styles in the conventional adders. Lately for design full adders use more than one logic style. These full adders called hybrid-CMOS full adders. In these full adders, features of different logic styles are exploited to improve the performance

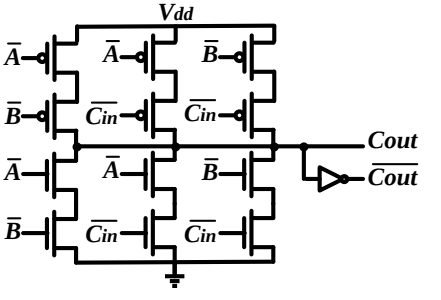
There are many papers in the field of hybrid-CMOS full adders design. In [1] a novel 1-bit full adder based on complementary pass-transistor logic and transmission gate logic is presented. In [6] a hybrid full adder, namely, the branch-based logic and pass-transistor (BBL-PT) cell is proposed. A new hybrid full adder based on pass-transistor logic and static CMOS logic is proposed in [7]. Other 1-bit hybrid full adder cells have been reported in the literature [8-10]. The proposed full adders in [1], [6] and [7] are shown in Fig. 1 (a), (b) and (c) respectively.



(a)



(b-1)



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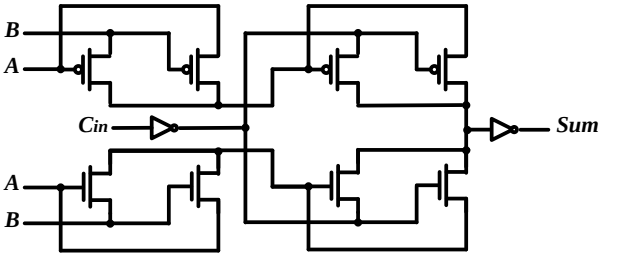
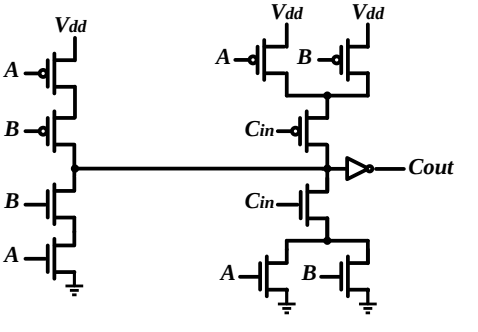


(c-1)



(c-2)

Fig. 1. Examples of hybrid-CMOS full adders (a) Full adder in [1], (b) Full adder in [6] {(b-1) sum, (b-2) carry out} and (c) Full adder in [7] {(c-1) sum, (c-2) carry out}.

In this paper a novel hybrid-CMOS full adder based on three logic styles (DCVSL-CPL-TG) is proposed. The paper is organized as follows. In Section 2 logic styles that used for designing full adder are studied. In section 3 the proposed full adder is presented. Simulation results in Section 4 and conclusion in Section 5 is expressed.

2. SURVEY OF DCVSL, CPL AND TG STYLES

2.1. DCVSL

One of the first realization of static differential CMOS logic known as the differential cascade voltage switch logic was introduced in 1984 [11]. The DCVSL style completely eliminates static currents and provides rail-to-rail swing. This style combines two concepts: differential logic and positive feedback. A differential gate requires that each input is provided in complementary format, and produces complementary outputs in turn. The feedback mechanism ensures that the load device is turned off when not needed. The DCVSL is depicted in Fig 2.

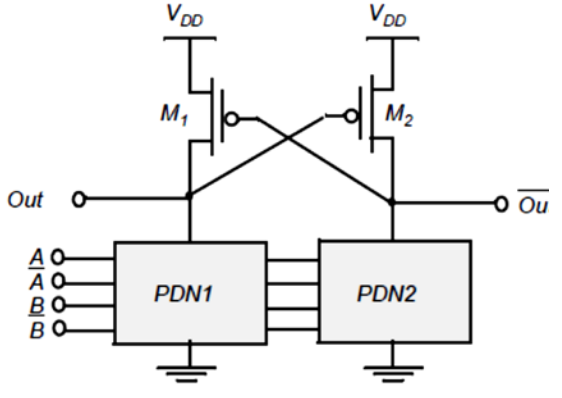


Fig. 2. Basic principle of DCVSL [3].

The pull-down networks PDN1 and PDN2 use NMOS devices and two networks cannot occur together (when PDN1 is on, PDN2 is off, and when PDN1 is off, PDN2 is on), such that the required logic function and its inverse are simultaneously implemented. Assume now that, for a given set of inputs, PDN1 is on while PDN2 is off, and that *Out* and $\overline{Out}$ are initially high and low, respectively. Turning on PDN1, causes *Out* to be pulled down, although there is still a fight between M1 and PDN1. $\overline{Out}$ is in a high impedance state, as M2 and PDN2 are both turned off. PDN1 must be strong enough to bring *Out* below $V_{DD} - |V_{Tp}|$, the point at which M2 turns on and starts charging $\overline{Out}$ to V_{DD} —eventually turning off M1. This in turn enables *Out* to discharge all the way to *GND* [3].

2.2. CPL

The complementary pass transistor logic was first introduced in 1990 (Yano, K, et al) [12]. The CPL style improves speed and reduces power consumption. The basic idea (similar to DCVSL) is to accept true and complementary inputs and generate true and complementary outputs [3]. The general structure of CPL is shown in Fig. 3. This style consist of complementary input/output, NMOS pass-transistor logic network and CMOS output inverters [12].

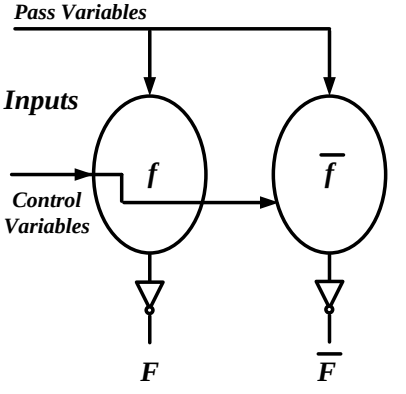


Fig. 3. CPL logic structure [13].

2.3. TG

The transmission gate is one of the most commonly used structures for full adder designs. The basic transmission gate includes a PMOS and NMOS transistors connected in parallel as shown in Fig. 4. The control signal *C* is applied to the gate of the NMOS and the complement $\overline{C}$ is applied to the gate of the PMOS. The bulk of the NMOS and PMOS are connected to *GND* and V_{DD} respectively. NMOS transistors pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The transmission gate acts as a bidirectional switch controlled by the gate signal *C*. When *C*=1, both MOSFETs are on, allowing the signal to pass through the gate. On the other hand, *C*=0 places both transistors in cutoff, creating an open circuit between nodes *A* and *B* [3]. This style is suitable for solving the problem of voltage drop and can be used to build some complex gates very efficiently.

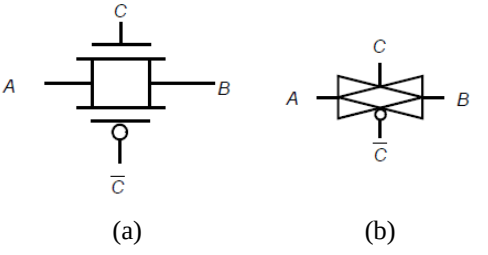


Fig. 4. (a) Circuit, (b) Symbol [3].

3. PROPOSED FULL ADDER

In this section a new hybrid-CMOS full adder includes DCVSL, CPL and TG styles are proposed. The proposed full adder which includes 16 transistors is shown in Fig. 5. The DCVSL style is used to produce $A \oplus B$ and $\overline{A \oplus B}$. This style resulting circuit exhibits a rail-to-rail swing, and the static power dissipation is eliminated. The CPL style is utilized to generate *Sum* signal. This style is generating full swing outputs; reduce power consumption, improve speed and noise margin. Finally, TG style is used to generate C_{out} with full swing output, high speed and low power consumption. This full adder is robustness against voltage scaling and transistor sizing. Also enables it to operate reliably at low voltage.

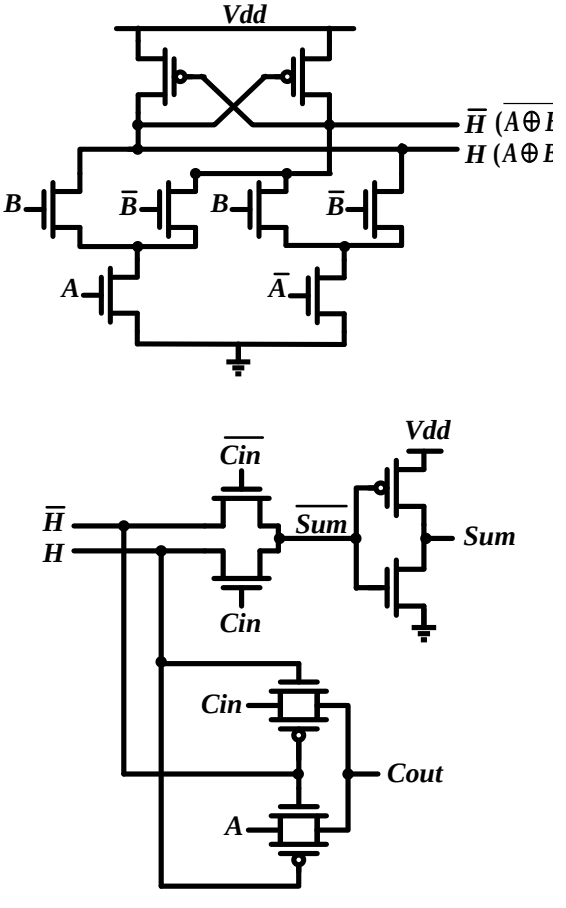


Fig. 5. Proposed full adder cell.

4. SIMULATION RESULTS

In this section, simulation of full adder cells (proposed full adder and full adder in [1], [6], [7]) is presented under the below conditions.

All the circuits are simulated using HSPICE in 0.18 μm CMOS process at room temperature with varying supply voltages from 1 V to 1.8 V with 0.2 V steps. The used simulation test bench is shown in Fig. 6, two CMOS inverters are inserted in serial in the input and output terminals of each adder respectively to accurately predict the circuit performance. The two inverters forms buffer function to simulate the signal driving capability and loading effects [7].

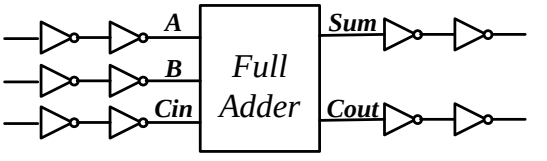


Fig. 6. Simulation test bench.

The input patterns used for simulations and output waveforms are shown in Fig. 7. For an accurate result, all the possible input combinations are considered for all the test circuits.

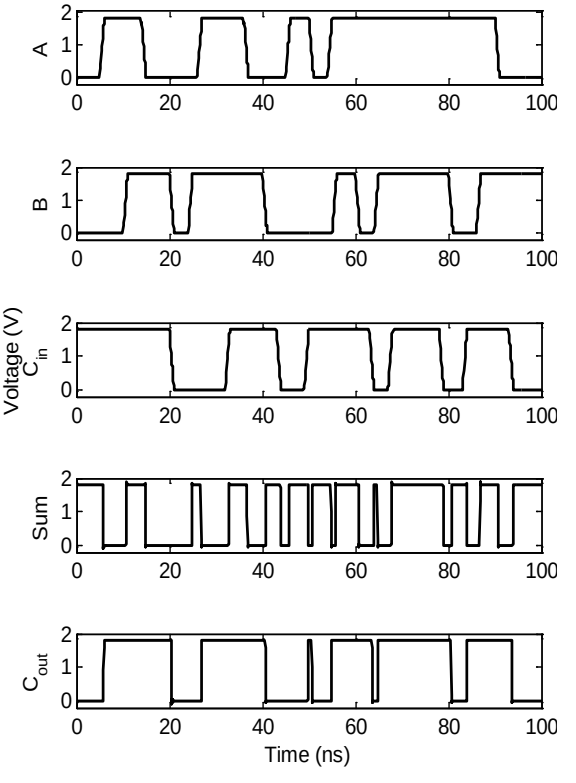


Fig. 7. Input patterns (*A*, *B* and C_{in}) used to test 1-bit adder cells and output waveforms of proposed full adder (*Sum* and C_{out}). Frequency of the inputs is 50 MHz with a supply voltage of 1.8 V.

The circuit performance of the test circuits is evaluated in terms of worst-case delay, power dissipation, and power delay product (PDP). To have a fair comparison, all the simulated circuits are prototyped at optimized transistor sizing values to achieve the best PDP. Also for the calculation of the power delay product, worst-case delay is chosen to be the larger delay amongst the two outputs.

4.1. DELAY

The delay is calculated from 50% of voltage level of input to 50% of voltage level of resulting output all the rise and fall output transitions. The propagation delay of the all full adder is show in Fig. 8. The proposed circuit has minimum propagation delay compared to other full adders.

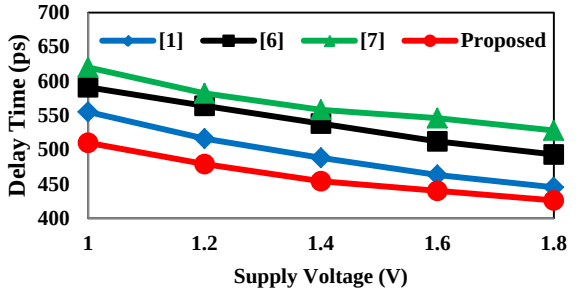


Fig. 8. Delay of the full adder cells vs. supply voltage.

4.2. POWER CONSUMPTION

The average power consumption of the all full adder is show in Fig. 9.

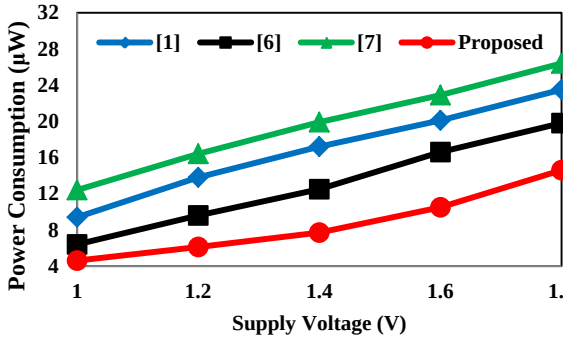


Fig. 9. Power consumption of the full adder cells vs. supply voltage.

4.3. POWER DELAY PRODUCT

The value of PDP under different supply voltage is shown in Fig. 10.

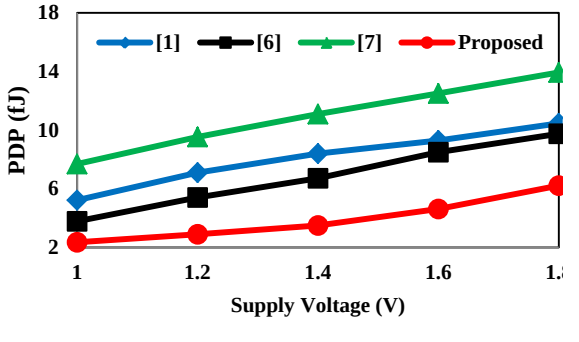


Fig. 10. PDP of the full adder cells vs. supply voltage.

The PDP is a quantitative measure of the efficiency of the tradeoff between power dissipation and speed, and is particularly important when low power operation is needed.

The simulation results of the all full adders are summarized in Table 1. According to this observing simulation results in Table 1, the proposed full adder in the average power dissipation, delay and power delay product is much better than other full adders. Our design takes approximately 35% to 60% less power, 4.46% to 23.94% better in time delay.

Table 1. Simulation results for full adders at 1.8 V power supply and 50 MHz frequency.

Full Adder	Power Consumption (µW)	Delay (ps)	PDP (fJ)	Device Count
[1]	23.5	445	10.46	26
[6]	19.8	493	9.76	23
[7]	26.4	528	13.94	24
Proposed	14.6	426	6.22	16

5. CONCLUSION

In this paper, a novel hybrid full adder cell based on differential cascode voltage switch logic, complementary pass-transistor logic and transmission-gate logic is presented. The advantages of these logic styles are low power consumption, high speed and full swing outputs. The compared results show that the performance of the proposed design is superior to other designs. The new full adder circuit has minimum PDP so that 57% to 124.1% improvement in PDP compare to other full adder cells. Also the proposed adder has propagation delay of 426 ps and power dissipation of 14.6 µW in a supply voltage of 1.8 V.

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