Bang-Bang clock and data recovery circuits – A survey

(Invited Paper)

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ABSTRACT:
Nowadays, the volume of the data transported in telecommunication systems is noticeably growing, which means that the bandwidth required for data transmission is also increasing. However, due to high transmission speed of the data, those circuits are needed which can properly act at high speed (frequency). Clock and data recovery (CDR) circuit using bang-bang phase detector (BBPD) are widely used in communication systems mainly because of their high-frequency capabilities. However, bang-bang clock and data recovery (BBCDR) circuits are hard nonlinear systems due to the nonlinearity introduced by the binary phase detector (BPD). In this paper, first, architecture of BBCDR circuits is stated in addition to expressing basic concepts of clock and data recovery circuits. Since characteristics of frequency response of CDR are determined by jitter tolerance and jitter transfer characteristics, concepts of these characteristics are mentioned and the presented analyses are evaluated.

KEYWORDS: Clock and Data Recovery (CDR), Bang-Bang Phase Detector (BPD), Jitter Transfer and Jitter Tolerance.

1. INTRODUCTION

The volume of the data transported over the Internet backbone has increased with the exponential growth of the number of Internet users. This means that the bandwidth requirements will extremely increase. Among the available transmission media, optical fibers achieve the highest bandwidth and the lowest lost. The majority of the backbone optical communication systems is based on the Short for Synchronous Optical Network (SONET) standard which defines a hierarchy that allows the data stream of different rates to be multiplexed.

Despite the unique transmission capabilities of optical fiber, the data get distorted while traveling through the fiber, which is because of the fiber dispersion. Thus, the transported data are required to be regenerated in the receiver by clock and data recovery (CDR) circuits. However, due to high transmission speed of the data, those circuits are needed which can properly act at high speed (frequency). CDR circuit using bang-bang (binary) phase detectors (BBPDs) is widely used in communication systems mainly because of its high-frequency capabilities [1]. Its examples include multi-gigahertz clock multipliers [2] and optical receivers (SONET) [3].

In this paper, jitter transfer and jitter tolerance for BBCDR with a first order loop filter are characterized by Fourier series analysis and formulating the time domain waveforms. As a result, new closed form equations are presented for the jitter transfer and the jitter tolerance. The presented method is general enough to be used for designing the BBCDR. Also, the proposed analysis does not need any extra assumption on system parameters especially loop capacitance. Behavioral simulation will be used to validate the analytical results with particular emphasis on jitter transfer and the jitter tolerance characteristics.

This paper is organized as follows. Section 2 reviews the BBCDR in the literature. In Section 3, different works on BBCDR loop analysis are briefly introduced; moreover, the most important analysis which has been given in the references is thoroughly described. Section 4 shows the transistor level simulation of BBCDR. Simulation results are compared with the values estimated by equations to show the validity of the method in Section 5. Finally, the paper will be concluded in Section 6.

2. BANG-BANG CDR

2.1. Basic Concept of CDR

In order to perform synchronous operations such as retiming on random data, optical receivers must generate a clock. As illustrated in Figure 2, a clock recovery circuit senses the data and produces a periodic clock. A D flip-flop driven by the clock then retimes the data; i.e., it samples the noisy data, yielding an output with less jitter. As such, the flip-flop is

sometimes called a "decision circuit". Note that the zero crossing of the received data are corrupted by noise and jitter whereas those at the flip-flop output area as "clean" as the recovered clock itself. This removal of timing errors forms the essence of data retiming [4] [5].

The clock generated in the circuit of Figure 2 must satisfy three important conditions. (1) It must have a frequency equal to the data rate; e.g., a data rate of 10 Gb/s (each bit 100 ps wide) translates to a clock frequency of 10 GHz (with a period of 100 ps). (2) It must bear a certain phase relationship with respect to data, allowing optimum sampling of the bits by the clock. As exemplified by the waveforms shown in Figure 3, if the rising edges of the clock coincide with the midpoint of each bit, then the sampling occurs farthest from the preceding and following data transitions, providing maximum margin for jitter and other timing uncertainties. (3) It must exhibit a small jitter as it is principal contributor to the retimed data jitter [4] [5].

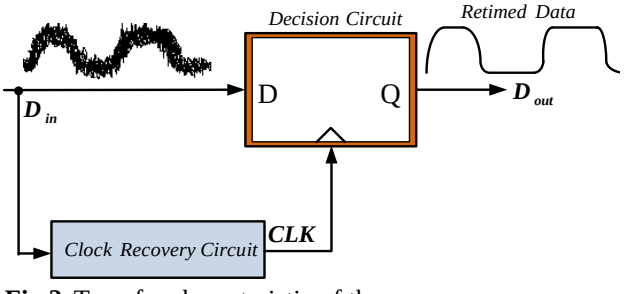


Fig.2. Transfer characteristic of the

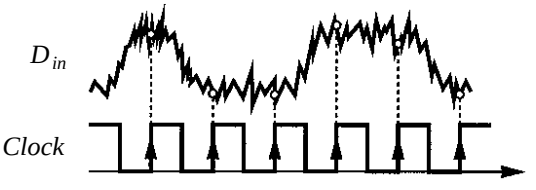


Fig.3. Optimum sampling of noisy data

2.2. Alexander (Bang-Bang) Phase Detector

The most commonly used bang-bang phase detector is the circuit proposed by Alexander [4] [5]. Figure 4(a) illustrates the Alexander PD principle, also known as the "early-late" detection method. Using three data samples, S_1-S_3, taken by three consecutive clock edges, the PD can determine whether a data transitions, all three samples are equal and no action is taken. If the falling edge of the clock leads (is "early"), then the last sample, S_3, is unequal to the first two. Conversely, if the clock lags (is "late"), then the last two samples, S_2 and S_3, are equal but unequal to the first sample, S_1. Thus, $S_1 \oplus S_2$ and $S_2 \oplus S_3$ provide the early-late information: (a) if $S_1 \oplus S_2$ is high and $S_2 \oplus S_3$ is low, then the clock is late; (b) if $S_1 \oplus S_2$ is low and $S_2 \oplus S_3$ is high, then the clock is early; (c) if $S_1 \oplus S_2 = S_2 \oplus S_3$, then no data transition is present.

The foregoing observations lead to the circuit topology shown in Figure 4(b) [4] [5]. Flip-flop FF_1 samples S_1 and S3 on the rising edge of clock and flip-flop FF_2 delayed the result by one clock cycle. Flip-flop FF_3 samples S_2 on the falling edge of clock and flip-flop FF4 delayed this sample by half a clock cycle.

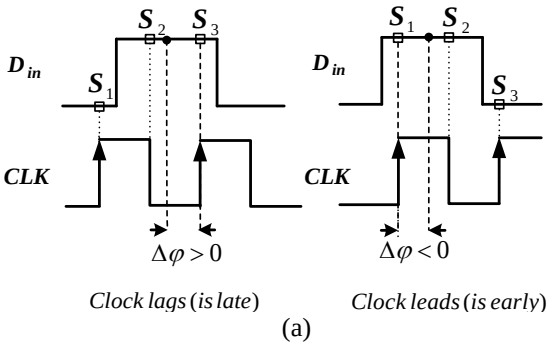
As depicted in Fig 4(c), the first rising edge of clock samples a high data level. The second rising edge of clock then accomplishes two tasks: it produces a delayed version of the first sample at the output of FF_2, and it samples the low level on the input data. The values of S_1 and S_2 are therefore valid for comparison at $t=T_1$, remaining constant for one clock period.

On the first falling edge of clock in Figure 4(c), FF_3 samples a high level on the input data and on the next rising edge, FF_4 reproduces this level. The key point here is that the choice of clock phases for the four flip-flops ensures that S_1, S_2 and S_3 reach valid levels for comparison at $t=T_1$, and remain at three levels for one clock period. As a result, the XOR gates generate valid outputs simultaneously.

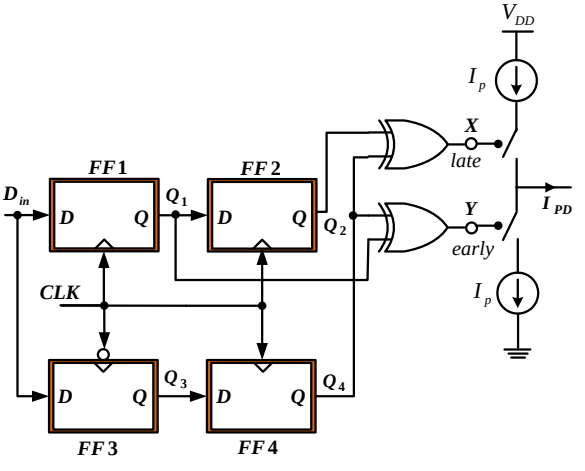
As shown in Figure (4), if the clock is late ($\Delta\varphi<0$), X assumes a high level for each data transition and Y a low level. Thus, the average PD output, $(X-Y)_{ave}$, remains at a high positive value. Conversely, if $\Delta\varphi>0$, then $(X-Y)_{ave}$, assumes a high negative value.

The advantage of BBPD over linear phase detectors is that BBPD exhibits a very high gain in the vicinity of $\Delta\varphi=0$ and is able to operate at higher speeds. Since, in linear detector and in the case of phase difference exists, a pulse proportional to the phase difference is generated; however, if frequency is high, the width of the produced pulse would be very narrow. In other words, the average output value of the PD would be very small and, as a result, the voltage required for adjusting frequency would not be provided and CDR would not properly work. But, if there is large or small phase difference, due to having very high gain BBPD produces constant and large voltage in the output to move the CDR loop toward the lock. In other words, BBPD output has two distinct and deterministic levels; depending on the sign of the input phase-difference. This has led to its application at higher speed (frequency).

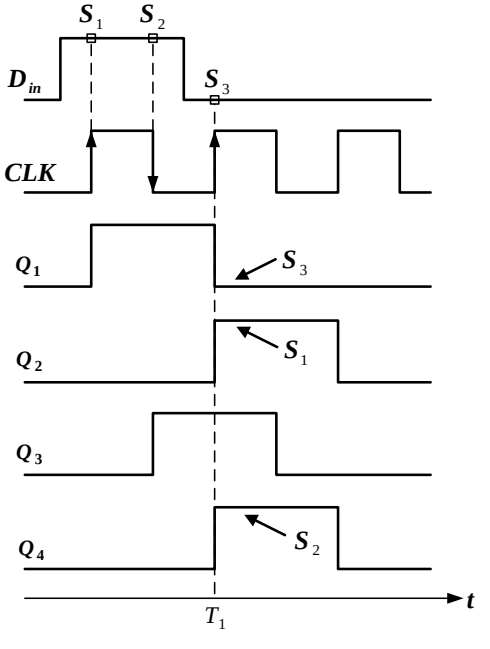
The transfer characteristic of a BBPD is shown in Figure (5). The output of BBPD is +1 and -1 for positive and negative phase errors, respectively. Thus, CDR based on BPD (BBCDR) is a nonlinear system due to the inherent nonlinear phase to voltage transfer function of the BBPD. Thus, unlike a linear CDR, the analysis of a bang–bang loop is complicated.



(a)



(b)



(c)

Fig.4. (a) Three-point sampling of data by clock, (b) Alexander phase detector, and (c) its waveforms.

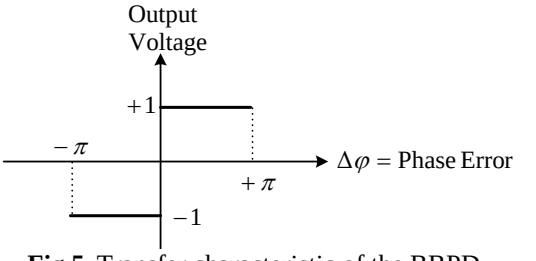


Fig.5. Transfer characteristic of the BBPD.

2.3. BBCDR Architecture

In general terms, the CDR architecture is similar to that of the PLL. The only difference is in the type of phase detector. The important point is that, in contrast to the phase detector in PLL which deals with periodic the input signal, the input data are random in the CDR. Also, considering that every bit of input data is recovered by one clock period in the CDR, data frequency (bit rate) is half of the clock (VCO) frequency. But, the frequency of the compared signals in the PLL (input and output signals of the PLL) is not equal in the input of phase detector. Using linear detectors, CDR relatively meets the needs of a system. However, for high speed applications, the CDR based on bang-bang detector is used. Since, in the CDR with linear phase detector a pulse proportional to the phase difference is produced. But, if frequency is high, the produced pulse width would be very narrow; in other words, the average value of the voltage generated in the linear PD output would be very small and, consequently, the required voltage for adjusting frequency would not be provided. Then, a long time would be required to provide sufficient voltage. Therefore, locking time would be long. But, in a bang-bang detector, in the case of small or large phase difference, constant and large voltage would be produced in the output in order to rapidly lock the CDR loop. These two important differences cause a distinction between the detectors used in CDR and the conventional PLL.

Figure (6) shows a block diagram of typical second order BBCDR which is composed of a data sampler bang- bang PD, a charge-pump or V/I converter, a first order loop filter and a voltage-controlled oscillator (VCO) [5]-[9]. The PD detects the phase difference between the data-sampling clock and the center of the incoming data and generates late or early signals for the charge-pump or V/I converter. The charge-pump supplies the loop filter that includes R_p, C_p according to the signals generated by the PD. The voltage over the loop filter is the VCO control voltage and determines the frequency and phase of the sampling clock. With this feedback mechanism, the data-sampling clock tracks the center of the incoming data bits, and the

clock to which the data is synchronized will be recovered in the receiver.

In some practical systems, a second capacitor is usually added in parallel with R_p and C_p and it increases the loop filter order to two. This capacitor is used to suppress the sudden jump on the VCO control voltage produced by charge injection and clock feed through of the two switches and improves the transient characteristics. If this capacitor is much smaller than C_p, for example about one-fifth to one-tenth of C_p, the time domain waveforms and frequency response remain relatively unchanged and are similar to those of the first order loop filter [5]-[9]. As a result, in this paper the added capacitor (C_2) is chosen much smaller than C_p and the BBCDR with a first order loop filter is analyzed.

The phase-domain model of the BBCDR has been shown in Figure (7) [5]-[9]. This model was implemented for a behavioral simulation to verify the accuracy of the derived equations. In Fig. 3, K_{VCO} is the VCO gain and I_p is the charge pump current. Here, $\varphi_{in}(t)$ and $\varphi_{out}(t)$ denote the excess phases of the input and output, respectively.

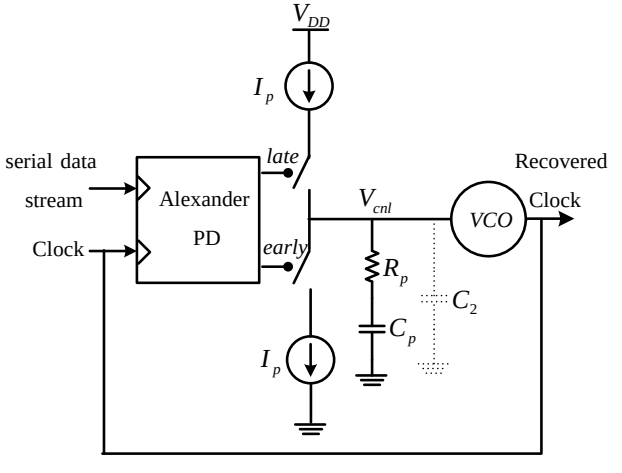


Fig.6. Structure of the second order CDR with a bang-bang phase detector and First-order loop filter.

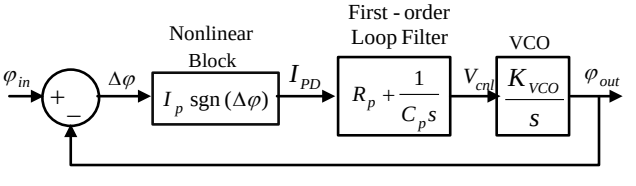


Fig.7. Phase domain model of the second order CDR based on bang-bang phase detector.

3. BBCDR JITTER ANALYSIS

The response of CDR to jitter is of extreme importance in most applications. Since, the jitter at the input leads to bit error at the output of CDR therefore, jitter analysis is very important for evaluating the performance of BBCDR. Therefore, the concept of jitter is first introduced in this paper. In an ideal PLL or CDR, the input or output signals are an ideal sinusoid at the frequency of $\omega_0=2\pi f_0=2\pi/T_0$ and can be expressed as $A\cos(\omega_0 t)$. Thus, the period is constant and the zero-crossing points occur at exactly integer multiples of T_0. But, in actual PLL or CDR, the input or output signals can be generally considered as $A\cos[\omega_0 t+\varphi_n(t)]$, where, $\varphi_n(t)$ indicates random phase variations caused by internal and external noise sources. Also, $\varphi_n(t)$ is called the excess phase. Since frequency is the derivative of phase, it can be imagined that $\varphi_n(t)$ causes small random changes in frequency. In other words, $\varphi_n(t)$ causes variation of the period of signal from its ideal value. Here, the zero-crossing may not occur at integer multiples of T_0. Therefore, the deviation of each period from ideal value in time is called jitter. It can be concluded that $\varphi_n(t)=0$ means the signal with no jitter.

In practical digital communication standards, the specification of the CDR frequency response is determined by jitter tolerance and jitter transfer characteristics. Jitter transfer characteristic can be considered as a gain by which the CDR attenuates or amplifies input jitter. This characteristic is indeed the same as the close loop transfer function. The frequency domain characteristic of jitter transfer must meet some requirements. First, the BBCDR loop bandwidth should be very small. Second, the peak of the jitter transfer must not be greater than a specific value. The amount of peaking in the jitter transfer must be less than 0.1 dB for SONET standard. So, the analysis of peaking is required. If the value of jitter peaking exceeds a definite level, a jump will occur in the amplitude of the output phase in the jitter frequency close to f_C. Then, the output phase may not track the input phase, which leads to bit error. On the other hand, long-haul networks employ many data regenerators in the signal pass and periodically suppress the effect of fiber non-idealities. It is therefore important to minimize the jitter accumulated through the chain of the repeaters, i.e. each repeater must provide a small jitter bandwidth. Furthermore, since the equivalent jitter transfer function of a cascade of regenerators is given by the product of the individual transfer functions, the amount of jitter peaking per generator must be so small that tens of them still yield acceptable peaking [5].

In the CDR, since the incoming data may exhibit substantial noise and experience considerable attenuation, the data bits must be ideally sampled by the recovered clock at their midpoints so as to provide maximum distance from the decision threshold and data transition points. The jitter tolerance characteristic determines the peak-to-peak amplitude of the input jitter for a given jitter frequency, which can be applied

to the CDR input without worsening the bit error rate (BER).

Thus, designers are still looking for the ways to design loop parameters and estimate the frequency response characteristic. Therefore, the first step is accurate analysis of the CDR loop.

Many efforts have been made to analyze the nonlinear loop dynamic of BBCDR [10]-[19]. However, almost none of these references have provided an analysis for designing the CDR directly so a more general analysis should be implemented. The effect of jitter can be accurately analyzed using Markov models but their applicability has been limited to first-order loop (without loop filter capacitor) [10]–[12]. Also, in [13] modeling and designing BBCDR with first order loop was presented. In [14], the effect of non-accumulative reference clock jitter (referred to as the input jitter throughout) on the output jitter in second-order BBPLL was modeled as a 2-D Markov chain. In [15], the steady-state analysis of BBCDR was performed for the cases with no jitter in the input and the value of output jitter amplitude was derived. However, jitter transfer and jitter tolerance characteristics have not been presented. Moreover, [16] and [17] mainly focus on the characterization of the jitter transfer and tolerance of BBCDR in response to large sinusoidal input jitters. In [16], the jitter transfer properties were investigated for the first order BBCDR (without loop capacitor) and in [17], an approximation was used to introduce a linear model of a second-order bang–bang loop and the slewing effect was utilized to derive expressions for jitter transfer, jitter tolerance and jitter generation. However, in [17], the analysis method was based on a large off-chip value assumption for the loop filter capacitor [18] and by this assumption, the voltage variations across loop capacitor have been ignored in obtaining the jitter transfer characteristic. In addition, for calculating the jitter tolerance characteristic at low jitter frequencies, the loop filter resistor effect has been neglected and only the capacitor has been considered in the calculations. But along with the increase of frequency, the effect of resistor will be considered and the voltage variations of capacitor are ignored. On the other hand, the off-chip capacitor increased the number of external components and pin count; also, it coupled noise from off-chip to the control voltage of the voltage-controlled oscillator (VCO) in the CDR block. Another issue was that the bond wire inductor drastically increased the high-frequency impedance of the loop filter and made the CDR more sensitive to high-frequency noise [18].

3.1. Jitter Transfer Analysis

The jitter transfer function is defined as the ratio of the output signal jitter to the jitter applied on the input versus frequency. Jitter transfer can be considered as a gain by which the CDR attenuates or amplifies input jitter. Jitter transfer must meet some specifications. Figure (8) shows the requirements for jitter transfer. As an example, in the SONET OC-48, the cutoff frequency, f_C, is 2MHz and the peaking is 0.1 dB [5].

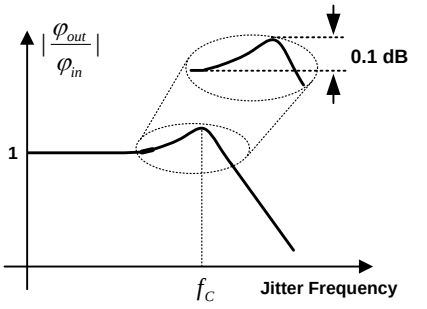


Fig.8. Jitter transfer curve [5].

In binary CDR, the jitter transfer function strongly depends on the input jitter magnitude. Thus, the linear models cannot be applied to binary CDR analysis.

As shown in Figure (7), the transfer function from I_{PD} to φ_{out} is equal to

$$F(s)=\frac{\varphi_{out}}{I_{PD}}(s)=\frac{K_{VCO}}{C_P}\left[\frac{R_P C_P s+1}{s^2}\right] \quad (1)$$

Thus, the differential equation can be obtained by calculating the inverse Laplace transform of (1)

$$\frac{d^2\varphi_{out}}{dt^2}=K_{VCO}R_P\frac{d I_{PD}}{dt}+\frac{K_{VCO}}{C_p}I_{PD} \quad (2)$$

Where, $I_{PD}=I_P\text{sgn}(\Delta\varphi)$. For negligible jitter peaking and jitter frequency close to f_C, the waveforms of the BBCDR have typical prototypes shown in Figure (9). Also, as the input jitter frequency exceeds f_C, the output jitter magnitude begins to fall as shown Figure (10). It can be reasonably assumed that all of the waveforms are symmetric around origin and have the same period of T_P. Where, T_P is the period of the applied input sinusoidal jitter. It should be noted that, as shown in Fig.5, there is a little peaking in the output phase at jitter frequencies near to f_c, which means definitely, φ_{out} is larger than φ_{in}. The waveform of φ_{out} and φ_{in} for $0<t<t_{max}$ has been shown in Figure (9) in a larger scale. Therefore, if $0<t<t_{max}$ then $\Delta\varphi<0$ and $I_{PD}=-I_P$.

As depicted in Figure (9), the output of the nonlinear component, I_{PD} is a periodic square wave and the derivative of it with respect to time causes the production of impulse functions plotted in Figure (11).

Using Fourier series, the periodic function $I_{PD}(t)$ can be expanded as:

$$I_{PD}(t)=a_0+\sum_{n=1}^{+\infty}[a_n\cos(n\omega_p t)+b_n\sin(n\omega_p t)] \quad (3)$$

Where, the Fourier coefficients a_i's and b_i's are generally the function of I_p and ω_p, determined by

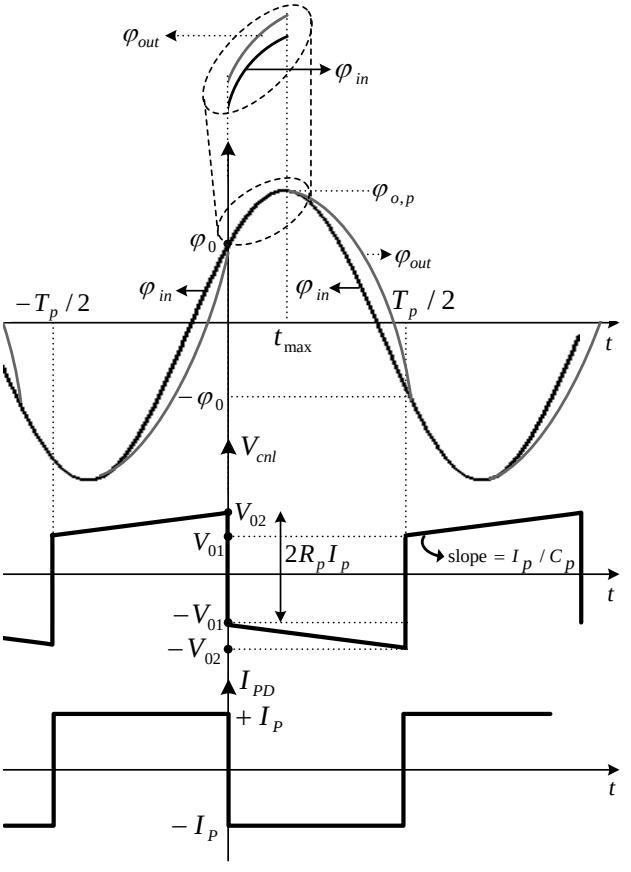


Fig.9. Waveforms of the BBCDR with first-order loop filter at jitter frequency close to f_C.

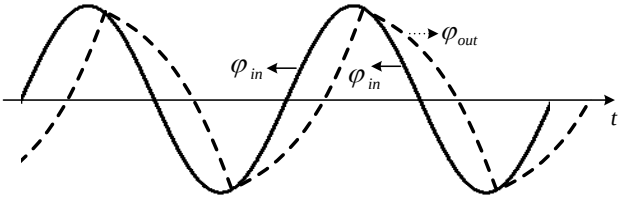


Fig.10. Waveforms of the BBCDR with first-order loop filter as jitter frequency exceeds f_C.

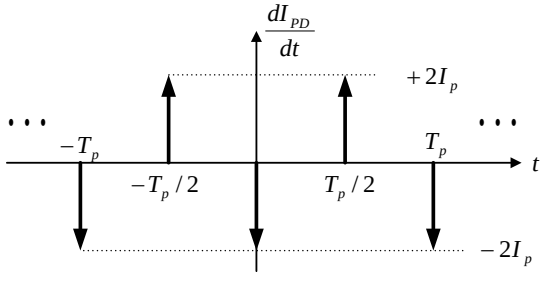


Fig.11. Waveform of dI_P/dt.

$$a_0 = \frac{1}{T_p}\int_0^{T_p} I_{PD}(t)\,dt \tag{4}$$

$$a_n = \frac{2}{T_p}\int_0^{T_p} I_{PD}(t)\cos(n\omega_p t)dt \quad , \quad \omega_p = \frac{2\pi}{T_p} \tag{5}$$

$$b_n = \frac{2}{T_p}\int_0^{T_p} I_{PD}(t)\sin(n\omega_p t)dt \tag{6}$$

As depicted in Fig.9, due to the odd nature of $I_{PD}(t)$, $a_0=a_n=0$, according to (6):

$$b_n = \frac{4I_P}{2n\pi}[(-1)^n - 1] = -\frac{4I_P}{n\pi} \quad , \quad \text{for } n\text{'s odd} \tag{7}$$

As a result, $I_{PD}(t)$ can be rewritten as follow:

$$I_{PD}(t) = -\frac{4I_P}{\pi}\sum_{n=1}^{+\infty}\frac{1}{n}\sin(n\omega_p t) \tag{8}$$

As shown in Figure (11), for $0 \le t \le T_P$,dI_{PD}/dt can be defined as follow

$$dI_{PD}/dt = 2I_P[-\delta(t) + \delta(t - T_p/2)] \tag{9}$$

Thus, the Fourier coefficients of dI_{PD}/dt are obtained as follows

$$a_0 = 0 \tag{10}$$

$$a_n = -\frac{8I_P}{T_p} \quad , \quad n = odd \tag{11}$$

As shown in Figure (11), since $dI_{PD}(t)/dt$ is an even function, $b_n=0$. Therefore, the Fourier series of $dI_{PD}(t)/dt$ is

$$\frac{dI_{PD}}{dt} = -\frac{4\omega_p}{\pi} I_P \sum_{n=1}^{+\infty}\cos(n\omega_p t) \tag{12}$$

Substituting (9) and (14) into (2), we have

$$\frac{d^2\varphi_{out}}{dt^2} = \sum_{n=1}^{+\infty} a_n\cos(n\omega_p t) + b_n\sin(n\omega_p t) = \sum_{n=1}^{+\infty} A_n\cos(n\omega_p t + \theta_n) \tag{13}$$

where,

$$a_n = -\frac{4}{\pi} I_P K_{VCO} R_P\,\omega_p \tag{14}$$

$$b_n = -\frac{4}{n\pi}\frac{I_P K_{VCO}}{C_P} \tag{15}$$

$$A_n = \sqrt{a_n^2 + b_n^2} \tag{16}$$

$$\theta_n = \tan^{-1}(b_n/a_n) \tag{17}$$

As depicted in Figure (9), $\varphi_{out}(t)$ is a continuous time signal and the Fourier series can be obtained by double integration of (13) as follows

$$\varphi_{out}(t)=\sum_{n=1}^{+\infty}-\frac{A_n}{(n\omega_p)^2}\cos(n\omega_p t+\theta_n) \qquad (18)$$

Note that the output jitter magnitude consists of various harmonics. From (1) the linear block F(s) has low-pass properties, i.e.

$$|F(j\omega_p)|>>|F(jn\omega_p)| \quad \text{for} \quad n=2,3,... \qquad (19)$$

This implies that higher-order harmonics in the output of the BBCDR will be filtered out significantly and therefore, these higher-order harmonics can all be neglected in the analysis in comparison with the magnitude of fundamental component. In other words, from (18) the amplitude of *n*th harmonic is attenuated in a ratio of $1/n^2$. Therefore, we only need the fundamental term in the Fourier series. It follows as

$$|\varphi_{out}|_{\max}=\varphi_{o,p}\approx\frac{A_1}{\omega_p^2} \qquad (20)$$

Assuming, the input jitter magnitude is equal to $\varphi_{i,p}$, and the value of the jitter peaking is approximately zero, at jitter frequencies close to f_c, still $|\varphi_{o,p}/\varphi_{i,p}|=1$. It follows that

$$\begin{aligned}|\frac{\varphi_{o,p}}{\varphi_{i,p}}|&=\frac{1}{\varphi_{i,p}}\frac{A_1}{\omega_p^2}=\frac{1}{\varphi_{i,p}}\frac{\sqrt{a_1^2+b_1^2}}{\omega_p^2}\\&=\frac{1}{\varphi_{i,p}\omega_p^2}\sqrt{(\frac{4}{\pi}K_{VCO}\,R_P\,I_P\omega_p)^2+(\frac{4}{\pi}\frac{K_{VCO}}{C_P}I_P)^2}=1\end{aligned} \qquad (21)$$

And finally the equation for the corner frequency is as (22).

$$\varphi_{i,p}^2\omega_p^4-(K_V R_P C_P)^2\omega_p^2-K_V^2=0 \qquad (22)$$

where

$$K_V=\frac{4K_{VCO}I_P}{\pi C_P} \qquad (23)$$

Equation (22) can be used to derive an approximate value for the -3db bandwidth (ω_P) of the jitter transfer.

It is therefore possible to approximate the entire jitter transfer with a first order low pass filter as (24)

$$\frac{\varphi_{out}}{\varphi_{in}}(s)=\frac{1}{1+\frac{s}{\omega_P}} \qquad (24)$$

As expected, it can be seen from (22) that in binary CDR, the bandwidth of the jitter transfer depends on the input jitter magnitude ($\varphi_{i,p}$).

Note that, the above analysis is valid when the value of the jitter peaking is approximately zero. This is equivalent to the large damping factor in the vicinity of ω_P. Thus, this condition should be met. Jitter peaking does not occur when the maximum output phase stays smaller than the maximum input phase. In order words, the expression (25) should be satisfied.

$$\varphi_{o,p}\le\varphi_{i,p} \qquad (25)$$

Using (21), the following important result can be derived.

$$\frac{1}{\omega_p^2}\sqrt{(\frac{4}{\pi}K_{VCO}\,R_P\,I_P\omega_p)^2+(\frac{4}{\pi}\frac{K_{VCO}}{C_P}I_P)^2}\le\varphi_{i,p} \qquad (26)$$

Equation (26) is generally used for designing the BBCDR loop parameters to meet SONET jitter transfer requirements (loop bandwidth and jitter peaking). The design methodology for the CDR is described as follows

1) The parameters ω_P and input jitter amplitude ($\varphi_{i,p}$) are given.

2) Having the VCO gain, the on-chip loop capacitor (C_p) and the reasonable value for loop resistor, the charge pump current I_p can be easily obtained from (28). As a result, jitter peaking is negligible.

3.2. Jitter Tolerance Analysis

In the CDR, since the incoming data may exhibit substantial noise and experience considerable attenuation, the data bits must be ideally sampled by the recovered clock at their midpoints so as to provide maximum distance from the decision threshold and data transition points. This concept is shown in Figure (12). For slowly varying jitter at the incoming data, the recovered clock tracks the phase variations in order to accurately sample the data to avoid increasing the BER. For rapidly varying jitter, the clock can not fully track the input phase variations and thus fail to sample the data optimally and create a greater BER. The jitter tolerance determines the peak-to-peak amplitude of the input jitter for a given jitter frequency, which can be applied to the CDR input without worsening the bit error rate (BER) of 10^{-12}. Jitter tolerance represents the ability of the CDR to recover an incoming serial data correctly despite the applied jitter. As illustrated in Figure (13), the specification is typically described by a jitter tolerance mask as a function of the jitter frequency. As an example, in the SONET OC-48, the CDR must withstand a peak-to-peak jitter of 15 UI [UI=Unit Interval] if the jitter frequency varies at a rate below 100Hz [5].

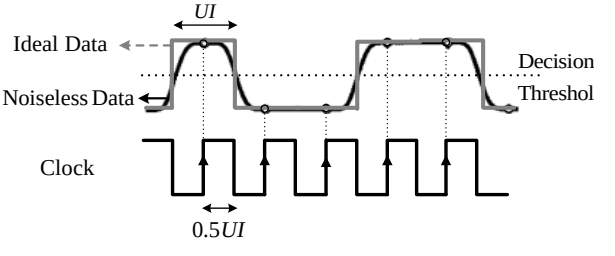


Fig.12. Noiseless data sampled by clock.

In order to achieve good jitter tolerance, high bandwidth is required so that the CDR can track the jittery input signal and be able to recover the incoming serial data. On the contrary, jitter transfer compliance is achieved by limiting the bandwidth of the CDR to ensure that higher frequency jitter is reduced. However, in binary CDR, the loop bandwidth cannot be defined in a given value because the loop bandwidth strongly varies with the input jitter magnitude.

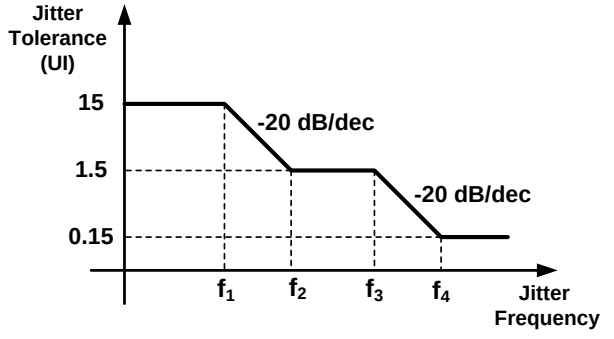


Fig.13. Jitter tolerance mask.

When input jitter frequency exceeds the loop bandwidth frequency, the output jitter magnitude begins to fall as shown in Figure (14). It is instructive to quantify the jitter tolerance of a typical CDR loop and compare the result with the mask shown in Fig. 8. At a given jitter frequency, we must increase the magnitude of the input excess phase, $\varphi_{in}(t)$, until the bit error rate begins to rise. In other words, the phase error, $\Delta\varphi$, approaches π [= half unit interval (UI)], bringing the sampling edge of the clock close to the zero-crossing points of data. Thus, an approximate condition to avoid increasing the BER is as follows [17]:

$$|\Delta\varphi|_{\max} = |\varphi_{in}(t) - \varphi_{out}(t)|_{\max} \le \frac{1}{2}UI = \pi \tag{27}$$

The input signal is sinusoid waveform and can be expressed as follows:

$$\varphi_{in}(t) = -\varphi_{i,p}\sin(\omega_p t - \theta_0) \tag{28}$$

Where, $\sin\theta_0=\varphi_0/\varphi_{i,p}$. Our objective is to determine φ_0. According to [19],

$$\varphi_{out}(t) = \begin{cases} K_{VCO}(\frac{1}{2}\frac{I_p}{C_p}t^2 + R_p I_p t + \frac{I_p T_p}{4C_p}t) + \varphi_0, & -T_p/2 \le t < 0 \\ K_{VCO}(-\frac{1}{2}\frac{I_p}{C_p}t^2 - R_p I_p t + \frac{I_p T_p}{4C_p}t) + \varphi_0, & 0 \le t \le T_p/2 \end{cases} \tag{29}$$

$\varphi_{out}(t)$ at $0 \le t \le T_P/2$ can be simplified as

$$\varphi_{out}(t) = at^2 + bt - \frac{1}{2}aT_p t + \varphi_0 \tag{30}$$

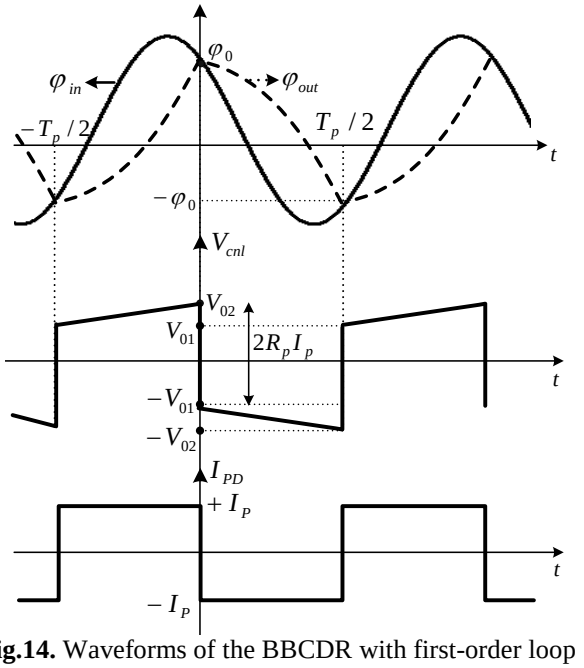


Fig.14. Waveforms of the BBCDR with first-order loop filter as jitter frequency exceeds loop bandwidth frequency.

where

$$a = -0.5K_{VCO}I_p/C_p \tag{31}$$

$$b = -K_{VCO}R_pI_p \tag{32}$$

According to Figure 14, since $\varphi_{out}(0) = \varphi_0 = -\varphi_{out}(T_P/2)$, using (30) we have

$$\varphi_0 = -a(\frac{T_p}{2})^2 - b\frac{T_p}{2} + \frac{1}{2}aT_p\frac{T_p}{2} - \varphi_0 \tag{33}$$

and,

$$\varphi_0 = -b\frac{T_p}{4} = -\frac{\pi}{2}\frac{b}{\omega_p} \tag{34}$$

Similar to the discussion of section (3.1), we consider only the fundamental term of $\varphi_{out}(t)$ from (13) as follows:

$$\varphi_{out}(t) \approx -\frac{a_1}{\omega_p^2}\cos(\omega_p t) - \frac{b_1}{\omega_p^2}\sin(\omega_p t) \tag{35}$$

Where, $a_1=-4I_PK_{VCO}R_p\omega_p/\pi$ and $b_1=-4I_PK_{VCO}/(\pi C_p)$. Using (31) and (32), a_1 and b_1 can be represented as follows:

$$a_1 = 4b\omega_p/\pi \tag{36}$$

$$b_1 = 8a/\pi \tag{37}$$

Therefore, by substituting (36) and (37) into (35), the approximate output phase can be rewritten as follows:

$$\varphi_{out}(t) \approx -\frac{4}{\pi}\frac{b}{\omega_p}\cos\omega_p t - \frac{8}{\pi}\frac{a}{\omega_p^2}\sin\omega_p t \quad (38)$$

Therefore, from (28) and (38) we get

$$\begin{aligned}\Delta\varphi &\approx \varphi_{in}(t) - \varphi_{out}(t)\\ &= (\varphi_{i,p}\sin\theta_0 + \frac{4}{\pi}\frac{b}{\omega_p})\cos\omega_p t\\ &\quad -(\varphi_{i,p}\cos\theta_0 - \frac{8}{\pi}\frac{a}{\omega_p^2})\sin\omega_p t\end{aligned} \quad (39)$$

From (28) and (34), $\varphi_{i,p}\sin\theta_0 = \varphi_0 = -\pi b/(2\omega_p)$ and we have

$$\varphi_{i,p}\cos\theta_0 = \varphi_{i,p}\sqrt{1-\frac{\varphi_0^2}{\varphi_{i,p}^2}} = \sqrt{\varphi_{i,p}^2 - \varphi_0^2} \quad (40)$$

Replacing φ_0 and (40) into (39), the phase error is obtained as follows

$$\begin{aligned}\Delta\varphi \approx &(-\frac{\pi}{2}\frac{b}{\omega_p} + \frac{4}{\pi}\frac{b}{\omega_p})\cos\omega_p t\\ &-(\sqrt{\varphi_{i,p}^2 - (\frac{\pi}{2}\frac{b}{\omega_p})^2} - \frac{8}{\pi}\frac{a}{\omega_p^2})\sin\omega_p t\end{aligned} \quad (41)$$

Thus, the maximum phase error is calculated as follows

$$\begin{aligned}|\Delta\varphi|_{\max} = [&(-\frac{\pi}{2} + \frac{4}{\pi})^2(\frac{b}{\omega_p})^2\\ &+(\sqrt{\varphi_{i,p}^2 - (\frac{\pi}{2}\frac{b}{\omega_p})^2} - \frac{8}{\pi}\frac{a}{\omega_p^2})^2]^{1/2}\end{aligned} \quad (42)$$

Equating $\Delta\varphi_{\max}$ to π yields the maximum tolerable input jitter can be obtained as follows

$$\begin{aligned}G_{JT} &= \varphi_{i,p}\\ &= \left[[\sqrt{\pi^2 - (\frac{b}{\omega_p}\frac{8-\pi^2}{2\pi})^2} + \frac{8}{\pi}\frac{a}{\omega_p^2}]^2 + (\frac{\pi}{2}\frac{b}{\omega_p})^2\right]^{1/2}\end{aligned} \quad (43)$$

The above equation contains two poles at the origin and two zeros. Consequently, as depicted in Figure (15), $|G_{JT}|$ falls at a rate of 40 dB/dec for $\omega_p<\omega_{p1}$ and at 20 dB/dec for $\omega_{p1}<\omega_p<\omega_{p2}$, approaching 1/2 UI [=π] for $\omega_p>\omega_{p2}$. The SONET mask is also plotted in this figure.

Equation (43) indicates that the jitter tolerance is proportional to VCO gain, CP current and filter resistor while inversely proportional to the smaller capacitor in the filter.

A comparison of the presented analysis with simulation results will be demonstrated in Section 5.

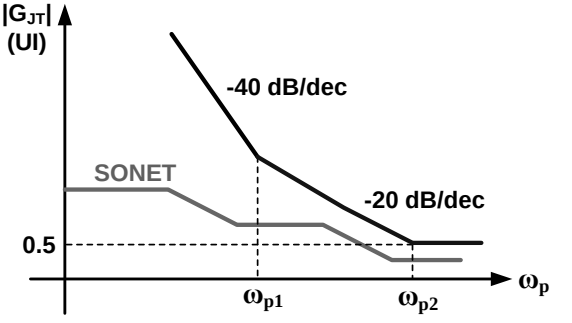


Fig.15. SONET jitter tolerance mask and jitter tolerance of a BBCDR.

4. TRANSISTOR LEVEL SIMULATION OF THE BBCDR

In order to validate the proposed analysis and modeling approach a BBCDR circuit operating at 2.5-Gb/s has been designed and simulated in 0.18-μm CMOS technology using HSPICE. The corresponding loop parameters are calculated using the design methodology described in Section 3. In this design, the CDR is designed for π input jitter amplitude although the loop parameters varied from design to design. Table 1 shows the parameter values of the designed BBCDR.

4.1. Alexander Phase Detector and V/I Converter

The D Flip-Flop (DFF) is the most important building block in a BBPD circuit. It is used in almost all practical phase detectors for retiming the data signal. A DFF is composed of two D latches connected in master/slave configuration, as illustrated in Fig. 16. (b). The clock signals into these two D latches are 180º out of phase. The latches in the PD are based on the topology depicted in Fig. 16.a [6]. Note that, all logic functions are designed based on current-mode logic (CML). The differential nature of CML makes it immune to power-supply variations and substrate noise. Since CML gates are biased at a constant current, no data-dependent current spikes are created on the power supply. For low-speed circuits, the tail current is decreased and the load resistors are increased to maintain a constant swing on the outputs. Fast rise/fall times for the high-speed gates are achieved by reducing load resistors. The tail current for these high-speed gates has to be increased correspondingly along with the differential-pair device sizes (higher g_m).

Fig. 17 shows the Alexander PD (followed by V/I converter) and the simulated characteristic in 0.18-μm CMOS technology for a data rate of 2.5 GB/s and a clock frequency of 2.5GHz. The phase detector characteristic can be yielded as the phase difference between data and clock varies in small steps. Figure (18) shows the differential V/I converter.

Table1. Designed BBCDR Loop Parameters

SONET	OC-48
f_C	2 MHz
C_p	400 pf
K_{VCO}	200MHz/V
a	-6.7×10^{13}
b	-23.7×10^{6}
I_p	270μA
R_P	0.5KΩ
R	140 Ω
L_p	1.5 nH

4.2. VCO

The VCO and the buffer are shown in Fig. 19. The VCO is an LC oscillator with accumulation-mode MOS varactors for frequency tuning. The buffer should provide desirable output common mode level and output swing for clock while isolating the VCO from PD. To determine ω_{osc}, each inductor is modeled by a simple parallel network of L_p and R, where R represents the loss. Defining $Q=R/L_p\omega_{osc}$, can be defined to have [7]

$$\omega_{osc}=\frac{1}{\sqrt{LC}}\sqrt{1-\frac{1}{Q}} \qquad (25)$$

In this design, the Q of inductor is approximately 7. Figure (19.c) shows the VCO tuning characteristic. The VCO provided a tuning range of 0.28 GHz. It can be seen that the VCO gain is approximately 200 MHz/V. Finally, BBCDR has been simulated based on the BBCDR architecture as shown in Figure (20). Table 2 gives the details of the simulated BBPD and VCO simulations.

Table2. Simulated BBCDR Parameters

K_{VCO}	≈ 200MHz/V
I_p	≈ 270μA

5. SIMULATION V.S. ANALYTICAL RESULTS

5.1. Jitter Transfer Simulations

In order to achieve the jitter transfer characteristic through simulation, input data was applied with sinusoidal jitter and varying amplitude at frequencies from 50 kHz to 30 MHz and at each jitter frequency, the output jitter amplitude is obtained by $\varphi_{out}=K_{VCO}\int V_{cnl}dt$ in lock state. For example, the jitter with an amplitude of 0.5UI and a frequency of 5MHz is applied as $\varphi_{in}=\pi\sin(2\pi\times5\times10^{6}t)$. Then, the magnitude of $\varphi_{out}(t) =K_{VCO}\int V_{cnl}dt$ is measured which equals $\varphi_{o,p}$=1.2rad. After that, the $\varphi_{o,p}/\varphi_{i,p}$ ratio is expressed in dB, that is $20\log(1.2/\pi)$= -8.35 dB. The output amplitude is also measured for other input frequencies in the same method and the $\varphi_{o,p}/\varphi_{i,p}$ ratio is expressed in dB. Jitter transfer characteristic is obtained through connecting these points. Figure (21) plots the theoretical and simulated jitter transfer of the designed CDR. This plot reveals a -20dB/dec roll-off in terms of jitter frequency. A comparison between transistor level simulations and calculated values shows the accuracy of analytical equations. The calculated and simulated angular frequency value of the designed CDR is summarized in Table 3. Also, Table 4 shows the jitter peaking values for different input jitter amplitudes for the designed example. As predicted, the jitter peaking is less than 0.1dB.

Table3. The calculated and simulated angular frequency

$\varphi_{i,p}$ (UI)	f_C	
	OC-48	
	calculated	simulated
0.5	2MHz	1.9MHz

Table4. The simulated jitter peaking for the designed example

$\varphi_{i,p}$ (UI)	Jitter Peaking (dB)
	OC-48
	simulated
0.5	0.02

5.2. Jitter Tolerance Simulation

Jitter tolerance is a measure of the CDR capability in tolerating the input jitter and is usually achieved by applying a sinusoidal jitter with different amplitudes at a given frequency range. Thus, input data is applied with sinusoidal jitter in lock state and then, at a given jitter frequency, the amplitude of the input jitter, $\varphi_{in}(t)$, is increased and $\Delta\varphi=\varphi_{in}(t)-\varphi_{out}(t)$ is obtain until the maximum phase difference become equal to π. Therefore, the maximum jitter amplitude, as a function of jitter frequency at which the maximum phase difference is equal to π, is called jitter tolerance. For example, for OC-48 $\varphi_{in}=\varphi_{i,p}\sin(2\pi\times110\times10^{3}t)$ is applied to input data in lock state and $\varphi_{i,p}$ is gradually increased until $\Delta\varphi_{max}=\pi$. It can be seen that, in $\varphi_{i,p}$=12UI=24π, $\Delta\varphi_{max}=\pi$ will take place. Therefore, the maximum tolerable input jitter amplitude for a jitter with the frequency of 110 KHz will be 12UI. This method is applied for different frequencies and the maximum tolerable $\varphi_{i,p}$ has been obtained for each frequency. The jitter tolerance curve is plotted by connecting these points. The simulated and calculated values of the maximum tolerable input jitter amplitudes for different jitter frequency are summarized in Table 5.

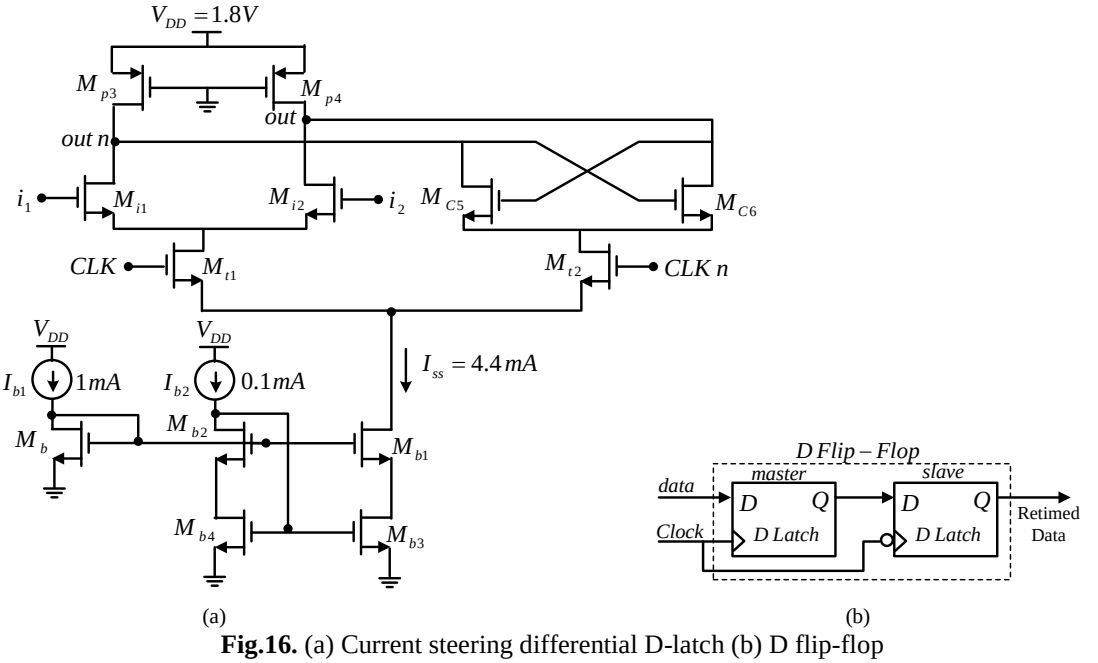


Fig.16. (a) Current steering differential D-latch (b) D flip-flop

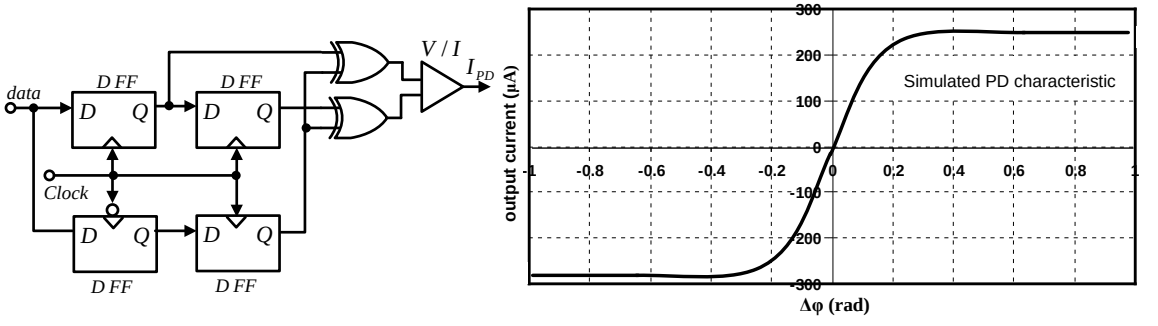


Fig.17. (a) Alexander PD. (b) Simulated characteristic at transistor level.

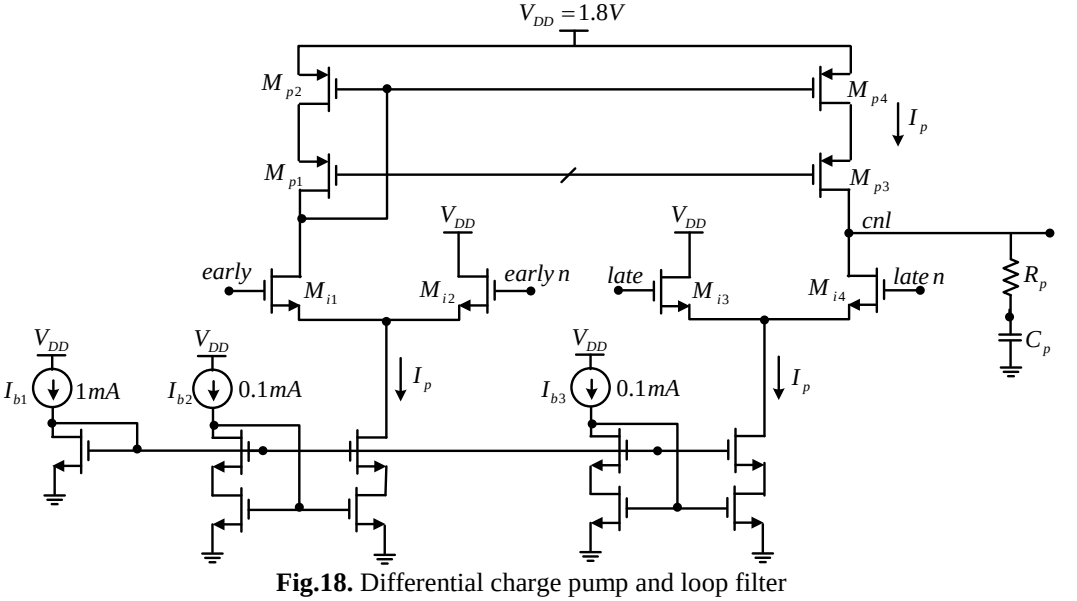


Fig.18. Differential charge pump and loop filter

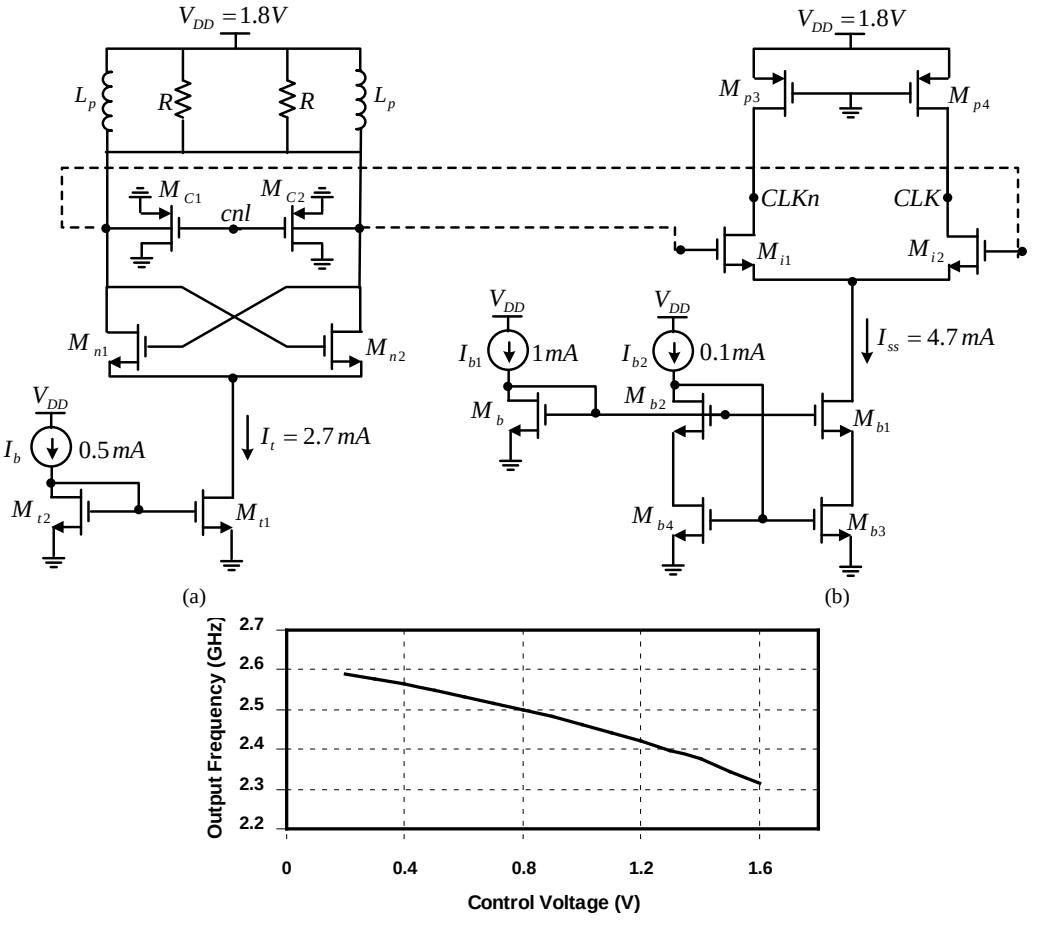


Fig.19. (a) LC cross-coupled VCO (b) Output buffer, (c) VCO tuning characteristic

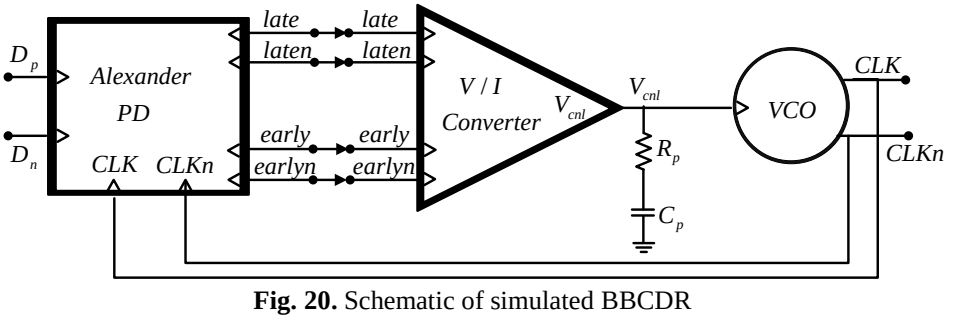


Fig. 20. Schematic of simulated BBCDR

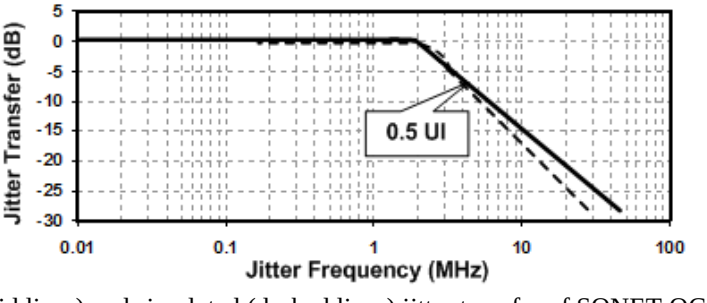


Fig. 21. Calculated (solid lines) and simulated (dashed lines) jitter transfer of SONET OC-48 for φi,p=π=0.5UI.

Table5. Summary of the simulated and calculated Results

$\varphi_{i,p}$ (UI)	The frequency at which $\Delta\varphi_{max}=\pi$	
	OC-48	
	calculated	simulated
15	195KHz	90KHz
12	225KHz	110KHz
8	275KHz	150KHz
2	750KHz	580KHz
1	1550KHz	1350KHz

The calculated values of the jitter frequency are given by (24). Figure (22) shows the theoretical and simulated jitter tolerance of the designed CDR. As seen; the good agreement between the closed-form analytical expression (23) and the transistor level simulation results confirms the present analysis. Note that, the specification of jitter tolerance is compared by a mask as a function of the jitter frequency. Thus, the SONET mask for OC-48 is also shown in Figure (22), which shows that the SONET mask is satisfied.

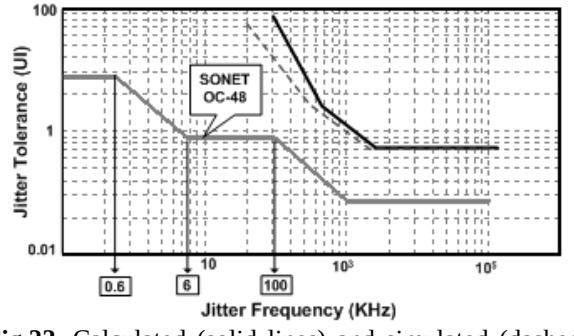


Fig.22. Calculated (solid lines) and simulated (dashed lines) jitter tolerance of SONET OC-48.

6. CONCLUSION

Clock and data recovery (CDR) circuit using bang-bang phase detector (BBPD) are widely used in communication systems mainly because of their high-frequency capabilities. However, bang-bang clock and data recovery (BBCDR) circuits are hard nonlinear systems due to the nonlinearity introduced by the binary phase detector (BPD). In this paper, first, architecture of BBCDR circuits is stated in addition to expressing basic concepts of clock and data recovery circuits. Since characteristics of frequency response of CDR are determined by jitter tolerance and jitter transfer characteristics, concepts of these characteristics are mentioned and the presented analyses are evaluated. The presented method is generally enough to be used for design of the BBCDR. The accuracy of the presented expressions is verified through transistor level simulation. Based on the presented tables and figures, it is clear that the results in this work would help designers to optimize the jitter performance of the BBCDR in system level design.

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