Design and simulation of an Improved NEMFET with Low Leakage Current and Sub-Threshold Swing

Nastaran Jafari[1], Farshad Babazadeh[2*], Zahra Ahangari[3]
1- Department of Electrical Engineering, Yadegar-e-Emam Khomeini (RAH) Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.
Email: n.jafari.web@gmail.com
2- Department of Electrical Engineering, Yadegar-e-Emam Khomeini (RAH) Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.
Email: babazadeh@iausr.ac.ir (Corresponding author)
3- Young Researchers and Elite Club, Yadegar-e-Emam Khomeini (RAH) Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.
Email: Zahra_ahangari@iausr.ac.ir

Received: September 2018 Revised: October 2018 Accepted: November 2018

ABSTRACT:
In this paper design and simulation of an improved depletion-mode n-channel nanoelectromechanical field effect transistor (NEMFET) at 300K is reported. The designed NEMFET is based on NEMS technology and fully compatible with CMOS fabrication process. A NEMFET is composed of a NEM relay and a MOSFET and comprises a movable gate and a semiconductor part, so that the flowing current is always in the semiconductor part. The nanomechanical movable gate was a bossed doubly clamped beam and simulated by COMSOL Multiphysics software and the electrical part was designed and simulated by ATLAS software. The designed NEMFET had a 25 nm length, 100 nm width and 5.2 nm thicknesses. Optimization was done by applying two 8.5 nm spaces, one between source to gate and the other between gate to drain. Simulation results show in the proposed structure, sub-threshold swing was decreased to 86 mV/dec and the I_{on}/I_{off} ratio was increased to 8.68×10^4.

KEYWORDS: Field Effect Transistor, NEM Relay, NEMFET, Nanoelectromechanical Systems**.**

1. INTRODUCTION

Sub-threshold swing limitation in conventional field effect transistors current is related to drift and diffusion mechanism and determines the minimum sub-threshold swing of 60mV/dec. Among of important parameters to determine performance of a transistor is its sub-threshold swing, so that, lower sub-threshold swing leads to higher performance. In the sub-threshold region, drain current is controlled by the gate. Sub-threshold swing is calculated from (1):

$$SS = ln(10)\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right) \quad (1)$$

To decrease short-channel effect and increase the gate control in FETs, it is needed to increase gate oxide capacitance. To increase this capacitance, dielectric thickness must be thinner or its dielectric constant should be greater. According to (1), when C_{ox} tends to infinity, FET sub-threshold swing is limited to 60mV/dec in 300K [1, 2]. Moreover, Static power consumption is also one of challenging of MOSFET scaling; which one of the major reasons is power consumption due to high off-state leakage current I_{off} in transistors [3].

This article describes an optimized depletion-mode n-channel NEMFET transistor with 25 nm gate length contains two spaces equal to 8.5 nm (ΔL) between source to gate and gate to drain. Typically, a NEMFET has a leakage current 100 times less than a MOSFET. So, logic circuits based on NEMFETs are suitable to implementing ultra-low power processors and operational units [4]. Abruptly switching characteristic is another property of a NEMFET [5]. Simple structure, switching, and NEMFET power issues can lead to the replacement of conventional MOSFETs in the implementation of future VLSI circuits [6].

2. STRUCTURE DESCRIPTION AND NEMFET ANSISTORS FUNCTION ANALYSIS

In Fig. 1 the structure and size of the proposed NEMFET transistors is shown. This transistor is composed of two mechanical NEM relay and electrical MOSFET. The mechanical part includes of a bossed doubly clamped beam and operates as a suspended gate

with 10 nm thickness. As shown in Fig. 1, the beam is separated from a thin dielectric by an air gap-spacing. To optimization, two spaces of ΔL between source to gate and gate to drain have been created. According to Fig. 2 (a), when the gate voltage is zero, the transistor will be in off-state and the air gap-spacing x is equal to zero. While in on-state (Fig. 2 (b)), suspended gate is located from thin dielectric with a distance of 1 nm. It is assumed that the gate electrode is attached to the channel firmly at two sides, resulting in the doubly-clamped beam (with spring constant k) is suspended over the channel. To reduce adhesion between the gate and the channel when gate is lowered, the NEMFET must be located in a vacuum [3]. It is noteworthy that the average potential of the channel in the electromechanical model is considered to be $V_{ds}/2$. In all simulations carried out, the displacement d in the gate voltage Vg=1V is zero and the maximum air distance x is equal to 1 nm. By lowering the gate voltage, the gate plate approaches the channel and the air gap x decreases.

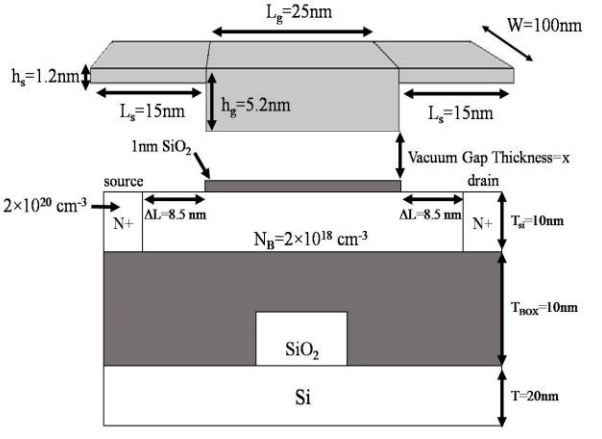

Fig. 1. Cross-section of the NEMFET structure used in the simulations.

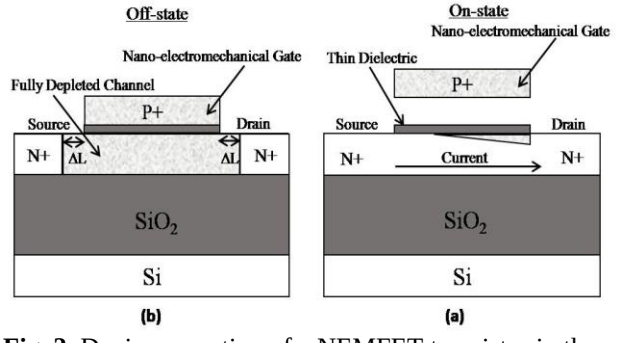

Fig. 2. Device operation of a NEMFET transistor in the (a) On state (b) Off state.

3. DESIGN OF THE SUSPENDED GATE NEM RELAY

NEM relay with suspended gate is a bossed doubly clamped beam with dimension of h=1.2 nm, W=100 nm and L=15 nm for lateral supporting beams and dimensions of h=5.2 nm, W=100 nm and L=25 nm for the proof mass (boss) all made of polysilicon. Displacement of the suspended gate simulated by COMSOL Multiphysics software [7] is shown in Fig. 3.

Considering supporting beams spring constant k, displacement is highly dependent on its thickness and length. A beam with longer in length and thinner in thickness leads to lower stiffness and higher flexibility.as a result, the supported beams will further deflected and central section of the gate (boss) not deflected. Then, gate can be moved easily towards up and down. In contrast, in the thicker and shorter beams, deflection will be difficult. In order to uniform distribution of electrostatic force along the beam and ignoring remained stress, spring constant k is defined as (2), [8]:

$$k = \frac{32EWh^3}{L^3} \tag{2}$$

Where E is the Young's modulus, h is the thickness, W is the width and L is the gate length. Pull-in voltage in capacitive structures is calculated from (3), [9]. By increasing the pull-in voltage, the beam is deflected further downward. In situation which x equals to 2/3 x_0, the beam loses its stiffness and gate collapses to the dielectric abruptly.

$$V_{pi} = \sqrt{\frac{8kx_0^3}{27\varepsilon_{gap}WL}} \tag{3}$$

Where W is the width of suspended gate, L is the gate length, ε_{gap} is permittivity of the air gap, k is stiffness of the suspended gate and x_0 is the initial air gap spacing. By increasing gate voltage (V_g) from 0 to 1 V for two voltage V_{ds}=0 V, V_{ds}=1 V air gap (x) is increased proportional to applied voltage. In Fig. 4, dependence of air gap x on gate voltage is shown.

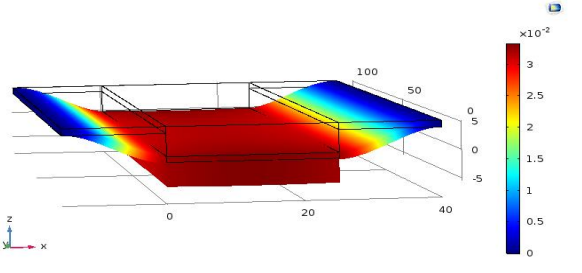

Fig. 3. Displacement of the doubly clamped beam simulated in COMSOL Multiphysics

4. DESIGN OF ELECTRICAL PART (MOSFET)

The electrical part includes a MOSFET transistor with a difference that in order to compromise between on-state and off-state currents, two spaces (ΔL) between source to gate and gate to drain are included which further decrease of the off-state current, while increasing the on-state current. Simulation results with ΔL from 7 nm to 10 nm are shown in Fig. 5. As it is obvious in figure 5, the 8.5 nm space is the most appropriate value, and this optimal amount has been used in all of simulations.

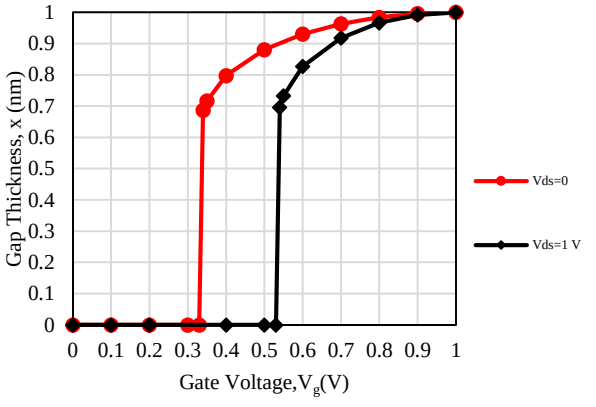

Fig. 4. Dependence of air gap-spacing x on gate voltage for V_{ds}=0 V and V_{ds}=1 V.

In order to determine the electrical characteristics of the NEMFET transistor, First, for different gate voltages and V_{ds} = 1 V, the air gaps (values of x) were extracted from COMSOL Multiphysics software, then simulated by ATLAS software, which is a subset of the SILVACO software [10]. The transfer characteristic of I_{ds}-V_g is shown in Fig. 6. Also, transfer characteristic of I_{ds}-V_{ds} is shown in Figure 7.

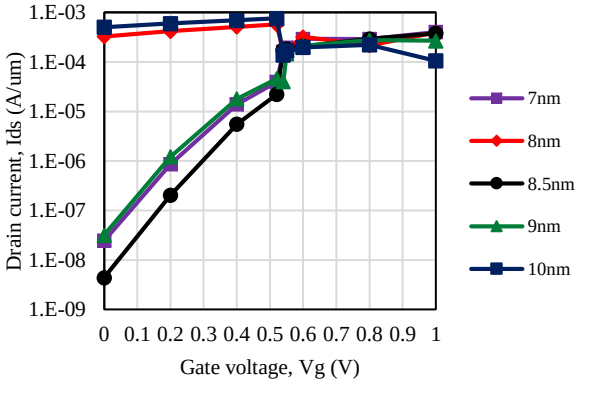

Fig. 5. Drain current vs. gate voltage for ΔL values of 7 nm, 8 nm, 8.5 nm, 9 nm, 10 nm for V_{ds}=1 V.

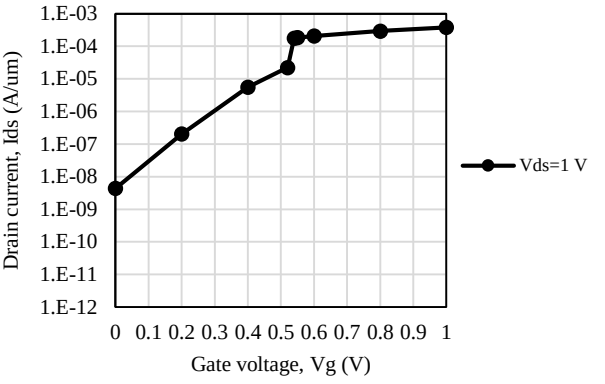

Fig. 6. I_{ds}-V_g transfer characteristics of the simulated NEMFET transistor.

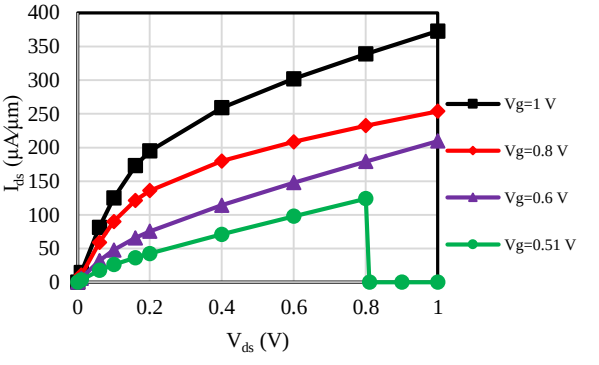

Fig. 7. Output characteristics of I_{ds}-V_{ds} for the simulated NEMFET transistor.

5. CONCLUSION

In this paper, electrical characteristics of an improved NEMFET transistor with gate length of 25 nm and two gap spaces of ΔL=8.5 nm between gate and source and gate to drain were studied and simulated by COMSOL Multiphysics and ATLAS in two mechanical and electrical part. The suspended gate causes a abruptly movement in mechanical beam (gate electrode) and as a result, decreasing the sub-threshold swing and increasing the I_{on}/I_{off} ratio. By considering the Simulation results and including effects of ΔL, sub-threshold swing and I_{on}/I_{off} ratio for 4 NEMFET transistor, common MOSFET, NEMFET and MOSFET including ΔL with same dimensions for V_{ds}=1are shown in Fig. 8 and Fig. 9 respectively. The simulation results show decreasing off-state current (I_{off}), and as a result decreasing power consumption, increasing the on-state to off-state current (I_{on}/I_{off}) up to 8.68×10^{4} and achieving sub-threshold swing equal to 86 mV/dec for NEMFET transistor with ΔL. According to the results, the NEMFET transistor with ΔL can be considered as a suitable replacement for the MOSFET transistor.

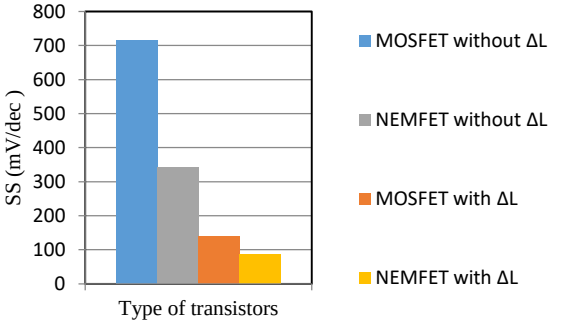

Fig. 8. Average sub-threshold swing for channel thickness of 10 nm in four different transistors with same dimensions for V_{ds} =1 V.

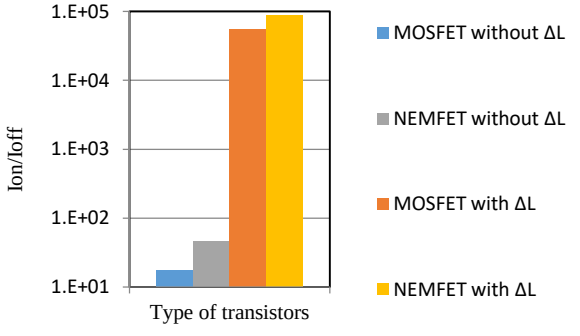

Fig. 9. I_{on}/I_{off} ratio for channel thickness of 10 nm in four different transistors with similar dimensions for V_{ds} =1 V.

REFERENCES

[1] Karnik,Tanay, and Peter Hazucha, **"Characterization of Soft Errors Caused by Single Event Upsets in CMOS Processes,"** *IEEE Transactions on Dependable and Secure Computing* 1.2, pp. 128-143, 2004.

[2] Takeda, E., Kume, H., Toyabe, T., & Asai, S,. **"Submicrometer MOSFET Structure for Minimizing Hot-Carrier Generation,"** *IEEE Transactions on Electron Devices*, Vol. 29(4), pp. 611-618.I.S, 1982.

[3] Kam, Hei, et al, **"A New Nano-Electro-Mechanical Field Effect Transistor (NEMFET) Design for Low-power Electronics,"** *IEEE International Electron Devices Meeting. IEDM Technical Digest*. IEEE, 2005.

[4] Enachescu, Marius, et al. **"Ultra low power NEMFET based logic,"** *IEEE International Symposium on Circuits and Systems (ISCAS2013)*. IEEE, 2013.

[5] Enachescu, Marius, et al. **"Low-Leakage 3D Stacked Hybrid NEMFET-CMOS Dual Port Memory,"** *IEEE Transactions on Emerging Topics in Computing*, 2016.

[6] Haldar, Ritwik, Koushik Guha, and Srimanta Baishya. **"Effect on Pull-in Voltage and Current in NEMFET by Scaling Channel Length,"** *TENCON IEEE Region 10 Conference. IEEE*, 2015.

[7] *COMSOL* Multiphysics® version *5.2a*.

[8] Osterberg, P., Yie, H., Cai, X., White, J., & Senturia, S, **"Self-consistent Simulation and Modelling of Electrostatically Deformed Diaphragms,"** *In Micro Electro Mechanical Systems, MEMS'94, Proceedings, IEEE Workshop on* pp. 28-32, 1994.

[9] Kim, J. H. , **"Near Zero Sub-threshold Swing Nano-Electro-Mechanical Field Effect Transistor with Suspended Germanium/Silicon Core/Shell Nanowire Channel."** University of California, San Diego, 2013.

[10] ATLAS User Manual, Santa Clara, USA: Silvaco International, 2015.