Fault Tolerant Design of QCA Binary Wire

Mojdeh Mahdavi[1*], Mohammad Amin Amiri[2]
1- Department of Electronics, Shahr-e-Qods Branch, Islamic Azad University, Tehran, Iran.
Email: m.mahdavi@qodsiau.ac.ir (Corresponding author)
2- Department of Electronics, Malek Ashtar University of Technology, Tehran, Iran.
Email: maamiri@mut.ac.ir

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ABSTRACT:
Dependability of a circuit is among the most important issues in the design process and reliability concerns are associated with the digital system design. A fault tolerant system should have the ability to detect, locate and correct the error and recover the system to normal operational conditions. It is more important to use fault tolerant gates in nano scale digital circuits because by decreasing the device dimensions the influence of external factors and therefore the probability of fault occurrence will increase. Since the binary wire is an essential part of digital systems and especially QCA (Quantum Cellular Automata) circuits, a redundancy based fault tolerant technique is presented in this paper to improve the fault tolerance of this part. The efficiency of this method is evaluated by MATLAB software. Results show that the fault tolerance of binary wire will significantly increase by using the proposed method. The hardware redundancy of this method is about 100% which is much less than TMR (Triple Module Redundancy) methods by more than 200% redundancy.

KEYWORDS: Quantum Cellular Automata, Fault Tolerance, Binary Wire.

1. INTRODUCTION

With the increasing development of technology and Moore's theory of shrinking the minimum feature size of transistors to sub atomic dimensions, achieving to higher speeds and density and less power consumption has been restricted. Quantum effects are of these restrictions which happen in sub-micron CMOS technology. Because of the extreme limitations in continuous shrinking of existing technologies, new methods and techniques should be developed for the production of logic circuits. These circuits should be sized in molecular dimensions and therefore the fabrication technology of digital circuits has tended to nano scale dimensions.

The quantum cellular automata which was first proposed by Lent et al. [1], is based on the movement of electric charge inside a cell and is a good nanotechnology alternative for microelectronic circuits. QCA cells have quantum dots in which the electrons positions will specify the binary level zero or binary level one. Determination of logic levels by electron placement in quantum dots is the distinctive feature of QCA circuits in comparison with CMOS circuits. By this concept, no current will flow among circuit devices and hence the power consumption will dramatically drop. Fig. 1 illustrates the QCA cell, its ground states and corresponding logic levels of '0' and '1' and four positions which electrons may occupy.

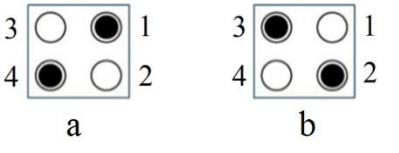

Fig. 1. QCA cell, its ground states and corresponding logic levels and four positions of electrons. (a) Logic level '1'. (b) Logic level '0'.

It should be note that reducing the device dimensions will increase the fault sensitivity of digital circuits. Nano scale devices and circuits are more sensitive and have further reactions to external stimuli such as radiation, temperature, etc. It is obvious that conventional fault tolerant techniques are not efficient in nano scale circuits. Therefore, along with advances in nanotechnology, investigations of fault tolerance of nano circuits are also continued and more attention is focused on proposing the new fault tolerant methods [2].

Different types of defects may occur during the production of QCA devices and circuits. Some of these previously investigated defects are mentioned below. Cell displacement, is a defect in which the defective cell is shifted from its original location [2]. The defective cell may be placed outside the radius of influence of its neighbors and may be polarized by

different value. Cell misalignment, is a defect in which the defective cell is not properly aligned with other cells [3], [4]. Cell omission, is a defect in which the defective cell is eliminated from its location and its position is vacant [5]. This defect may influence the logic level of the QCA circuit. Cell rotation, is a defect in which the defective cell is twisted around its original position [6], [7]. This defect may cause the defective cell to be not completely polarized and therefore may lead to circuit malfunctioning. Single electron cell, is a defect in which the defective cell has one electron instead of two electrons [8]. This defect leads to circuit malfunctioning. Single event upset (SEU) is a potential creator of this defect [9].

SEU is a phenomenon in which a microscopic effect can influence QCA devices and circuits and lead to generation of a macroscopic fault. These phenomena can force electrons to tunnel inside or outside of a QCA cell and hence the faulty cell may have invalid number of electrons. Considering the QCA cells which have two electrons inside themselves, it is obvious that defective cells can lead to incorrect polarization and the logic value of circuit may change.

The main goal of this paper is to introduce a method to improve the fault tolerance of binary wire in presence of single electron fault. A redundancy based method is proposed to retrofit the binary wire against the mentioned fault. Redundancy techniques are related to usage of additional resources (Hardware, Software or Information) or additional usage of available resources (Time). Previous fault tolerant techniques for QCA circuits are mainly constructed on triple redundancy basis [10-12], but this paper is based on double redundancy. In addition to less hardware usage of the proposed method, the binary wire is completely tolerant against single electron fault. The MATLAB software is used to simulate the defect effects in simple binary wire and fault tolerant binary wire. Section 2 will investigate the effect of single electron fault on binary wire. Section 3 explains the method to improve the fault tolerance of binary wire. Section 4 investigates the simulation results and section 5 will conclude the paper.

2. REVIEW OF FAULT MODELING IN QCA BINARY WIRE

These phenomena can force electrons to tunnel inside or outside of a QCA cell and hence the faulty cell may have invalid number of electrons. Initially, the defective cell with a single electron is stimulated by the previous cell at logic zero and one and the position of the single electron in the defective cell is calculated. The simulation results are presented in Table 1. The results were obtained using the Coulomb energy equation [9]. Electron position and cell polarization are derived from the minimum coulomb energy as mentioned in (1), where q_i and q_j are electron charge, ε_0 is vacuum permittivity, and ε_r is the relative permittivity of the material that is used for the construction of cell which is assumed to be gallium arsenide. Simulation results are utilized to evaluate the situations, and all the simulations have been performed with MATLAB [9, 13].

$$E_{i,j} = \frac{q_i q_j}{4\pi\varepsilon_0\varepsilon_r\left|r_i - r_j\right|} \quad (1)$$

Depending on the position of the electrons of the previous cell, the single electron in the defective cell may occupy one of the four quantum dots which are available positions. Among these four quantum dots, the electron will occupy a position to impose minimum Coulomb energy to the system. As illustrated in Table 1 [9], the logic value of zero for the stimulating cell will force the electron to occupy the number one position in the defective cell, because the results show that the lowest energy is imposed to binary wire in this position. The logic value of one for the stimulating cell will force the electron to occupy the number two position in the defective cell. Because the results show that the lowest energy is imposed to binary wire in this position. The steady state for placement of electrons is the lowest energy state. All values in the Tables are expressed in milli electron volts (meV).

Table 1. Electrostatic energy for positions of electrons in a faulty cell according to its previous cell polarization.

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	0.0089	0.0092	0.0152	0.0134
One	0.0092	0.0089	0.0134	0.0152

After finding the position of the single electron in defective cell, we should reasonably determine the polarization of the next cell. For the second case, the simulation results show that if the electron of a defective cell is in position 1 or 2, the next cell will obtain the polarization one and polarization zero respectively. Coulomb energy is calculated for each polarization and the polarization with the minimum Coulomb energy is considered as target polarization. Coulomb energy of each polarization is shown in Table 2. It can be concluded from Table 1 that positions 3 and 4 in the defective cell cannot be occupied by single electron, but in order to have the complete simulation results, these two states are also presented in Table 2.

Fig. 2 shows the effect of presence of a defective cell in a binary wire. As illustrated in Fig. 2a, if the left side cell has the logic value of zero, the single electron in

the defective cell will be placed in position 1 and the right side cell will obtain the logic value of one and as shown in Fig. 2b, if the left side cell has the logic value of one, the single electron in the defective cell will be placed in position 2 and the right side cell will obtain the logic value of zero. Simulation results show that a single electron fault occurrence in a binary wire will lead to a logic value inversion of that wire [9], [13].

Table 2. Electrostatic energy for polarization of next cell according to the position of electron in faulty cell.

Faulty Cell Position	Next Cell Polarization Zero	Next Cell Polarization One
Position 1	0.0152	0.0134
Position 2	0.0134	0.0152
Position 3	0.0089	0.0092
Position 4	0.0092	0.0089

Investigation of this fault in QCA is important because the separated electron (several factors may cause an electron leave its original location) from the QCA cell, do not have the required energy to return to its original place. Therefore, a defect which can cause transient fault in CMOS circuits may cause a permanent fault in QCA circuits. Now, some methods should be developed to improve the resistance of these circuits against such defects.

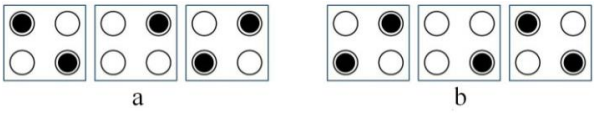

Fig. 2. Faulty cell effect on binary wire. (a) Stimulating cell with logic level '0', Single electron in position 1 and next cell polarized to logic level '1'. (b) Stimulating cell with logic level '1', Single electron in position 2 and next cell polarized to logic level '0'

3. FAULT TOLERANCE OF QCA BINARY WIRE

To increase the fault tolerance of single electron faults in the binary wire, the double redundancy method has been used which is not so far used to strengthen the QCA basic gates. In this way, the probability of single electron faults propagation in the binary wire will be reduced to zero. As seen in Fig. 3, in this method, two binary wires are coupled to each other. To investigate all possible error scenarios, four cases must be considered. In each case, the effect of previous cell on the defective cell must be examined and then the effects of the defective cell on subsequent cell should be analyzed.

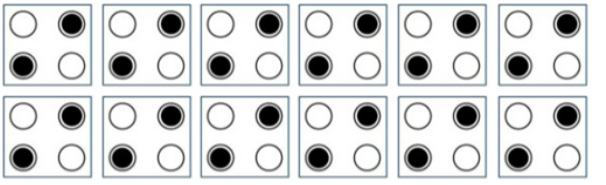

Fig. 3. Double redundancy technique for binary wire.

In the case that the input of binary wire is one and the defective cell in the upper binary wire or the lower binary wire, the simulation results are shown in Table 3. The simulation results for the case that the binary wire has a "0" input and the defective cell is in the upper or lower binary wire, is illustrated in Table 4. The single electron in the defective cell is placed in a location with the lowest electrostatic energy with other electrons in neighbor cells. As an example, in the case that the binary wire has a "1" input and the defective cell is in the lower binary wire, simulation results show that the single electron in the defective cell will occupy the position 2, as illustrated in Fig. 4b.

Table 3. Electrostatic energy for positions of electrons in a faulty cell for logic level '1' and upper or lower position of faulty cell.

Previous Cell Logic	Position 1	Position 2	Position 3	Position 4
'1' and Upper defective cell	111.9	118.9	124.8	118.9
'1' and Lower defective cell	119.7	113.7	119.7	129.7

And in the case that the binary wire has a "0" input and the defective cell is in the lower binary wire, simulation results show that the single electron in the defective cell will occupy the position 2. In this location, the single electron in defective cell has the lowest electrostatic energy with other electrons in neighbor cells. This can be seen in Fig. 4a. After determining the position of electron in the defective cell as illustrated in Table 3 and Table 4, the polarization of next cells should be investigated.

Table 4. Electrostatic energy for positions of electrons in a faulty cell for logic level '0' and upper or lower position of faulty cell.

Previous Cell Logic	Position 1	Position 2	Position 3	Position 4
'0' and Upper defective cell	113.7	119.7	129.7	119.7
'0' and Lower defective cell	118.9	111.9	118.9	124.8

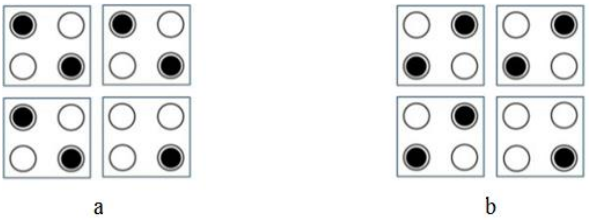

Fig. 4. Electron position in case of lower defective cell. (a) Previous cell with logic level ‘0’ with the faulty cell in the lower binary wire and the single electron in position 2. (b) Previous cell with logic level ‘1’ with the faulty cell in the lower binary wire and the single electron in position 2

Table 5 shows the polarization of next cells, when the input of binary wire is "1" and "0" and the defective cell is located in the upper or lower binary wire. As it can be seen, all four states for two cells after the defective cell have been investigated. As concluded from the results, in the case that the binary wire has a "1" input, even with the defective cell existence in the transmission flow of data, the output of binary wire will not change and remain "1" and when the binary wire has a "0" input, the output of binary wire will not change and remain "0". For example, two faulty modes and the impact of defective cell on the output are shown in Fig. 5.

Table 5. Electrostatic energy of next cells for different logic levels and upper or lower position of faulty cell.

Next Cell Logic	‘0’ ‘0’	‘0’ ‘1’	‘1’ ‘0’	‘1’ ‘1’
‘1’ and Upper defective cell	121.8	121.3	123.2	119.7
‘1’ and Lower defective cell	119.2	121.5	119.7	118.9
‘0’ and Upper defective cell	118.9	121.5	119.7	119.2
‘0’ and Lower defective cell	119.7	121.3	123.2	121.8

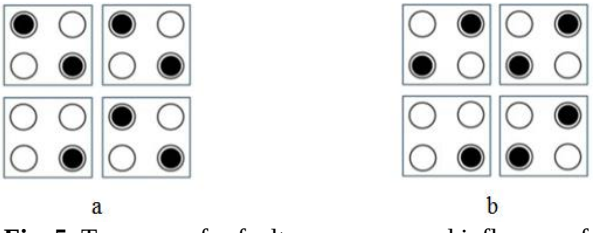

Fig. 5. Two cases for fault occurrence and influence of defective cell on the output logic. (a) The faulty cell in the lower binary wire and the logic level ‘0’ for the upper binary wire will polarize the next cells to logic level ‘0’. (b) The faulty cell in the lower binary wire and the logic level ‘1’ for the upper binary wire will polarize the next cells to logic level ‘1.’

Thus, using the described method and in the case of double redundancy for binary wire, the existence of defective cell in the upper or lower binary wire will not lead to error propagation and reduction of the system robustness, in other words the binary wire is now resistant against single electron fault. Full results of the simulation of single electron fault tolerance in the wire binary can be seen in Fig. 6.

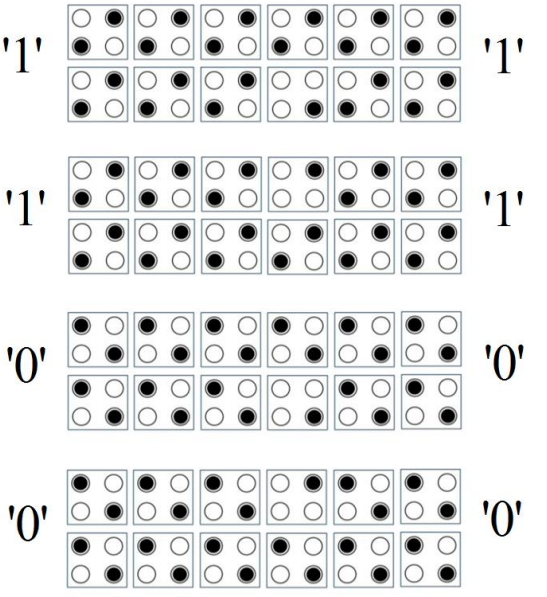

Fig. 6. Full modeling of single electron fault in double redundant binary wire.

4. DISCUSSION ON SIMULATION RESULTS

One of electrons in the QCA cell can be diverted from its original location due to various factors and could result in QCA cell having a single electron. It should be mentioned that the separated electron does not have enough energy to return to its original position. Therefore, such fault that causes a transient error in CMOS circuits can cause a permanent fault in QCA circuits. It is required to find a way to increase the resistance of these circuits against such permanent faults.

Due to the significance of fault tolerance in digital circuits, different methods have been developed to increase the endurance of such circuits and have been investigated in various papers, among which N-module redundancy and particularly, tile structure can be mentioned which have provided exceptional capabilities for gates in this technology [14-19]. For improvement of different types of combinational circuits in this technology, several methods have been proposed for cell misalignment or missing cell faults [20-23].

Double module redundancy has been used in this paper to increase the fault tolerance of QCA binary wire against single-electron fault. This method fully tolerates the QCA binary wire against the single-electron fault.

By investigating the results of the simulation of double module redundancy and comparing the results with the mentioned papers, we conclude that double module redundancy method reduces the circuit complexity and increases the reliability of binary wire compared to the previous conventional methods, among which triple modular redundancy is the most popular. The hardware redundancies of this method is about 100% which is much less than triple module redundancy method by more than 200% hardware redundancy.

5. CONCLUSION

Fault tolerance techniques are playing an important role in designing digital systems and these techniques are improving continuously. The vulnerabilities in digital circuits, especially in nano scale circuits may cause the system to malfunction during the normal operation. There are threats for system operation that illustrate the necessity of fault tolerant circuit's existence. A redundancy based technique is used in this paper to improve the fault tolerance of QCA binary wire. It is illustrated that the proposed method has completely removed the fault effects and its circuit complexity and hardware redundancy are much less than conventional methods.

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