A Novel Approach for Low Phase Noise Voltage Controlled Oscillator Design based on TSMC 0.18 um Technology

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Received: September 2020 Revised: November 2020 Accepted: January 2021

ABSTRACT:
In this paper, a new structure of Voltage Control Oscillator (VCO) to reduce the phase noise using two plans of a variable voltage capacitor is proposed. The aim of the current paper is to analyse two structure of a completely integrated 3.7 GHz LC-VCO based on TSMC 0.18 um technology. In the first plan for different voltages with variable voltage capacitors in this circuit can be achieved to a suitable phase noise of about 125 dB per Hz and in the second plan, a noise of -123 dB per Hz is achieved in the deviation frequency of 1 MHz. Also, the Figure of Merit (FOM) values for the first plan of -4/186 and for the second plan of –4/184 are achieved and the power consumption is 10 mW.

KEYWORDS: Voltage Control Oscillator, Phase noise, Figure of Merit, TSMC.

1. INTRODUCTION

Voltage controlled oscillators are applied in telecommunication systems. Most telecommunication systems now use the inactive elements on the chip in their oscillator structure [1, 2]. Two types of oscillators on the chip include ring oscillators and LC oscillators. In order to select the type of oscillator, after determining the scope of the oscillator, requirements such as power consumption, silicon consumption rate, and phase noise will be considered. For example, it is clear that the proper oscillator architecture is the use of LC oscillators for frequency synthesizers. These oscillators can have a good phase noise at microwave frequencies [2]. Ring oscillators have a simpler structure than LC oscillator. Ring oscillator properties include low power consumption, low silicon consumption and high adjustment range. The inadequacies of these oscillators may be due to the inadequacy of phase noise in Gigahertz frequencies [3]. A method for reducing phase noise in a VCO is to use a cross-coupled series LC receiver [4, 5]. Another way to reduce the phase noise in the LC VCO is to use the Switch Current Source. Using this method, the current duty cycle decreases [6]. One of the important parameters of VCO is low power, low phase noise, wide tuning frequency band, tuning linearity and low area occupation [4]. One of the important applications of VCO is their application in PLL circuits, telecommunication systems, Wireless Local Area Network (WLAN), GPS receivers, Wireless Personal Area Network (WPAN) and IEEE 802.11g standard applications [7-10].

One of the ways to increase the tuning frequency band of VCO is the use of Switched-Inductor and Switched-Capacitor [8]. One of the common ways to enhancement the tuning frequency band is to use the switched capacitors [11]. During these years, several methods for implementing this technique are presented in accordance with the IEEE 802.11g standard [9, 10]. There is a conciliation between tuning linearity and the tuning frequency band [12]. Recently the application of millimeter wave (mm-wave) applications has developed in broadband circuits. The III-V or SiGe technology is used is used in mm-wave VCO [13]. Another VCO design approach for broadband users is using quadrature VCO (QVCO), which consists of serially coupled. In this VCO, SiGe heterojunction bipolar transistors are used in QVCO for oscillation [14, 15]. In order to achieve low phase noise and large output swing in QVCO the p-core indirect back-gate coupled Technique is used [16], this method can access a strong coupling trans conductance for a quadrature phase [16]. Another way to develop the tuning frequency band of low phase noise oscillators is to use a higher order tank circuit that is implemented by transformers on the chip [17]. Therefore, tank-based circuit-based oscillators show higher potentials for use in broadband applications and multiple band applications [18]. One of the methods to reduce the area occupation and phase noise in the VCO, a helical

Paper type: Research paper
DOI: https://doi.org/10.29252/mjtd.10.1.17
How to cite this paper: F. Setoudeh, N. Nouri, **"A Novel Approach for Low Phase Noise Voltage Controlled Oscillator Design based on TSMC 0.18 um Technology"**, *Majlesi Journal of Telecommunication Devices*, Vol. 10, No. 1, pp. 17-22, 2021.

inductor based filtering technique is used [19 20]. To achieve wide-frequency band and low phase noise, a dual-mode VCO based on mm-wave topology is designed using parasitic capacitances of cross-coupled pair to sense dual-mode operation [21]. In [22], a LC push pull VCO is designed to attain a wide frequency range in the Ku and Ka bands. This paper presented a new structure of VCO to reduce phase noise in the c frequency band. For this reason, we will first introduce the structure of a variable capacitor with a new voltage for applications of voltage controlled oscillators.

2. DESIGN AND ANALYSIS OF PROPOSED VOLTAGE CONTROL OSCILLATOR

Fig. 1 shows a circuit of Ordinary oscillator. In order to analyse this circuit, it is necessary to obtain the differential amplifier equivalent resistance seen from both X and Y. As shown in Figure 1, it can be proven that the equivalent resistance seen from both X and is equal to:

$$-V_{gs2} + V_{YX} + V_{gs1} = 0 \xrightarrow{V_{gs1}=-V_{gs2}} V_{YX} + 2V_{gs1} = 0 \xrightarrow{V_{gs1}=\frac{I_{YX}}{g_m}} \frac{V_{YX}}{I_{YX}} = \frac{-2}{g_m} \quad (1)$$

In this case, you can obtain the oscillation condition. To have stable oscillations, it is required that in the parallel resonant RLC circuit resistance must be greater than the size of the differential amplifier equivalent resistance seen from both X and$Y$. Therefore, the circuit oscillation condition is written as follows:

$$R_P \geq \left|\frac{-2}{g_m}\right| \rightarrow R_P \geq \frac{1}{g_m} \quad (2)$$

2.1. First Proposed Design

The first proposed circuit for a variable voltage capacitor is based on the use of capacitive property of the density layer in a CMOS transistor based on 0.18 µm technology and the setting and tuning of capacitive property with a voltage change.

Given that our ultimate goal is to design VCO with a low phase noise, we used an oscillator with a differential structure.

For this reason, the symmetry in the proposed form for a variable capacitor seems to be necessary to achieve the goal of a low phase noise and differential structure. Figure 2 shows the first proposed structure for a variable voltage capacitor. The number of transistors in this topology is based on the achievement of proper tuning and symmetric structure. Table 1 shows the equivalent capacitance seen from both A and B in terms of voltage variable voltage capacitor for the proposed topology.

According to Table 1, the results indicate a change from 0.11 to 0.18 pF (range of capacitance variation is 0.07 pF) for an equivalent capacitor in design frequency (about 3.8 GHz).

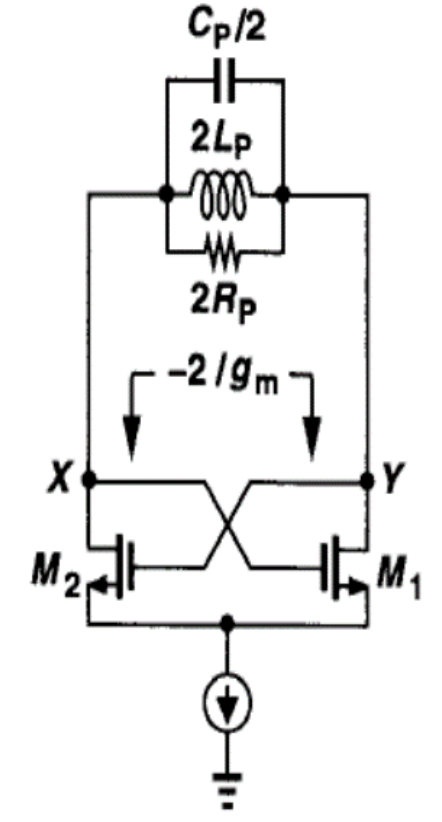

Fig. 1. Ordinary oscillator circuit.

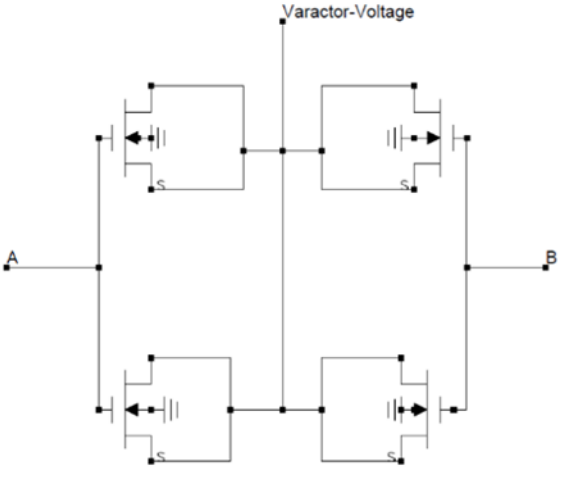

Fig. 2. The first proposed plan for a variable voltage capacitor.

Table 1. Capacitor Variations In Terms Of Voltage In The First Proposed Structure At The Frequency of 3.8 GHz.

Voltage (in terms of Volt)	Varactor Capacitor (in terms of Pico Farad)
0	0.18
1	0.15
2	0.13
3	0.12
4	0.11
0	0.18
1	0.15

LC cross-oscillators play an important role in the design of high frequency circuits due to a relatively good performance of the phase noise and ease of implementation. In this paper, differential cross-oscillators are used.

Fig. 3 shows the first proposed low phase noise VCO circuit schematic. This oscillator consists of three parts with a variable voltage capacitor: 1- A constant current source for feeding LC; 2- A differential amplifier; and 3- A suitable differential amplifier circuit (the bottom of the circuit).

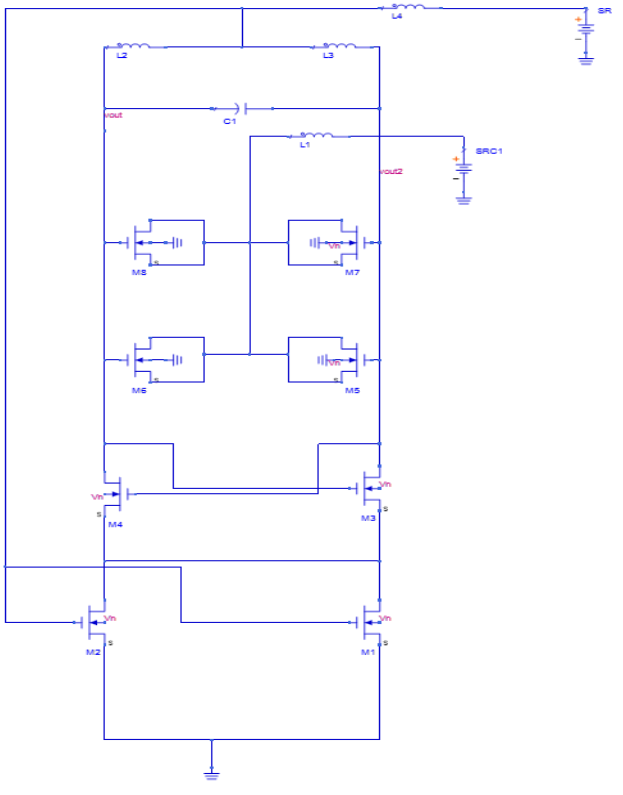

Fig. 3. A proposed oscillator controlled by voltage using the first variable capacitor topology.

The equivalent inductor value in accordance to L2, L5 and L4 inductor in Figure 3 is achieved as follows:

$$L_{eq} = \left(\frac{1}{5} + \frac{1}{0.95} + 0.95\right) = 2.2nH \quad (3)$$

If we consider $\omega_0 = 3.7\ GHz$ then the equivalent capacitance can be obtained as follow:

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C_{eq}}} \rightarrow C_{eq} = \frac{1}{{\omega_0}^2 L_{eq}} = 0.82PF \quad (4)$$

Where ω_0 is the frequency of an oscillation. The equivalent capacitor required in theoretical calculations is equal to $0.82PF$. It can be said that the results of analysis and simulation are relatively good in this case. Fig. 4 shows the frequency of oscillation in term voltage control.

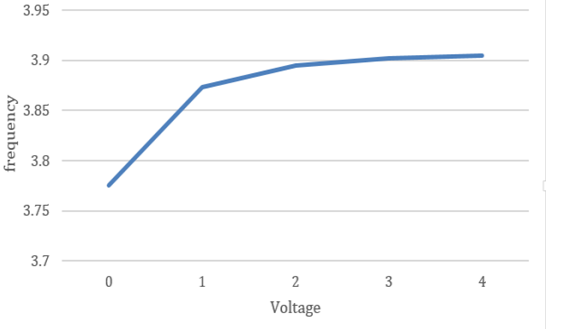

Fig. 4. Freuency of Oscillation Versus Voltage Control

2.2. Second Proposed Design

In the second proposed circuit, the goal was to increase the tuning rate. To do this, we used the topology presented in Fig. 5. In this topology, the capacitance and its variations were increased in accordance to the simulation results, which is given in Table 2. The results indicate changes from 0.21 to 0.33 Pico Farad ($0.12PF$) for an equivalent capacitor at design frequency (about 3.8 GHz).

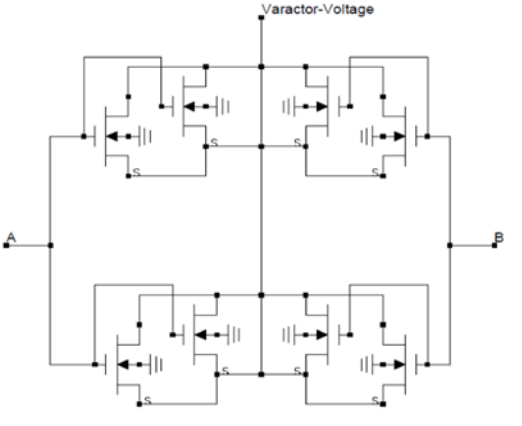

Fig. 5. The Second Proposed Topology for a Variable Voltage Capacitor.

The second proposed VCO circuit topology is shown in Figure 6. The difference between this circuit and the first Topology of VCO circuit as shown in Figure 3 is in the variable capacitor topology. This oscillator has more frequency setting range than the first design. But at the same time, the cost increases due to the increased number of transistors.

Table 2. Capacitor Variations in Terms of Voltage in the Second Proposed Structure at the Frequency of 3.8 GHz.

Voltage (in terms of Volt)	**Varactor Capacitor (in terms of Pico Farad)**
0	0.33
1	0.26
2	0.24
3	0.23
4	0.21

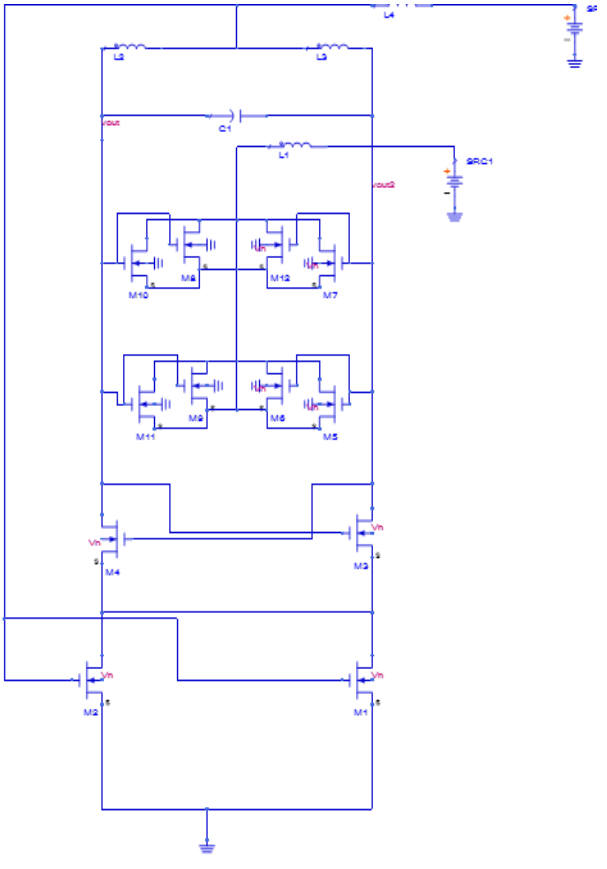

Fig. 6. A proposed oscillator controlled by voltage using the second variable capacitor topology.

3. ANALYTICAL AND SIMULATION RESULTS

In Advance Design System (ADS) software, first DC point of first design was examined. The results indicate the proper operation of the circuit, and especially the differential amplifier in terms of DC; that is, as expected, the circuit differential part works quite symmetrically in terms of DC. The current in both differential branches is equal and about 6.439 mA. Thus, from a 0.8 volt circuit power supply, a current as 12.88 mA is taken equivalent to a relatively low and suitable power consumption as 10 mW.

In the first design, results show that for different values of the voltage control, an appropriate phase noise of about -125 dBc/Hz can be obtained at the frequency of 1 MHz in the first design. In addition, by changing the voltage control of the variable capacitor, the oscillation frequency can be set from 3.775 to 3.905 GHz. In other words, the tuning rang of the oscillation frequency is about 130 MHz.

In the second design, for different values of the variable voltage control, an appropriate phase noise as -123 dBc/Hz can be obtained at the frequency of 1 MHz in the second design. In addition, by changing the voltage control of the variable capacitor, the oscillation frequency can be set from 3.651 to 3.901 GHz. In other words, the tuning range of the second design is nearly two times the value of this parameter in the first design. In order to arrive at a general conclusion, the comparison between the proposed oscillator and similar cases has been made. In Table 3, the frequency parameters, the setting range of frequency, phase noise, and power consumption are compared. It is also a key factor in determining the performance of the VCO (FOM) calculated by the following formula:

$$FOM = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \qquad (5)$$

In this formula L (Δf), the phase noise at the deviation frequency Δf, f_0 is the oscillation frequency and P_{dc} of the DC power consumption is in terms of mw. In fact, in the FOM parameter, the effect of frequency factors, DC power consumption, and phase noise is hidden. Therefore, the FOM parameter is also used for comparison in Table 3.

The results show that the VCO in this paper are better than references [5-22] in terms of phase noise and have the best status.

Table 3. Comparison of Oscillator Performance with References 5-22.

Reference	**Frequency (GHz)**	**Frequency Setting Range (MHz)**	**DC Power Consumption (mW)**	**Phase Noise at Deviation Frequency 1MHz (dBc/Hz)**	**FOM (dBc/Hz)**
[5]	3.87	-	5.6	-122	-201
[6]	5.36	-	3	-121.3	-198.8
[7]	5.2	780 (14.7%)	-	-118	-188.6
[8]	2.4	190 (8%)	0.66	-121	-190.4
[9]	1.57	240 (15%)	3.06	-120	-179
[10]	2.6	560 (22%)	2.7	-122.3	-186.3
[11]	5.8	1140 (19%)	10.8	-117	-181.9
[12]	2.4	390 (16%)	10	-115.7 in 600 KHz	-177.7
[13]	57	2000 (3.5%)	15	-96	-179.3
[14]	5	700 (14.6%)	19.8	-114 in 2 KHz	-169
[15]	2.36	300 (12.7%)	16.25	-104.33 in 600 KHz	-164
[16]	5.96	0.64	4.4	-120.5	-190.4
[17]	3.49	5	4.2	-123.06	-180
[18]	5.2	870 (16.7%)	9.7	-113.7	-178
[19]	2.5	131 (5%)	1.5	-119.2	-185.4
[20]	5.32	260 (4.9%)	5.7	-116	-183
[21]	55.7	17.2%	-	-93.5	-163
[22]	15	-	8.1	-109.30	-172
First proposed oscillator	3.7	130 (3.5%)	10	-125	-186.4
Second proposed oscillator	3.7	250 (7%)	10	-123	-184.4

4. CONCLUSION

In this paper, a new structure of Voltage Control Oscillator (VCO) to reduce the phase noise using two plans of a variable voltage capacitor is proposed.
The proposed oscillators are considered as low power oscillators in terms of DC power consumption and in terms of the FOM key factor among the compared references, and they are also in a very good condition. The results show that the VCO in this paper are better than references [5-22] in terms of phase noise and have the best status.

The frequency setting range of 3.5 and 7% is moderate. Generally, the voltages controlled by the proposed voltage in this paper are suitable for low power and low phase noise applications with the moderate tuning range.

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