Simulation, Modeling and Implementation of an Ultra-Low Phase Noise X-band Frequency Synthesizer

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ABSTRACT:
One of the most important components in telecommunication systems and radar activities are frequency synthesizers. Among the important parameters of a frequency synthesizer are phase noise, frequency resolution, programming speed, scanning rate and spur level in the output spectrum of the system. Typically, it is not possible for a frequency synthesizer to reach all of these parameters simultaneously. In other words, there are trade-offs between desired parameters. Among the structures of frequency synthesizers that can be used to achieve the optimal point for these parameters are multi-loop phase lock loop. In this paper, by presenting the noise model of different elements of a frequency synthesizer, simulations related to the achievable phase noise for a sample synthesizer in the X band are presented and finally the results of implementation of a sample synthesizer are presented.

KEYWORDS: Phase Locked Loop, Phase Noise, Multi-Loop Frequency Synthesizer.

1. INTRODUCTION

Nowadays, the use of low phase noise systems is increasing to improve the sensitivity of telecommunication receivers and increase the efficiency and range of military radars. Therefore, these subsystems are known as one of the most sensitive modules in telecommunication systems. On the other hand, lack of a proper synthesizer in such systems causes loss of adjacent channel signals for broadband receivers and also detection of clutters in radar systems. In this paper, by examining the general method of design and implementation of this type of frequency synthesizers, some models for simulating and modeling different circuit components, as well as simulating the output phase noise and implementation of a X band synthesizer are investigated.

2. PLL SYNTHESIZERS

Synthesizers, as one of the most important components in telecommunication systems, play a very important role in the performance and efficiency of a telecommunication system. In general, there are different methods for implementation of frequency synthesizers. In the following, we will review some general methods based on phase lock loops for implementation of frequency synthesizers.

2.1. Single-Loop PLL

In this type of frequency synthesizers, in order to obtain low frequency steps in the output, a combination of a phase lock loop and also a direct digital synthesizer are used. Due to the structure of these synthesizers, they usually have a high programming and scanning speed, but achieving high frequency resolution requires loss of phase noise at the system output. In fact, in classical frequency synthesizers, due to the fact that the reference signal is multiplied in a multiplier loop, the phase noise of the output signal increases by 20Log (N). Therefore, in cases where it is necessary to achieve low phase noise at the output, these loops can't be used. Also, due to the inherent nature of direct digital synthesizer and due to the fact that the power of its output spurs increases by 20Log (N), so they have a relatively high power level.

2.2. Multi-Loop PLL

The general method of implementation of low phase noise synthesizers is to use multi-loop PLL. In fact, in cases where we want to achieve low frequency steps in synthesizers, we have to use a loop with a number of mixers or several loops. In this case, due to the fact that the reference signal is placed in the collector circuits instead of in a multiplier circuit, the output phase noise will not increase with the increase seen in classical loops. Fig. 1 shows a block diagram of a synthesizer using several mixers in order to achieve a low frequency

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step at the output[1]. But one of the main disadvantages of mixer loops is the possibility of locking the loop on multiple frequencies at the output due to the multiplier nature of the mixer. To prevent this from happening, methods called voltage-controlled oscillator steering are used. The dividing path on N placed parallel to the mixer in Fig. 1 plays practically the same role. In fact, first the frequency synthesizer locks on the above path and then switches to the mixer path. By doing this, due to the fact that the loop is locked in the mixed mode, the loop will lock on the desired frequency.

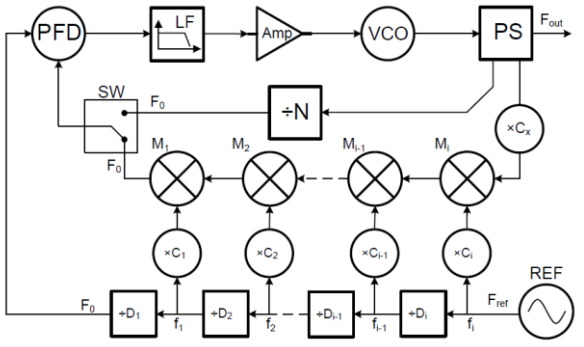

Fig. 1. Block diagram of a synthesizer using several mixers.

3. NOISE MODEL OF CIRCUIT ELEMENTS

In order to perform phase noise simulations, we need the noise model of different circuit elements. ADS software library models have been used in the simulations. However, due to the lack of phase-frequency detector element noise model with high and low output in the software library, the model of Fig. 2, which is a modified phase-frequency detector model in the software, has been used.

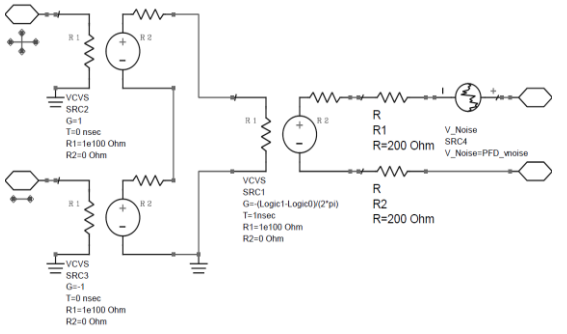

Fig. 2. Phase-frequency detector element noise model with up/down output.

4. EQUIVALENT CIRCUIT OF MULTI-LOOP NOISE

In order to investigate and simulate the phase noise of a frequency synthesizer, in the first stage, the phase lock loop noise model must be obtained. In fact, it is very important to determine where the equivalent noise source should be located for each element, because by moving the noise source location, the closed-loop response of the output noise to that source will change. According to the structure suggested for this synthesizer, the frequency of the noise equivalent circuit of Fig. 3 is considered for the loop [3].

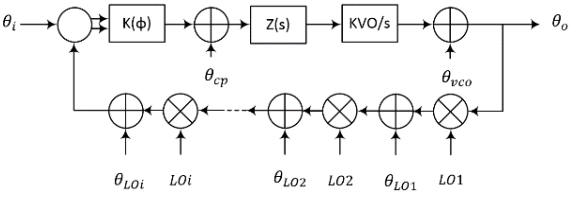

Fig. 3. Frequency synthesizer equivalent noise circuit.

By obtaining the equivalent circuit for this frequency synthesizer, the noise conversion function of each considered noise sources can be obtained. The voltage conversion function of a voltage-controlled oscillator is shown in Equation (1).

$$T_{VCO}(S)=\frac{\theta_O(S)}{\theta_{VCO}(S)}=\frac{1}{1+G(S)H(S)} \tag{1}$$

Depending on the structure of the loop, Equation (1) can be rewritten as Equation (2).

$$T_{VCO}(S)=\frac{1}{1+G(S)} \tag{2}$$

With a little care in the relation above, since G(S) conversion function contains a virtual integrator (which is due to the inherent nature of the voltage-controlled oscillator), it is clearly observed that, like all classical loops, this conversion function is a high-pass function.

Also, the phase noise conversion function of the phase-frequency detector element is shown in Equation (3).

$$T_{CP}(S)=\frac{\theta_O(S)}{\theta_{CP}(S)}=\frac{G(S)}{1+G(S)}.\frac{1}{K_\Phi} \tag{3}$$

Equation (3), which shows the conversion function of the phase-frequency detector noise effect at the output of the frequency synthesizer, is similar to that in classical loops and a low-pass function.

Now, in order to obtain the noise effect of the mixers and the local signals of each mixer at the output of the conversion function, we show them as Equation (4).

$$T_{CP}(S)=\frac{\theta_O(S)}{\theta_{Mix}(S)}=\frac{G(S)}{1+G(S)} \tag{4}$$

An important point in Equation (4) is that in addition to the low-pass conversion function of the phase noise effect of the local signals of the feedback path mixers, this conversion function shows the same shape for all mixers.

5. SIMULATION RESULTS

To simulate a frequency synthesizer, a sample was considered in the X band with a frequency step of 1Hz. By implementation the circuit of this synthesizer in ADS software and also using the noise models introduced above, the effect of the phase noise of the loop elements and also the total phase noise on the output of the frequency synthesizer was investigated.

Fig. 4 shows the results of simulating the effect of voltage-controlled oscillator phase noise on the system output. As this Fig. shows, the effect of voltage-controlled oscillator phase noise on the output is the same as a classic phase locked loop in the form of a high-pass filter. Also, in Fig. 5, the effect of other noise sources on the final output phase noise is obtained, which shows the low-pass function of the reference signal phase conversion effect function, local oscillators of mixers, as well as phase-frequency detector.

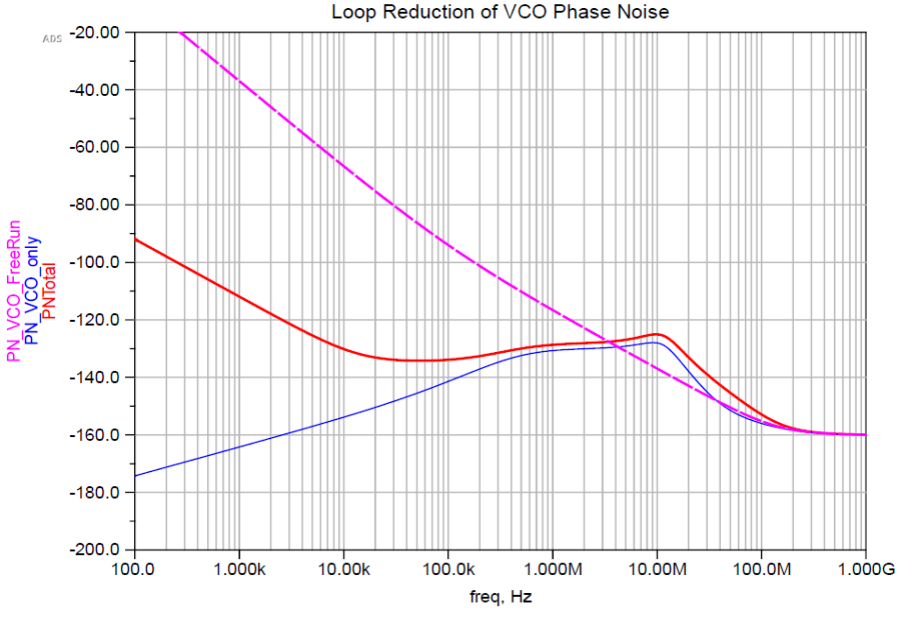

Fig. 4. Effect of VCO phase noise on synthesizer output.

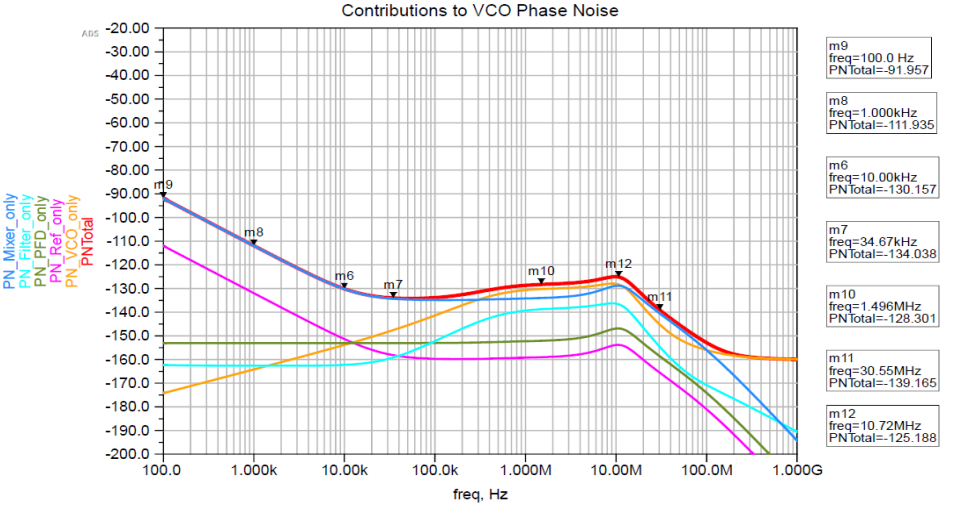

Fig. 5. Phase noise effect of individual lock loop elements.

6. TEST RESULTS

After simulating this frequency synthesizer, it was constructed and implemented in the laboratory. Fig. 6 shows the blocks made to implement this frequency synthesizer.

The various blocks that make up this frequency synthesizer include a direct digital synthesizer block implemented with the AD9954 chip (to achieve low frequency pitch), a block including analog dividers and multipliers (for larger frequency phases), and another block including the main frequency synthesizer loop. The result obtained from the output phase noise of this frequency synthesizer that corresponds to its simulation is shown in Fig. 7.

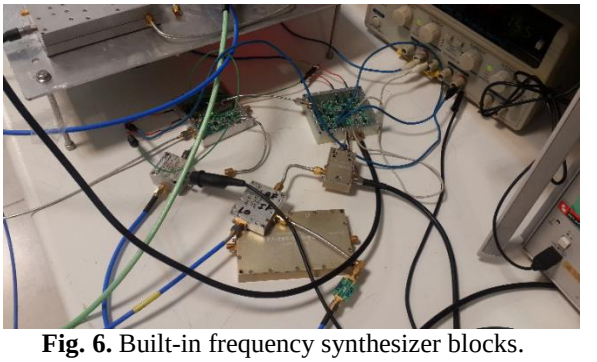

Fig. 6. Built-in frequency synthesizer blocks.

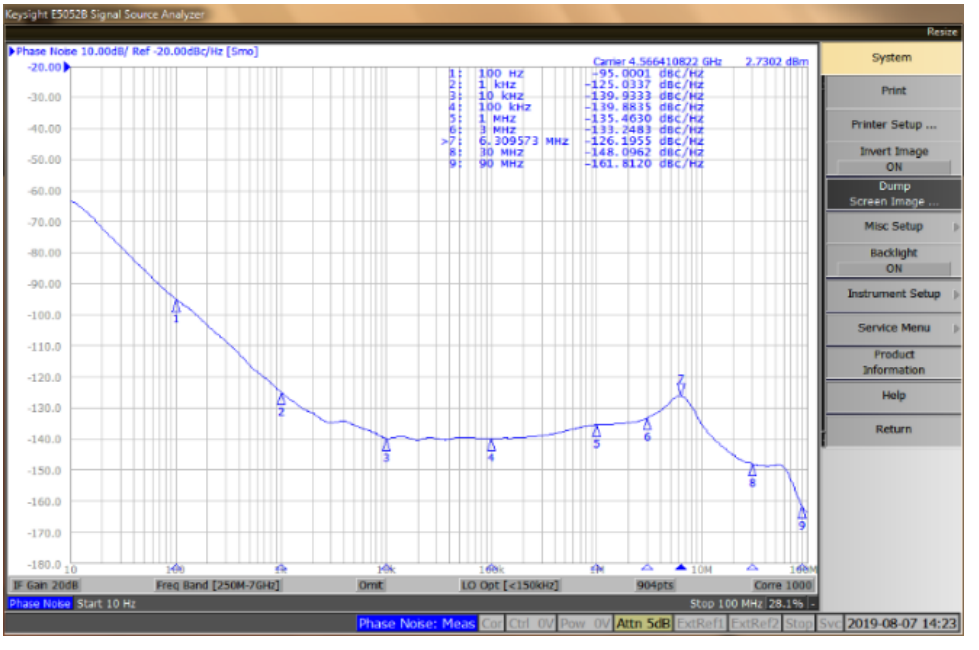

Fig. 7. Measured phase noise.

7. CONCLUSION

In this paper, firstly, the general method was considered to implement an ultra-low phase noise frequency synthesizer. Then by simulating a sample synthesizer in the X band, output noise as well as the effect of individual sources of limiting output phase noise was investigated. After examining and simulating the multi-loop phase lock loop, a frequency synthesizer in the X band was made by this method and its test results were presented.

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