Design and Simulation of a Fully Integrated, Low-Power, 2.5Gb/s Optical Front-End

Tahereh Shafiei[1*], Soorena Zohoori[2], Mehdi Dolatshahi[2]
1- Department of Electrical Engineering, Shiraz Branch, Islamic Azad University, Shiraz, Iran
Email: tahereh.shafiei90@gmail.com(Corresponding Author)
2- Department of Electrical Engineering, Najafabad Branch, Islamic Azad University, Najafabad, Iran

Received: August 2018 Revised: September 2018 Accepted: October 2018

ABSTRACT:
This paper, describes a CMOS trans-impedance amplifier (TIA) and Limiting Amplifier (LA) for 2.5Gb/s, low-power opto-electronic communication receiver systems. The single ended TIA, which benefits form active type of inductors, is designed and simulated using 0.18µm CMOS process parameters. The proposed circuits are analyzed mathematically and all necessary simulations for proving the proper performance of the proposed TIA stage and the proposed LA stage such as eye-diagram, MONTECARLO and noise analysis are done. Simulation results in HSPICE show the trans-impedance gain of 45.5dBΩ, frequency bandwidth of 1.85GHz and power consumption of 1.1mW at 1.5V supply for the TIA stage and 87dB gain and 2GHz frequency bandwidth for the whole receiver system, which consumes only 7.3mW power. Results indicate that the proposed circuits are suitable to work as a low-power building block as opto-electrical communication receiver.

Keywords: Low-Power, Trans-impedance Amplifier, Limiting Amplifier, Integrated Optical Receiver.

1. INTRODUCTION

For decades in 20th century, carrying massive volume of information over long distances was a dream. Till 1979, that fibers were improved by reducing dislocations and impurities, fiber optic telephone system was used for the first time. That was because losses in fibers reaches 0.2db per kilometer in 1979, and bandwidth of fiber reaches 25GHz and even 50GHz. In comparison with twisted-pair cables, which have the loss of 200db per kilometer at 100MHz, fiber optics has a great advantage.

Another advantage of fiber optics is their bandwidth. This advantage leads to possibility of use of multiple frequencies to carry several channels on a single fiber [1]. Fig.1 shows a simple optical system.

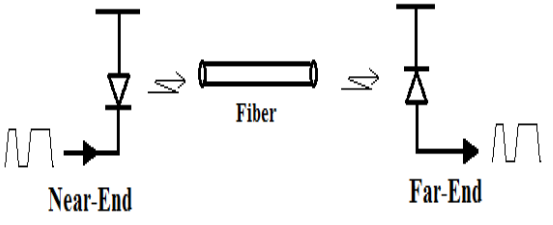


Fig.1. Simple Optical System.

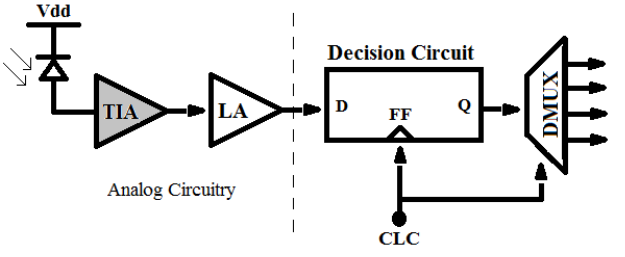


Fig. 2. Block Diagram of the Far-End Receiver.

At Far-End, the weak current produced by photodiode, needs to reach a proper logical level to be usable in digital circuitry. So the current needs to be amplified and converted to voltage. For that, one stage trans-impedance amplifier (TIA) and several stages of limiting amplifiers (LA) are being used. The block diagram of the front-end receiver consists of an analog circuitry and a digital circuitry is shown in fig. 2. The most critical stage in Front-end receiver is the TIA stage. Because, the TIA stage not only should amplifies the photodiode current, but also should provide a sufficient bandwidth [2-6] and produce low range of thermal noise. The problem of noise of course, can be easily solved in LA stages, because they have basic structure of differential amplifiers.

In this paper, a low-power TIA stage is proposed. The proposed TIA, not only has the sufficient trans-impedance gain and bandwidth, but also consumes low power. Also, In order to minimize the occupied chip area, the proposed TIA is designed in a fully integrated structure.

So, this paper is organized as follow: in section 2 the proposed TIA is presented and discussed. In section 3, simulation results and analysis of the TIA are given. In section 4, a brief discussion on the proposed LA stage is given, and section 5 describes the whole receiver system. Finally, section 6 concludes the paper.

2. THE PROPOSED TIA

The proposed TIA is shown in Fig. 3. Frequency response of TIA structures are usually given in form of (1) or (2), as follows:

$$H_{(s)} = \frac{A_0}{1+\frac{S}{w_0.Q}+\frac{S^2}{w_0^2}} \quad (1)$$

$$H_{(s)} = \frac{A_0}{1+\frac{S}{w_0.Q^2}+\frac{S^2}{w_0^2.Q^2}+\frac{S^3}{w_0^3}} \quad (2)$$

For the proposed TIA, transfer function can be written in form of (2), but as the pole in drain of M2, in comparison with input pole and output pole is omissible, transfer function for simplicity can be written as (1). Poles in the TIA are consisting of output pole, which originates from load capacitance, and input node, which originates from photodiode capacitance. The input pole is the dominant one.

In the proposed TIA, M6-M11 and M12 are used for two reasons: First, to obtain the proper biasing fpr M1 and second to form an inductive behavior by combination of M11 and M12 at input node. Therefore, the input capacitance (dominant pole) resonates with M11 and M12, and as a consequence the speed of the circuit and it's bandwidth is improved at the input node.

The proposed TIA is consists of a cascade stage and a common-source stage. These two stages povide the trans-impedance gain. Trans-impedance gain of the proposed TIA can be given by (3), as follows:

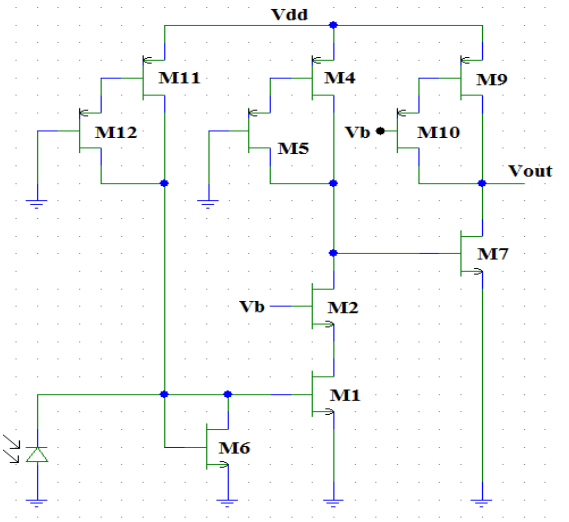


Fig. 3. The Proposed TIA.

$$V_{out} = (I_{ph} \times Z_{in}).A_{v1}.A_{v2}$$
$$A_{v,total} = \frac{V_{out}}{I_{ph}} = Z_{in} \times A_{v1} \times A_{v2}$$
$$A_{v1} \approx g_{m1}.\ (Z_{D2} \| r_{o1}.[(g_{m2}+g_{mb2})r_{o2}+1])$$
$$A_{v2} = g_{m7} \times Z_{D3} \quad (3)$$

In which Z_{D1}, Z_{D2} and Z_{D3} are the combinations which form the active inductive peaking technique for input and output nodes.

The input impedance of the TIA can be given as follows:

$$Z_{in} = \frac{Z_{D1}}{1+Z_{D1}.g_{m6}} \quad (4)$$

In which Z_{D1} is the impedance of combination of M11 and M12 seen at input node (Z_{D2} and Z_{D3} can be written in a same way), and is equal to:

$$Z_{D1} = \frac{r_{o12}.C_{gs11}.S+1}{g_{m11}+C_{gs11}.S} \quad (5)$$

From which the inductance behavior can be extracted, and is equal to:

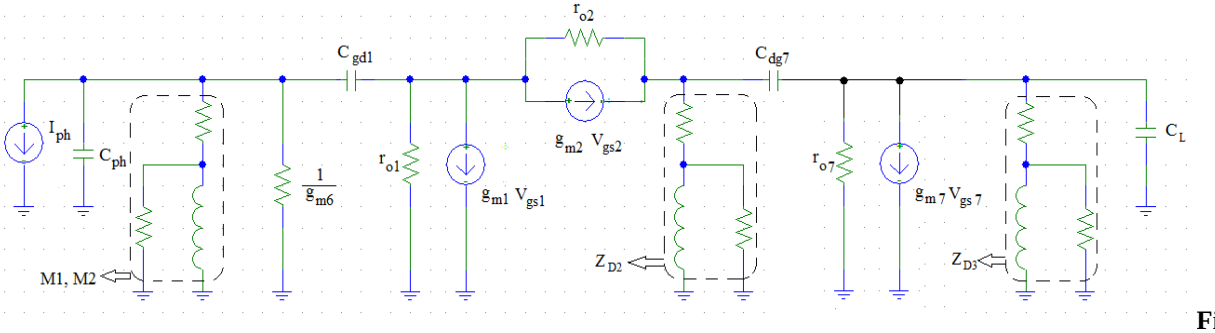


Fig. 4. Equivalent Circuit of the Proposed TIA.

$$L = C_{gs11}\left(\frac{r_{o12}}{g_{m11}} - 1\right) \quad (6)$$

As it is mentioned in [1], in order to obatin the optimum peaking, the quantity of the inductor should be equal to (7), as follows:

$$L = 0.4 \times R^2 \times C \quad (7)$$

So, by having the input impedance and knowing the fact that the summation of input capacitances of the TIA and photodiode capacitance is approximately equal to the photodiode capacitance (C_{in}+ $C_{ph} \approx C_{ph}$), the input pole can be given as follows:

$$C_{in} = C_{ph} + C_{db6} + C_{dg11} + C_{db11} + C_{dg12} + C_{db12} \approx C_{ph}$$
$$S_{p,in} = -\frac{1+Z_{D1}.g_{m6}}{C_{in}.Z_{D1}} \quad (8)$$

So, M1 amplifies the photodiode signal. M2 is used to increase the gate voltage of M7, and as a consequence the voltage at output node shifts up. Increased output voltage makes M7 to operate in saturation region so that adequate gain can be obtained. The increased output voltage also provides enough dc biasing for next stage (LA stage). Also, the inductive technique at output node with active elements is obtained. So, the effect of the output capacitance is also lessened. Output impedance can be written as (9), as follows:

$$Z_{out} = \frac{r_{o7}.r_{o10}.C_{gs9}.S + r_{o7}}{(r_{o10}.C_{gs9} + r_{07}.C_{gs9})S + r_{o7}.g_{m9}} \quad (9)$$

Also, input and output impedance at low-frequencies can be given, as follows:

$$Z_{out(S=0)} = \frac{1}{g_{m9}} \quad (10)$$
$$Z_{in(S=0)} = \frac{1}{g_{m6} + g_{m11}} \quad (11)$$

So, the pole at output node can be written as (12):

$$S_{p,out} = -\frac{1}{C_L.R_{out}}$$
$$C_L = C_{dg7} + C_{dg9} + C_{dg10} + C_{db9} + C_{db10} \quad (12)$$

And as it was discussed before, the input node of the TIA is the dominant pole, because the parasitic capacitance of photodiode is so large (in range of 0.2pF to 0.5pF) [1]. So, the -3db frequency can be written as (13), as follows:

$$f_{-3db} \approx \frac{1}{2\pi.C_{ph}.R_{in}} \quad (13)$$

M4 and M5, according to (5) and (6), reduce the effect of the pole seen at drain of M2. Also, M9-M10 and M11-M12 resonate with output and input capacitances. So, the proposed TIA not only has a wide bandwidth, but also has a proper trans-impedance gain. Active inductive peaking technique in the proposed TIA lets us obtain proper frequency response by using less dc current. That is how the power dissipation of the TIA is reduced.

3. SIMULATION RESULTS OF THE TIA

To verify the performance of the proposed TIA, the circuit is simulated in HSPICE using 0.18µm CMOS technology parameters. The input capacitance of 1pF for simulations is chosen. Fig. 5 shows the frequency response of the proposed TIA. As it can be seen in fig. 5, trans-impedance gain of the proposed circuit is equal to 45.5dBΩ and it's bandwidth is equal to 1.85GHz. Also, power consumption of the TIA for 1.5V supply is 1.1mW. Moreover, as it was expected dc voltage at output node is higher, and that is the effect of adding M2.

Fig. 6 shows the simulated eye-diagram of the proposed TIA. The eye is opened for input pulse current of 800µA. Fig. 6 clearly shows that the output signal has proper swing and quality.

As it is important to analyze the input resistance, due to the dominant pole at this node, fig. 7 shows the simulated input resistance of the circuit. As it can be seen, the input resistance at -3db frequency is only about 35Ω.

MONTECARLO analysis is also done in HSPICE and is shown in fig. 8. As it is shown in fig. 8, in fabrication process no significant fluctuation may happen on frequency response and only bandwidth may change for 04.4 percent.

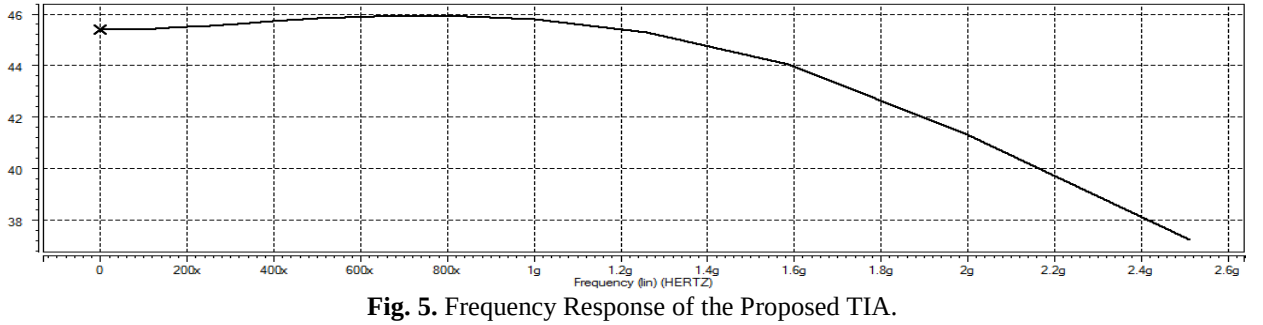


Fig. 5. Frequency Response of the Proposed TIA.

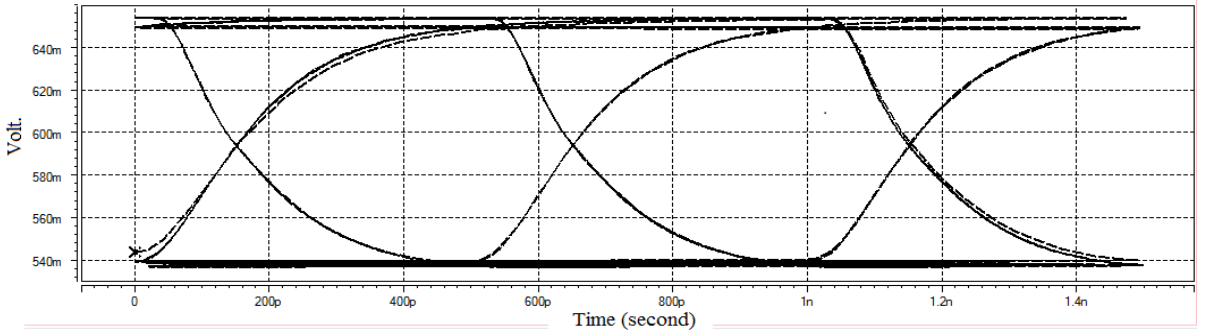


Fig. 6. Eye-Diagram of the Proposed TIA.

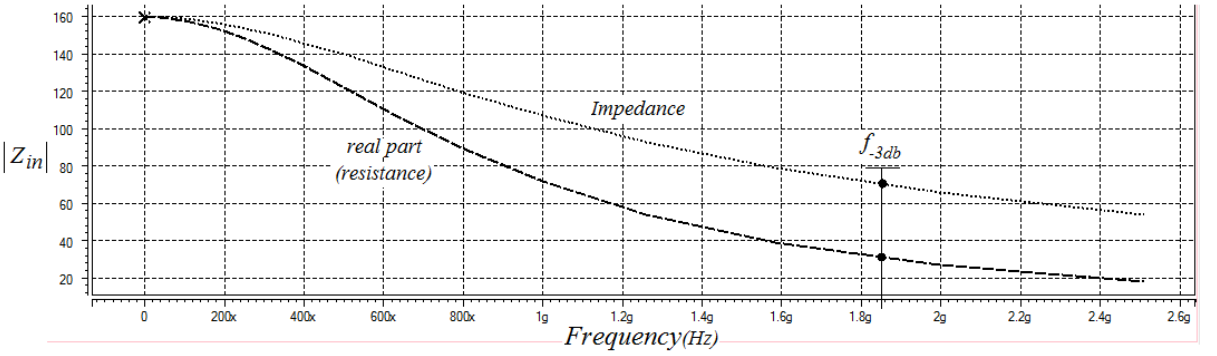


Fig. 7. Input Impedance and Resistance of the TIA.

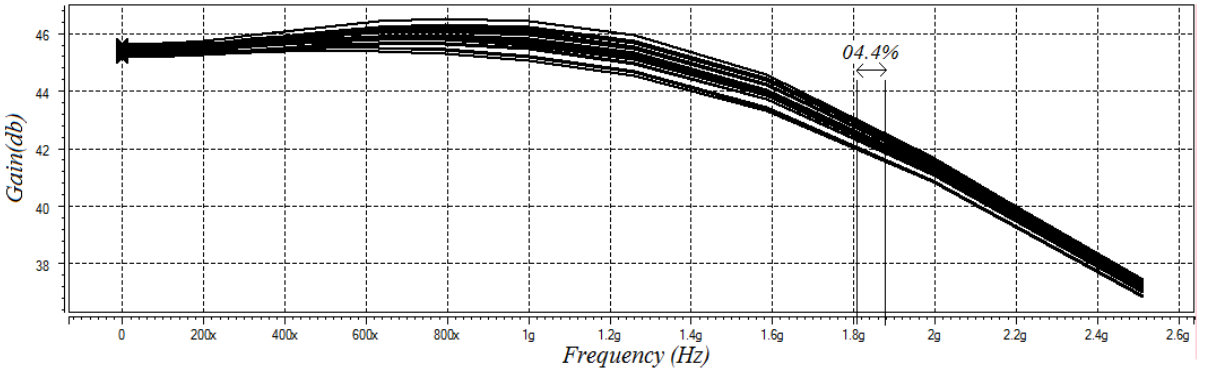


Fig. 8. MONTECARLO Analysis.

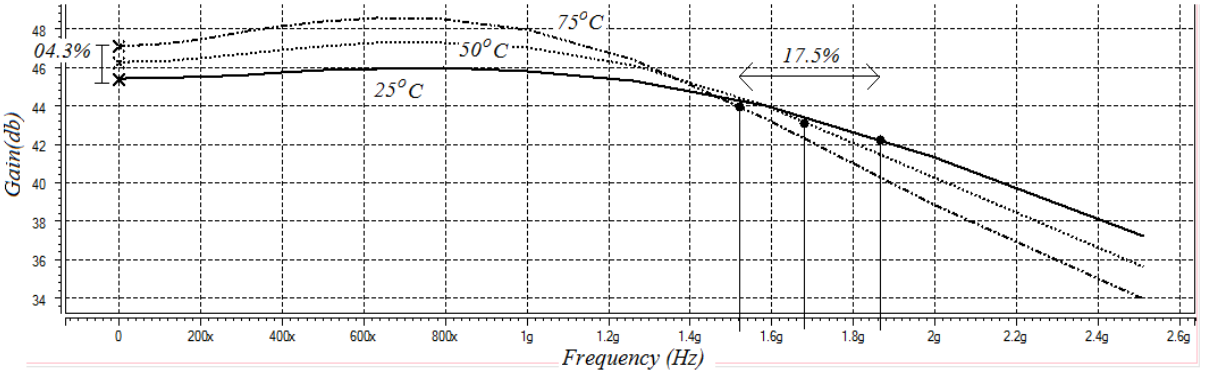


Fig. 9. Effect of Temperature variations for 25°C, 50°C and 75°C.

Fig. 9 also shows the effect of temperature variation on frequency response. As it can be seen, bandwidth varies for 17.5% and trans-impedance gain varies for 4.3% for 50^{O}C temperature variation. In receiver systems, structure of LA stages is usually based on differential structures. Albeit produced thermal noise in TIA stage can be easily eliminate in LA stages, it is constructive to study the thermal noise of the TIA. In fig. 10 (a) and (b), thermal noise of each transistor is represented by a current source.

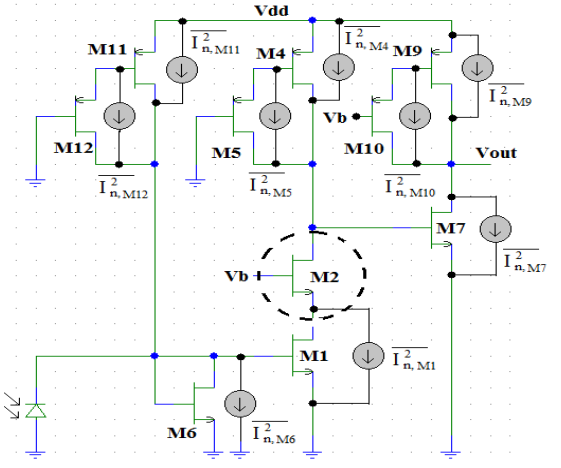


Fig. 10 (a). Noise Circuit of the Proposed TIA.

In order to calculate the input referred noise of the system, produced thermal noise of the common-source stage should be divided by $(g_{m7} \times g_{m1})^2$, and thermal noise of cascade stage should be divided by ${g_{m1}}^2$. M2 produces no thermal noise, because all of produced current by M1 flows through Z_{D1} and no part of $\overline{I_{n,M2}^2}$ flows through Z_{d1}.

So, at input node we have:

$$\left(\overline{I_{n,M7}^2} = 4KT.\gamma.g_{m7} \quad , \quad \overline{I_{n,M1}^2} = 4KT.\gamma.g_{m1}\right)$$

$$\overline{I_{n,2nd\ stage}^2} = \frac{\overline{I_{n,ZD3}^2} + \overline{I_{n,M7}^2}}{(\frac{1}{g_{m7}}.\frac{1}{g_{m1}})^2} \tag{14}$$

$$\overline{I_{n,1st\ stage}^2} = \left(\overline{I_{n,ZD2}^2} + \overline{I_{n,M1}^2}\right) \times \frac{1}{g_{m1}^2} \tag{15}$$

Where γ is the noise factor of the MOSFET.

Because M6 operates in triode region and works as a resistor, $\overline{I_{n,M6}^2}$ is as follow [14]:

$$\overline{I_{n,M6}^2} = \frac{KT}{C_{ph}} \tag{16}$$

In fig. 11, the simulated input referred noise and output noise of the proposed TIA is shown.

Also, fig. 12 shows the transient output voltage of the TIA. As it can be seen, proper swing is obtained for the signal.

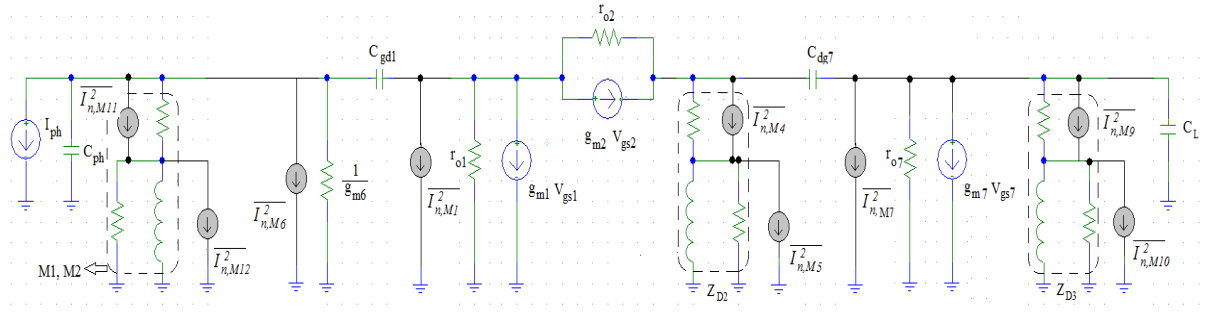
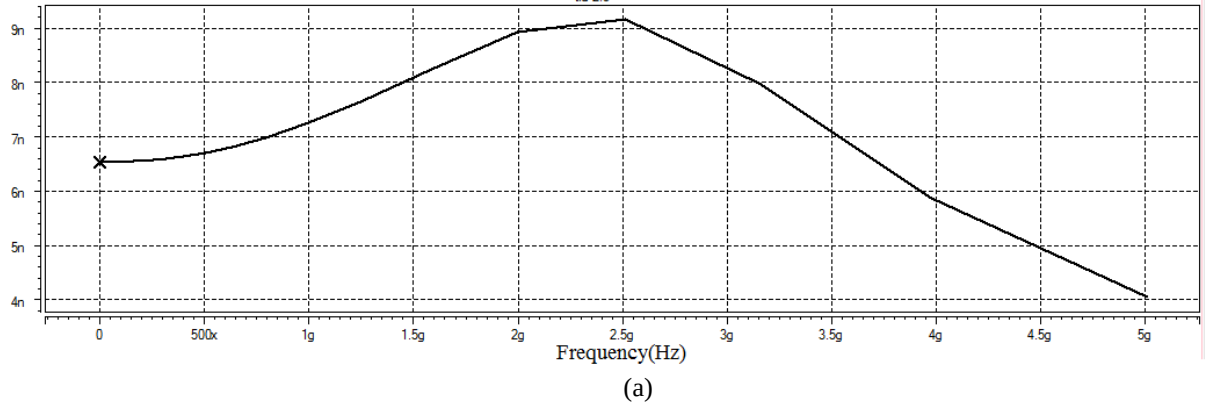
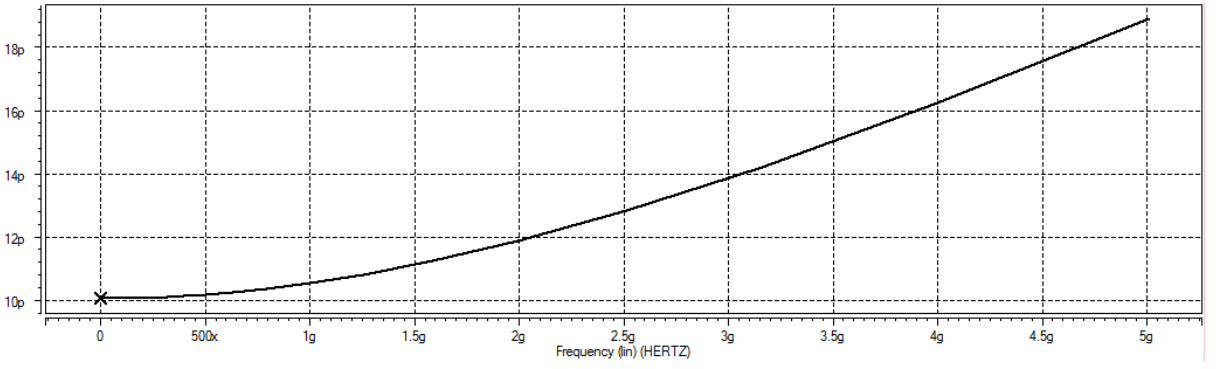


Fig. 10 (b). Noise Circuit of the Proposed TIA.



(a)



(b)

Fig. 11. (a) Output Noise and (b) Input Referred Noise.

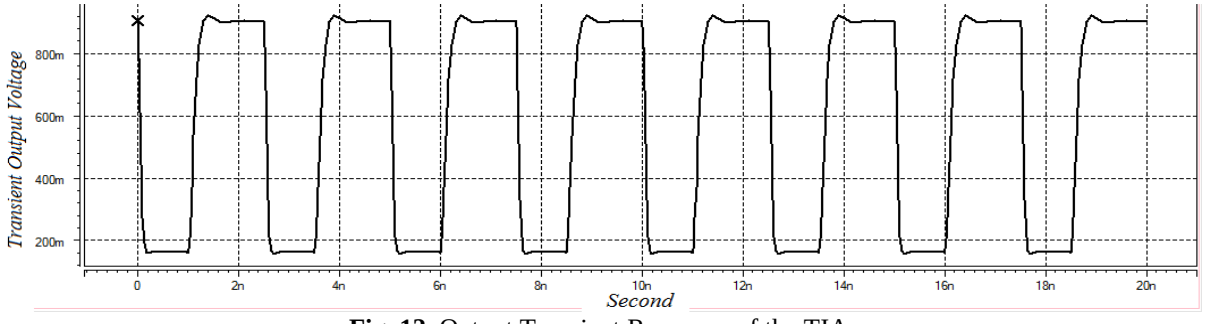


Fig. 12. Output Transient Response of the TIA.

4. THE PROPOSED LA STAGE

As it was mentioned before, a LA structure should be based on differential topologies, to eliminate the thermal noise of previous stages. One of the challenges in designing LA stages is their proper frequency bandwidth.

Fig. 13(b) shows the proposed LA circuit. In order to obtain more ac current from differential structure, two transistors are used in parallel. Active inductors are used as load in each circuit. M5 and M6 operate as inductors, So, the active loads resonate with output capacitance and it can be said that a zero is added to the transfer function and the pole at output node, formed by the load capacitance, is transferred to a higher frequency. In such a way, by using active loads, it is possible to obtain a higher bandwidth using less dc current.

Output impedance of each cell is as follows:

$$Z_{out,LA} = \frac{1}{2}\frac{r_{oN}.(R_1.\ C_{gs5}.S+1)}{(R_1.\ C_{gs5}.S+1)+\frac{1}{2}r_{oN}\,(g_{m5}+C_{gs5}.S)} \qquad (17)$$

So, The output pole can be written as $S_P = \frac{1}{R_{out}.C_L}$.

Also, as three stages of LA are cascaded, the -3dB frequency will be decreased. Considering -3dB frequency of each cell gain as follows:

$$w_s = w_n \cdot \sqrt{1-2\xi^2+((1-2\xi^2)^2+1)^{\frac{1}{2}}} \qquad (18)$$

In which the transfer function of each cell gain is equal to $A(s) = \frac{A_v.\ w_n^2}{S^2+2\xi w_n.S+\ w_n^2}$, where A_v is small signal gain, and ξ is the corresponding damping factor. For 3 stages of LA, the -3dB frequency is as follows:

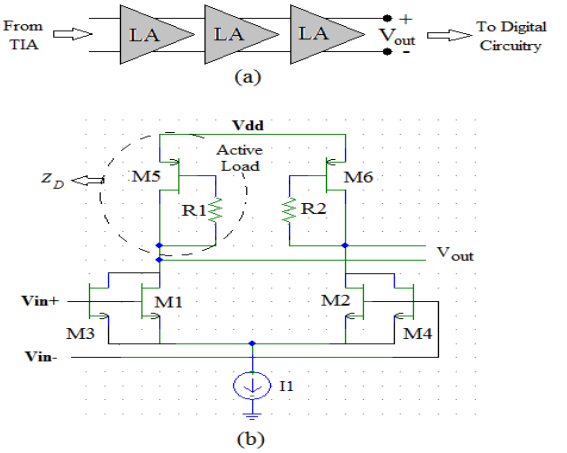


Fig. 13. (a) Block Diagram of LA. (b) Structure of Each Cell Gain.

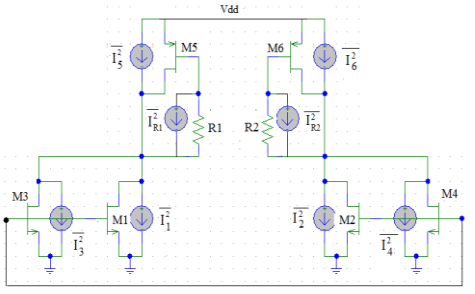


Fig. 14. Equivalent Thermal Noise Model.

$$w_C = w_n \cdot \sqrt{1 - 2\xi^2 + \sqrt{(1-2\xi^2)^2 - 1 + \sqrt[3]{2}}} \qquad (19)$$

For analyzing the thermal noise of the proposed TIA, fig. 14 represents thermal noise of each transistor by a current source.

Considering that thermal noise is uncorrelated, output thermal noise can be written as follows:

$$\overline{V_{n,out}^2} = \left(\overline{I_{n3}^2} + \overline{I_{n1}^2} + \overline{I_{n4}^2} + \overline{I_{n2}^2}\right) Z_D^2 + 2\overline{I_{n,ZD}^2} . Z_D^2 \qquad (20)$$

And at input node, it is equal to:

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{2(g_{m3}^2 + g_{m1}^2) \cdot Z_D^2} \qquad (21)$$

Fig. 15, shows the block diagram of the optical communication receiver. It consists of 2 TIA circuits, and 3 LA stages.

Fig. 16, shows the frequency response of the whole receiver, simulated in HSPICE using 0.18µm CMOS technology parameters. As it can be seen, the whole receiver has a gain total of 87dB and bandwidth of 2GHz. Also the power consumption of the whole system in a 1.5v supply voltage is only 7.3mw.

Also, fig. 17, shows the effect of the temperature variations on frequency response of the whole receiver. It depicts the frequency response for 25^{O}C, 35^{O}C and 45^{O}C.

Eye-diagram of the whole receiver is also simulated and is presented in fig.18. The eye is opened for proper amount of voltage domain, which shows the proper quality of the output signal in the designed receiver system. The input applied current pulse is 100µA and the domain of the signal for entering digital circuitry is about 600m volt.

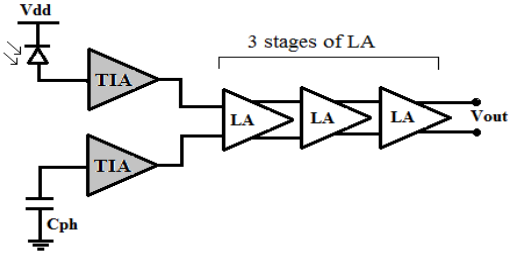


Fig. 15. Block Diagram of the Receiver.

5. THE OPTICAL RECEIVER

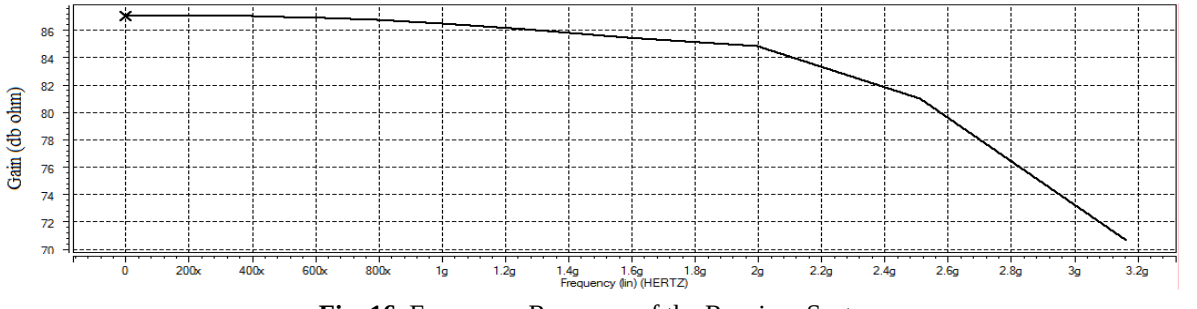


Fig. 16. Frequency Response of the Receiver System.

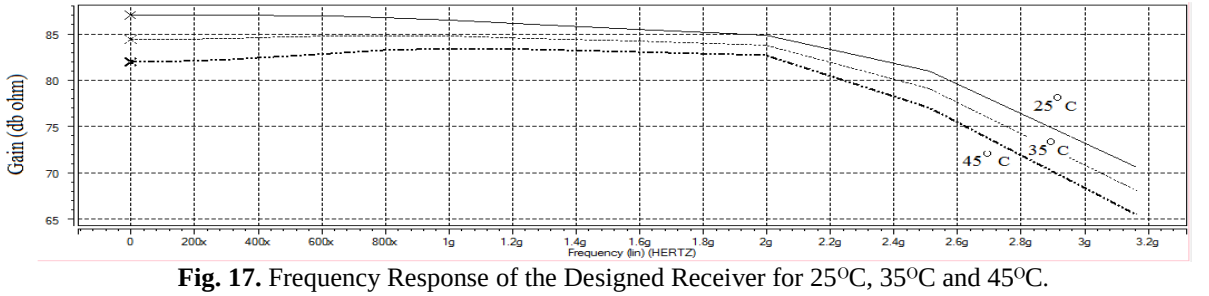


Fig. 17. Frequency Response of the Designed Receiver for 25^{O}C, 35^{O}C and 45^{O}C.

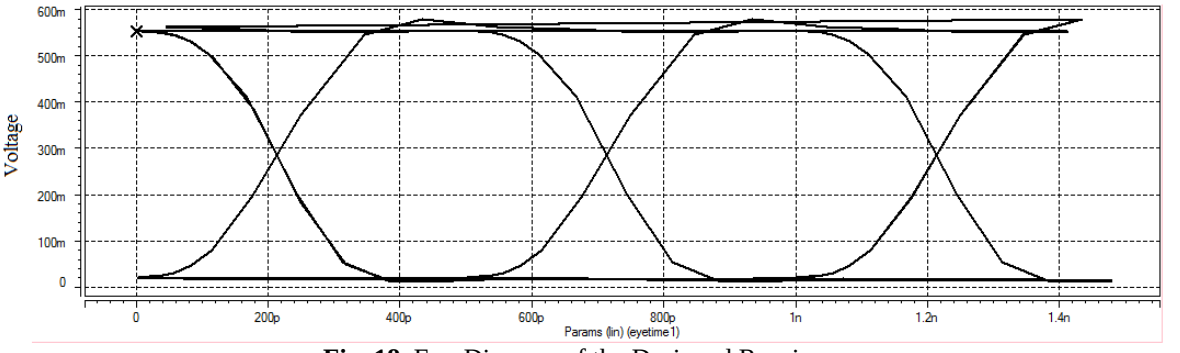


Fig. 18. Eye-Diagram of the Designed Receiver.

Finally, table.1 shows the comparison of the proposed TIA, with other reported ones. As it can be observed, the proposed TIA has some superiors in compare to other ones.

Table 1: Comparison of the Proposed TIA.

Ref	Tech.	Supply Voltage	Power Consumption	Gain (dBΩ)	Band width
[7]	0.6 µm CMOS	6v	135mw	61	3.5 GHz
[8]	0.25 µm CMOS	2.5v	27mw	80	670MHz
[9]	0.18 µm CMOS	1.8v	7.2mw	41	1.8GHz
[10]	0.18 µm CMOS	1.8v	68mw	52	4.2GHz
[11]	0.18 µm CMOS	1.8v	19.5mw	82	2.4GHz
[12]	0.35 µm CMOS	3.3v	148mw	60	10GHz
[13]	60 F_T GaAs	-5.2v	19.5mw	28	10.5GHz
This work	0.18 µm CMOS	1.5v	1.1mw	45.5	1.85GHz

6. CONCLUSION

In this paper, a full-transistor, 2.5Gb/s, low-power trans-impedance amplifier is proposed, which is followed by a LA stage. The proposed TIA is discussed mathematically, and all necessary simulation such as eye-diagram, MONTECARLO analysis, Noise analysis and effect of temperature variation on the TIA are done and discussed. Simulations in HSPCIE using 0.18µm CMOS technology parameters show the trans-impedance gain of 45.5dbΩ, bandwidth of 1.85GHz and 1.1mw power consumption for 1.5v supply voltage. Also, the whole receiver system shows 87dB gain and 2GHz frequency bandwidth, while consumes only 7.3mW power. Results indicate that the proposed Circuits are suitable to work as low-power optical front-End.

REFERENCES

[1] B. Razavi, **"Design of *Integrated Circuits for Optical Communications"*** , *Wiley series in lasers and applications* , 2nd edition, 2003.

[2] F. Aznar, S. Celma and B. Calvo, "**CMOS Receiver Front-Ends for Giga-bit Short-Range Optical Communications**", *Springer Science+Business Media New York*, 2013.

[3] C. Y. Wang, and C. S. Wang, **" An 18mw Two Stage CMOS Transimpedance Amplifier for 10Gb/s Optical Application***", In proceedings of IEEE Asian Solid-state Circuits Conference in Jeju*, pp. 412-415, 2007.

[4] J. Kim and J. Buckwalter, "**Bandwidth Enhancement with Low Group-Delay Variation for a 40 Gb/s Transimpedance Amplifier**", *IEEE Transaction on Circuits and Systems*, TCAS I, Vol. 57, pp.1964-1972, 2010.

[5] F. Aflatouni and H. Hashemi, "**A wideband 57dbΩ Transimpedance Amplifier in 0.13µm CMOS in IEEE radio Frequency Integrated Circuits Symposium**", *Digest of papers in Boston*, pp.57-60, 2009.

[6] W. Chen, Y. Cheng and D. Lin. **" A 1.8v 10Gbps Fully Integrated CMOS Optical Receiver Analog Front End"**, *IEEE Journal of Solid State Circuits*, Vol. 40, pp.3904-3907, 2007.

[7] C. Toumazou, and S. M. Park, **"Low-noise Current-Mode CMOS Transimpedance Amplifier for Giga-Bit Optical Communication"**, *IEEE Proc. ISCAS*, vol. 3, June 1998

[8] J. Lee, and S. j. Song, "**A Multichip on oxide of 1Gb/s 80db Fully Differential CMOS Transimpedance Amplifier for optical Interconnect Applications"**, *ISSCC*, pp. 80-81, Feb. 2002.

[9] Y. Wang, and R. Raut, **"A Design of Transresistor Amplifier for High Gain Bandwidth Applications,"** *10th IEEE International Conference on Electronics, Circuits and Systems*, pp. 185-188. 2003.

[10] Y. Wang, and r. Raut, **"A 0.18µm CMOS Fully Differential Transimpedance Amplifier for optical Receiver,"** *2nd IEEE Northeast Workshop on Circuits and Systems*, pp. 229-232, 2004.

[11] Y. Wang, and r. Raut, **"A 2.4GHz db Fully Differential CMOS Transimpedance for Optical Receiver Based on Wide-Swing Cascode,"** *IEEE International Conference on Electronics*, pp. 1601-1605, 2005

[12] Y. Wang, and r. Raut, **"A 2.4GHz db Fully Differential CMOS Transimpedance for Optical Receiver Based on Wide-Swing Cascode,"** *IEEE International Conference on Electronics*, pp. 1601-1605, 2005

[13] H. Fenfei and D. jingxing, **"0.35µm SiGe BiCMOS Front-End Amplifier for 10Gb/s Optical Receiver"** *International conference on microwave and millimeter Wave technology*, ICMMT, pp. 249-252, 2008

[14] B. Razavi**, "Design of Analog CMOS Integrated Circuits"**, *MacGraw – Hill Series in Electrical and Computer Engineering*, 2002.

[15] S. Galal and B. Razavi, **"Broadband ESD Protection Circuit in CMOS Technology"** *Digest of IEEE ISSCC*, pp. 182-183, 2003.