Gain Enhancement and Noise Figure Improvement of Low Noise Amplifiers in 0.13 µm CMOS Technology for UWB Applications

S. Khodabakhshi[1], M. H. Ostovarzadeh[2], A. Hakimi[3]
1. Department of Electrical Engineering, Graduate University of Advanced Technology, Kerman, Iran
S.khodabakhshi@ymail.com
2. Department of Electrical Engineering, Graduate University of Advanced Technology, Kerman, Iran
mh.ostovarzadeh@kgut.ac.ir
3. Department of Electrical Engineering Shahid Bahonar University, Kerman, Iran
hakimi@uk.ac.ir

Received: December 2015 Revised: January 2016 Accepted: January 2016

ABSTRACT:
A novel CMOS wideband low-noise amplifier (LNA) with a new architecture of high gain, low NF and low power-consumption is proposed. This architecture consists of two non-uniform stages. In order to achieve high power gain (S_{21}) and low power consumption, a current reused with resistive feedback based on an inverter-type amplifier is utilized at the first stage. The second stage of this circuit is used to increase the bandwidth and power gain. Simulation results show that the proposed LNA achieves a power gain between 19±.3 dB. The input return loss (s_{11}) and output return loss (s_{22}) are better than -10 dB. The noise figure (NF) of the proposed LNA is between 2~3.6 dB and reverse gain (S_{12}) is below -30 dB for 3.1~10.6 GHz bandwidth. The input third-order intercept point (IIP3) and power consumption of the proposed LNA are -5 dBm and 13.6 mW, respectively.

KEYWORDS: RF, CMOS, Low-Noise Amplifier (LNA), Low-Power, Ultra Wideband (UWB).

1. INTRODUCTION

Nowadays due to increasing demand of globally spread users for high speed information transmission technology, RF circuit designers tend to offer wideband transceivers. LNA, which is used at the first stage of the receiver, after antenna, plays an important role in receiving signal, amplifying it while reducing its undesirable noise. Design of a wideband LNA is one of the challenges in RF circuits because it must have proper input and output matching, low noise, high gain and low power consumption across a wide frequency bandwidth.

Numerous wideband LNAs have been designed for good performance [1], [2], [8] with advanced technology based on the complementary metal–oxide semiconductor (CMOS)

The LNA with two stages is designed in [1] which has used current reused technique at the first stage and cascode structure at the second stage. Although the proposed LNA has low power consumption (p_D) of 7.2 mW and flat power gain (S_{21}) of 11±1.5 dB, But its noise figure (NF) of 5±2 dB is not acceptable. Authors in [3] proposed a LNA with two stages which uses wideband dual-RLC-branch input matching network. This circuit has reasonable NF and S_{21}, but using five inductors occupies large chip area. Two inductors less wideband LNA with noise canceling teqnique was proposed in [4]. By employing inductor scheme, the chip area decreased, but low power gain is a drawback for this topology.

Moreover, reference [5] has proposed a two-stage ultra wideband LNA combining the common source and common gate configuration that occupies small chip area, But its NF of 4.4~6.5 dB, power gain of 10.9±1.5 dB and power consumption of 12 mW are not convenient.

The LNA bandwidth is limited by the parasitic capacitances of devices. For increasing the bandwidth, two methods are often used: the inductive peaking techniques [6] and the distributed Amplifier (DA) topology [7], [8]. Although, DAs improve the power gain and extend the bandwidth at higher frequencies, the power consumption of these circuits is high and also they occupy large chip area. Contrastingly, in inductive peaking techniques, inductors are employed as few as possible because they occupy most area of the chip. To reduce LNA, self-forward body bias and forward combining techniques are proposed in [8]. In the present study, a high-gain and low-power-

consuming circuit is proposed which functions conveniently in NF terms.

In section II, we analyze the proposed circuit. In section III, we present the results associated to the proposed LNA using ADS software. A conclusion will follow the results and findings of this simulation.

2. CIRCUIT DESIGN AND ANALYSIS

The schematic of the proposed LNA is illustrated in Fig. 1. As is seen from this figure, it is composed of two stages. The analysis of these stages is discussed as follows:

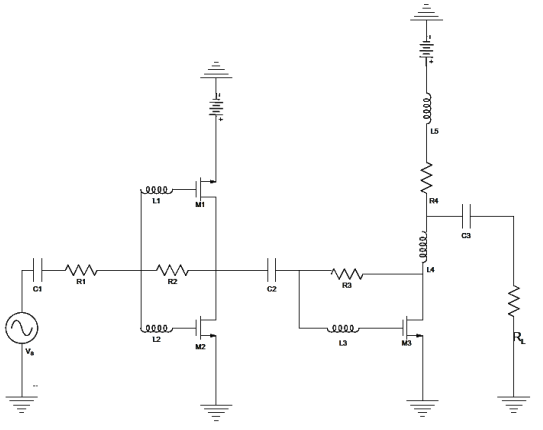

Fig. 1. Schematic Diagram of the proposed CMOS LNA

2.1. First stage

In the first stage, a stacking NMOS and PMOS current reused topology with resistive feedback is employed. Because of reusing the DC current of M_2 by M_1, no additional driving currents are needed for M_1. Hence, the power consumption of this topology is low. To bias the first stage and improve the bandwidth and linearity, the resistive feedback R_2 is employed [8]:

The first stage power gain can be derived as follows:

$$A_{V1}=\frac{V_{01}}{V_{in}}=\frac{1}{S^2L_1C_{gs1}+1}.\frac{1-R_1(g_{m1}+g_{m2})+s^2L_1C_{gs1}(1-g_{m2}R_1)}{1+\frac{R_1}{r_{01}\|r_{02}\|z_{in2}}} \quad (1)$$

Where r_{o1} and r_{o2} are the output resistances, g_{m1} and g_{m2} are the Trans-conductance, C_{gs1} and C_{gs2} are the gate-source parasitic capacitance of M_1 and M_2 MOSFETs, respectively. Z_{in2} is the input impedance of the second stage. Based on equation (1), the first stage obtain high power gain because of including $(g_{m1}+g_{m2})$ term in the power gain equation. Due to the high power gain of the first stage, the second stage noise is negligible.

The input impedance of the amplifier is derived as follows:

$$z_{in1}=\frac{1}{SCgs2}\left\|(SL_1+\frac{1}{SCgs1})\right\|\frac{R_1+(r_{o1}\|r_{o2}\|z_{in2})}{1+(g_{m2}+\frac{g_{m1}}{s^2L_1C_{gs1}+1})(r_{o1}\|r_{o2}\|z_{in2})} \quad (2)$$

Good input impedance matching is achievable by calculating the optimal value of Z_{in2}, L_1, R_1, DC bias current and transistors sizes. The inductor L_1 in the gate of the NMOS transistor extends the 3-dB bandwidth and improves flatness of the power gain. Putting L_1 in series with C_{gs1} move the frequency pole to higher frequency. Therefore the bandwidth is increased.

S_{21} of the amplifier can be obtained as follows:

$$S_{21}\approx\frac{V_{OUT}}{V_{in}}\approx\frac{1}{1+s^2L_{g1}C_{gs2}}.$$
$$\frac{1-R(g_{m1}+g_{m2})+s^2L_{g1}c_{gs2}(1-g_{m1}R)}{1+SR_1(C_{gs3}+c_{gs4})}.$$
$$\frac{1}{1+s^2L_{g2}C_{gs4}}. \quad (3a)$$
$$\frac{1-R_2(g_{m3}+g_{m4})+s^2L_{g2}C_{gs4}(1-g_{m3}R_2)}{1+R_2/R_L}\approx$$
$$\frac{R_1R_2(g_{m1}+g_{m2})(g_{m3}+g_{m4})}{1+R_2/R_L} \quad (3b)$$

The noise factor of the amplifier is given by [5], [6]:

$$F\approx1+\frac{Rg}{Rs}+\frac{\alpha\delta W^2C^2_{gs1}}{5(g_{m1}+g_{m2})}.\left|R_S-W^2L_1C_{gs2}R_S\right|$$
$$(C_{gs1}+C_{gs2}\frac{R_S}{R_1}))^2.\left|\frac{S^2+S(\frac{W_{o,dn}}{Q_{dn}})+w_{o,dn^2}}{g_{m1}+g_{m2}-\frac{1}{R_1}}\right|^2++\frac{\gamma(g_{m1}+g_{m2})}{\alpha R_S}+$$
$$\frac{(L_1(C_{gs1}+C_{gs2}(g_{m1}+g_{m2})R_S))^2}{R_SR_1}\times \quad (4a)$$
$$\left|\frac{S^2+S(\frac{W_{o,rln}}{Q_{rln}})+w_{o,rln^2}}{g_{m1}+g_{m2}-\frac{1}{R_1}}\right|$$

where:

$$W_{O,\mathrm{dn}} = \sqrt{\frac{1+R_S/R_1}{L_{g1}(C_{gs2}+C_{gs1}R_S/R_1)}} \quad (4b)$$

$$Q_{dn} = \frac{\sqrt{L_{g1}(C_{gs2}+C_{gs1}\frac{R_S}{R_1})(1+\frac{R_S}{R_1})}}{(\frac{L_{g1}}{R_1}+C_{gs2}R_S)} \quad (4c)$$

$$W_{o,\mathrm{rln}} = \sqrt{\frac{1+(g_{m1}+g_{m2})R_S}{L_{g1}(C_{gs2}+C_{gs1}(g_{m1}+g_{m2})R_S)}} \quad (4d)$$

$$Q_{r\,\mathrm{ln}} = \frac{\sqrt{L_{g1}(C_{gs2}+C_{gs1}(g_{m1}+g_{m2})R_S)(1+(g_{m1}+g_{m2})R_S)}}{L_{g1}(1+(g_{m1}+g_{m2})+R_S C_{gs2}} \quad (4e)$$

Values of L_1 and R_1 created trade-off between bandwidth and NF.

2.2. Second stage

Re-consumption of current forms the core of the second stage in which a self-bias resistant feedback plan has been implemented to set up the transistor.

As is shown in figure 1, in order to improve the power gain, bandwidth and linearity of the common source stage with self-biasing, the resistive feedback (R_3) is employed in the second stage. Also the shunt peaking inductor is used in the output drain. The inductor which is placed in the gate of NMOS Transistor serves the purpose of increasing bandwidth, impedance matching and improving the flatness of the circuit gain.

The second stage power gain can be obtained as follows:

$$A_{V2} = \frac{r_{o3}R_L(R_3+SL_3)(1-g_{m3}R_2)}{AS^2+BS+C} \quad (5)$$

Where:

$$A = L_2L_3(r_{o3}+R_2) \quad (6)$$

$$B = L_3R_L(r_{o3}+R_2)+L_2(R_L+R_3)(r_{o3}+R_2)+L_3R_2r_{o3} \quad (7)$$

$$C = (r_{o3}+R_2)R_LR_3+(R_L+R_3)R_2r_{o3} \quad (8)$$

The equation (6) shows that L_3 leads to extend the bandwidth and reach to good power gain in high frequencies. The inductor L_4 improves the output return loss (S_{22}), third-order input intercept point (IIP3) and gain flatness at high frequencies. To achieve better S_{22}, the size of M_3 should be optimized. As is deduced from equations (7) and (8), the shunt peaking inductor moves the pole frequency to higher frequencies. To decrease loading effect and improve wideband output matching the resistance R_2 should be selected high. By choosing suitable values for R_5 and L_5, the bad effect of output parasitic capacitance at the high frequencies can be decreased.

As A_{v2} indicates, the gain of second floor stands to high values due to inductor L_3.

The second stage input impedance (Z_{in2}) is calculated as follows:

$$Z_{in2} = \frac{1}{SC_{gs3}}\left\| \frac{R_2+r_{o3}\|(SL_2+(R_3+SL_3)\|R_L}{1+g_{m3}\left[r_{o3}\|(SL_2+(R_3+SL_3)\|R_L\right]} \right. \quad (9)$$

By calculating optimal value of Z_{in2}, good impedance matching is achievable. To improve power gain at low frequencies and also to achieve flat and high gain across the bandwidth, the Value of R_3 should be chosen low. The resistive feedback which is used for self biasing, provides the bias voltage for drain of M_3. The bias voltage of transistors and their sizes were optimized to reach appropriate input impedance.

To achieve appropriate bandwidth, the inductor L_3 was placed into the gate of M_3.. In order to reduce parasitic impact of capacitor at high frequencies.

To reduce power consumption, A compromise must be made between circuit gain and power supply voltage.

3. RESULTS

The proposed circuit has been designed and simulated based on 0.13µm CMOS technology. Moreover, in the preset circuit, inductors are considered de-idealized; therefore, for each inductor, depending on specific quality index, a level of resistance is defined. The proposed circuit was simulated by ADS software.

As is shown in Fig. 1, using current reused and common source topology leads to high power gain that is between 19±.3 dB. Also, the power gain tolerance across the bandwidth is low. M_1, M_2, M_3 and M_4 sizes are set to W_1=220 µm, W_2=100 µm W_3=78µm and W_4=400 µm, respectively.

In the first stage, 6.17 mA current is drawn from 1.25V supply voltage. In the second stage, 4.46 mA current is drawn from the 1.28V supply voltage. Thus power consumption of the proposed LNA is low and equal to 13.7 mW.

Fig. 2 and Fig. 3 show the simulated results for $|S_{11}|$ and $|S_{21}|$ versus frequency, respectively. The proposed LNA achieves $|S_{11}|$ of -12 dB for frequency band 1~11 GHz, and $|S_{11}|$ is better than -10 dB for frequencies lower than 12 GHz.

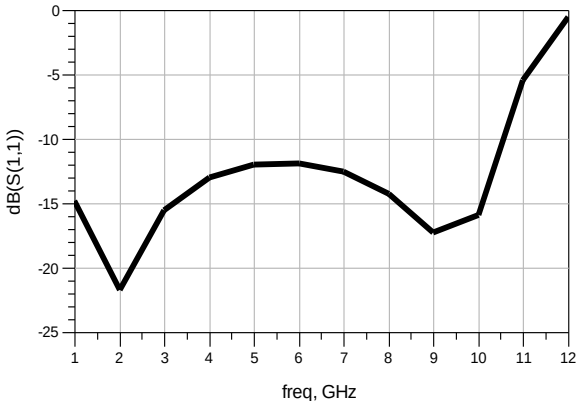

Fig. 2. Magnitude of S_{11} of the proposed CMOS LNA

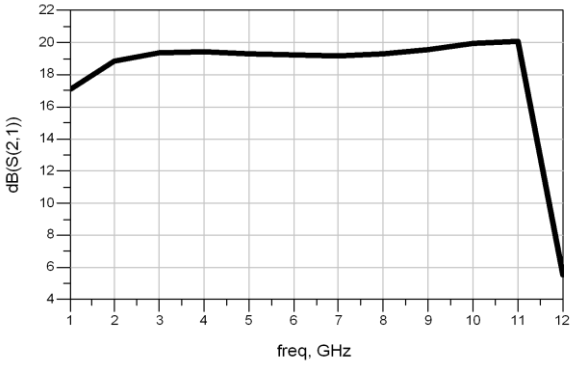

Fig. 3. Gain (S_{21}) Response of the proposed CMOS LNA

Figure 4 and figure 5 show the simulated values for $|S_{22}|$ and $|S_{12}|$ versus frequency. The $|S_{22}|$ and $|S_{12}|$ are respectively better than -11.4 dB and -33 dB across the Bandwidth.

Fig. 4.magnitude of S_{22} of the Proposed Circuit

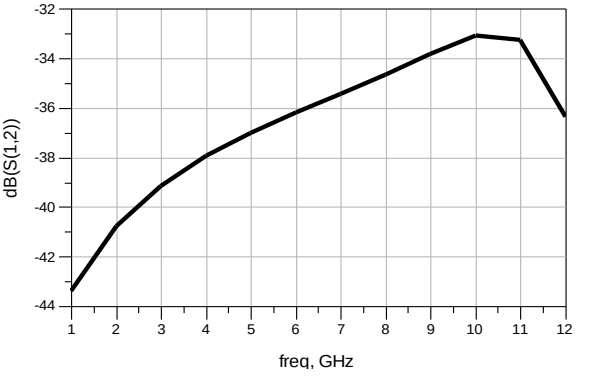

Fig. 5. Magnitude of S_{12} of the proposed CMOS LNA

Fig.6 clearly shows that the designed LNA achieves a noise characteristic below 2.3 dB from 1 to 12 GHz which is a good candidate for wideband low noise application.

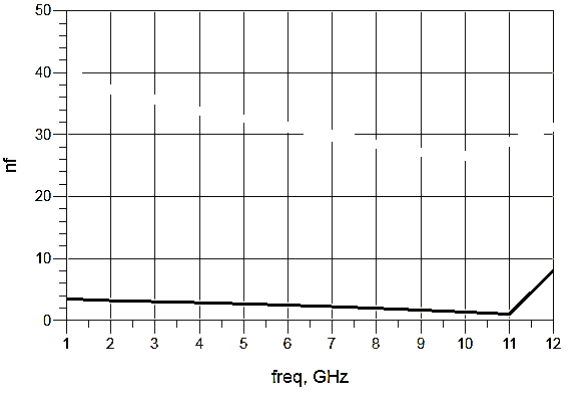

Fig. 6. Simulated values of NF of the proposed circuit versus Frequency

The stability of a LNA is an important requirement. The stability factor (k) is a popular measure of circuit stability [9]. If k>1 and $|\Delta|<1$, the amplifier is unconditioally stable meaning the LNA will be stable under any load condition. The appropriate values of k and $|\Delta|$ are obtaind as follows [10]:
As can be seen in figure 7, the k factor of the proposed LNA (stability factor) is more than 2. Thus, circuit stability is satisfactory across bandwidth.

$$K = \frac{1-|S_{11}|^2+|S_{22}|^2+|S_{11}\times S_{22}-S_{12}\times S_{12}|^2}{2|S_{12}\times S_{21}|} > 1 \quad (10)$$

$$|\Delta| = |S_{11}\times S_{22}-S_{12}\times S_{21}| < 1 \quad (11)$$

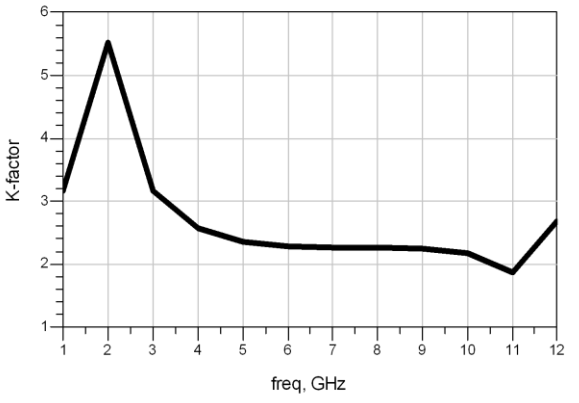

Fig. 7. Simulated values of k-factor of the Proposed Circuit

Figure 8 shows the simulated values of |Δ| in a wide frequency range.As is seen from this figure, Δ satisfied the condition [12].

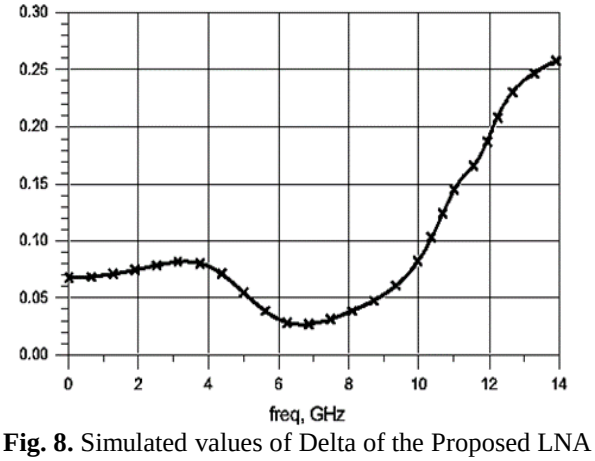

Fig. 8. Simulated values of Delta of the Proposed LNA

Figure 9. shows the IIP3 for the proposed LNA. The IIP3 for this design is -8.5 dBm.

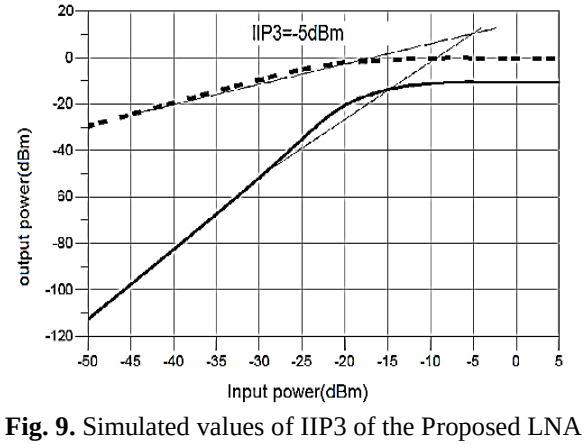

Fig. 9. Simulated values of IIP3 of the Proposed LNA

In Table I. we Compare the proposed LNA and other works.

Table 1. Comparison between the proposed LNA and other works

Ref	BW	$S_{11,S22}$	Gain	NF	IIP3	P_D	Tech
[9]	2.6-10.2	<-9	11±1.5	5±2	NA	7.2	90nm
[10]	0-10	<-10	9±1.5	3±.3	-3.5	13.7	65µm
[11]	1.5-11.9	<-10.6	11±.47	4.3±.57	-3.6	7	.18µm
[12]	1-12.5	<-10.7	13.7±1.5	2.3±.1	-.2	18	.18µm
[13]	1.5-11.7	<-8.6	12±.63	4±.5	-12	10.3	.13µm
[14]	.7-10	<-10	14±1.6	2.8±.3	-11.5	23	.13µm
[15]	3.1-10.6	<-7.3	11±1.4	3.2±.5	-3.8	14.4	.13µm
This work	3.1-10.6	<-10	19±.3	2-3.6	-5	13.6	0.13µm

As we know, achieving a high power gain in LNAs leads to high power consumption. But our proposed LNA architecture allows us to have high power gain and low power consumption, simultaneously.

4. CONCLUSION

We designed low noise amplifier using 0.13µm CMOS technology. The results show that the proposed LNA has good performance for wideband systems. In comparison with other works which used more than six inductors and occupied large area on chip, proposed LNA employes five inductors causing small area on chip. Simulation results prove that the proposed LNA achieves good power gain, low power consumption and low NF in a wide frequency range.

REFERENCES

1. G. Sapone and G. Palmisano**, "A 3–10-GHz low power CMOS low-noise amplifier for ultra-wideband communication,"** *Microwave Theory and Techniques, IEEE Transactions on*, Vol. 59, pp. 678-686, 2011.
2. I.-C. Chen and J.-R. Yang, **"3–10GHz CMOS distributed amplifier low-power and low-noise and high-gain low noise amplifier for UWB systems,"** *in TENCON 2010-2010 IEEE Region 10 Conference*, pp. 2045-2047, 2010.
3. C.-H. Wu, Y.-S. Lin, J.-H. Lee, and C.-C. Wang, **"A 2.87±0.19 dB NF 3.1~10.6 GHz ultra-wideband low-noise amplifier using 0.18µm CMOS technology,"** i*n Radio and Wireless Symposium (RWS), IEEE*, pp. 227-230,2012
4. K.-H. Chen and S.-I. Liu**, "Inductor less wideband CMOS low-noise amplifiers using noise-canceling technique,"** *Circuits and Systems I: Regular Papers, IEEE Transactions on*, Vol. 59, pp. 305-314, 2012.

5. K.-H. Chen, J.-H. Lu, B.-J. Chen, and S.-I. Liu, **"An ultra-wide-band 0.4–10-GHz LNA in 0.18-µm CMOS,"** *Circuits and Systems II: Express Briefs, IEEE Transactions on*, Vol. 54, pp. 217-221, 2007.
6. C.-F. Liao and S.-I. Liu**, "A broadband noise canceling CMOS LNA for 3.1–10.6-GHz UWB receivers,"** *Solid-State Circuits, IEEE Journal of*, Vol. 42, pp. 329-339, 2007.
7. Y.-S. Lin, J.-F. Chang, and S.-S. Lu, **"Analysis and design of CMOS distributed amplifier using inductively peaking cascaded gain cell for UWB systems,"** *Microwave Theory and Techniques, IEEE Transactions on*, Vol. 59, pp. 2513-2524, 2011.
8. C. H. Wu, Y. S. Lin, and C. C. Wang, **"A 3.1-10.6-GHz Current-Reused CMOS Ultra-Wideband Low Noise Amplifier Using Self-Forward Body Bias and Forward Combining Techniques,"** *Microwave and Optical Technology Letters*, Vol. 55, pp. 2296-2302, 2013.
9. G. Gonzalez, **"Microwave Transistor Amplifiers: Analysis And Design"**, *2nd ed, Prentic-Hall*, Upper Saddle River, NJ,1997.
10. M. Rajashekharaiah, "**Gain control and linearity improvement for low noise amplifier in 5GHz direct conversion receivers",** *Master of Science Thesis*, May 2005.
11. G. D. Nguyen , k. Cimino , and M.Feng, **"A RF CMOS amplifier with optimized gain, noise, linearity and return loss for UWB applications,"** in *proc. IEEE RFIC Symp*., ,pp. 505-508, 2008.
12. Y. Lu, K. S. Yeo, Ab. cabuc, J. Ma, M. Do, Z. Lu, **"A novel CMOS low noise amplifier design for 3.1-10. GHz ultra-wideband wireless receivers",** *IEEE Trans. circuits syst.* I: Regular Papers 531534-1692, 2006.
13. Kim, S.-S., Lee, Y.-S., Yun, T.-Y.: **"High-gain and wideband CMOS low noise amplifier with two-stage cascade and simplified Chebyshev filter"**, *ETRI J.*, Vol. 29, No. 5, pp. 670–672, 2007.
14. J.-H. Ham, J.-Y. Lee, and T.-Y. Yun, **"21-dB gain ultra-wideband complementary metal-oxide semiconductor low-noise amplifier with current reuse technique,"** *IET microwaves, antennas & propagation*, Vol. 5, pp. 1495-1501, 2011.
15. J.-H. Ham, J.-Y. Lee, and T.-Y. Yun, "**21-dB gain ultra-wideband complementary metal–oxide semiconductor low-noise amplifier with current-reuse technique**," *IET microwaves, antennas & propagation*, Vol. 5, pp. 1495-1501, 2011.