A 10-Bit Low Power SAR ADC with a New Control Logic Using Monotonic Capacitor-Switching

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ABSTRACT:
A 10 bit Low power 666KS/s successive approximation register is presented. Monotonic capacitor-switching has been employed to reduce the switching energy power and total capacitance by 81% and 50% respectively. The ADC achieves an SNDR of 53.6 dB and ENOB of 8.61, while the power consumption and supply voltage are 0.83mW and 1.2V respectively. all simulations are carried out using cadence simulating software in 0.18um technology.

KEYWORDS: Analog-to-digital converter**,** successive approximation register, energy efficient, monotonic switching, comparator, ENOB, SNDR.

1. INTRODUCTION

There has been a growing interest in the design of wireless sensing device for portable or implantable biomedical applications. the digitization of the sensed biomedical signals is mostly performed by a moderate resolution (8-12 bits) and a sampling rate of (1-1000 KS/Sec). Energy efficiency and battery lifetime is one of the critical issues in the design of ADCs employed in this devices which requires a design with microwatt power consumption to run a small battery for decades. At the same time the maximally allowed supply voltage VDD_{max} is continuously decreasing In modern CMOS process, but the threshold voltage of devices V_T is not scaled down in proportion to VDD_{max} due to the off-state currents and the related static power consumption of logic circuits. Among different ADCs, only SAR ADC benefits from technology downscaling, because of two reasons (1) it is an Opamp-free architecture (2) it mainly consists of digital circuits which is faster in deep sub-micron technologies.

The conventional SAR architecture needs a capacitor array with 2^N unit capacitors, where N is the resolution in bits. the switching order in this method is always from the largest one to the smallest, consequently, most of energy will be consumed in first several switching due to larger capacitances and voltage variation. The conventional SAR ADCs apply a Binary search algorithm to find the closest digital code to match with signal.in this kind of ADC the reference DAC is added or subtracted a binary-weighted voltage according to the comparator output in each bit cycle. The dominant source of power dissipation in SAR ADCS are comparator and the switching of capacitor array. The DAC switching network which is used in this design saves 81% of switching energy and 50% of total capacitance.

2. ADC ARCHITECTURE

A fully differential architecture is used in proposed paper because of better substrate and supply noise suppress. Binary weighted capacitors are used for better linearity, compared with C-2C capacitor array. Figure.1 shows the architecture of proposed 10-bit SAR ADC. It comprises a dynamic comparator, a differential capacitor array, Successive Approximation Register and a bootstrap switch.

The differential capacitor networks are composed by 10-bit binary-weighted capacitors with monotonic switching capacitor array. The switching procedure in Monotonic switching can be either upward or downward in contrast to conventional switching which is switched from largest capacitor C_1. The input signal is sampled on the top plates via Bootstrap switches which increases both input bandwidth and settling speed, and the bottom plates of capacitors are reset to V_{ref} simultaneously. next, after turning the bootstrapped switches off the comparator directly performs the first comparison without switching any capacitor. According to the results of first comparison the largest capacitor C_1 on the higher voltage potential side is switched to ground and the other one remains unchanged. The procedure is repeated until the LSB is obtained. The design consideration of building blocks are described in the following subsection.

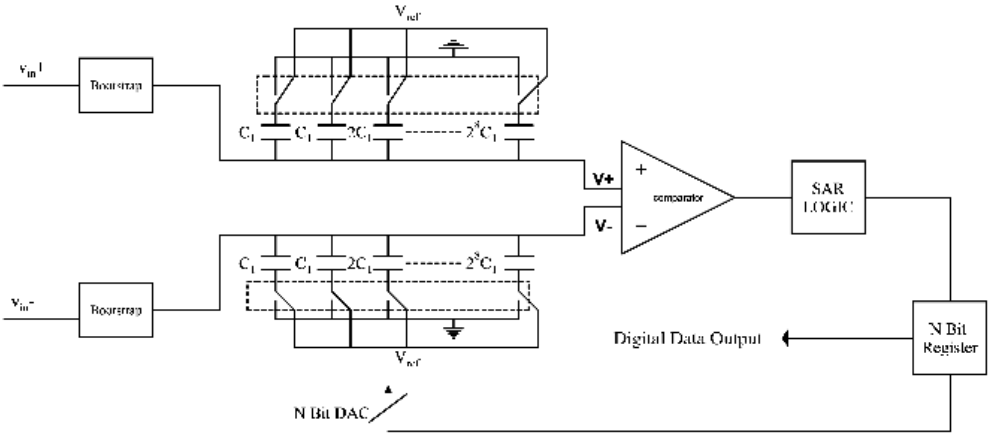


Fig.1. The block diagram of fully differential SAR ADC

2.1. Bootstrapped Switch

The Bootstrapped switch shown in figure.2 performs the S/H function .The gate-source of sampling transistor is fixed at the supply voltage (V_{DD}) which is significantly effective to make the on-resistance constant, consequently offers better linearity. The bootstrap switch is on during sampling phase which is 500 nano second. In the next one us the switch doesn't pass the signal.(the whole period is 1.5us)

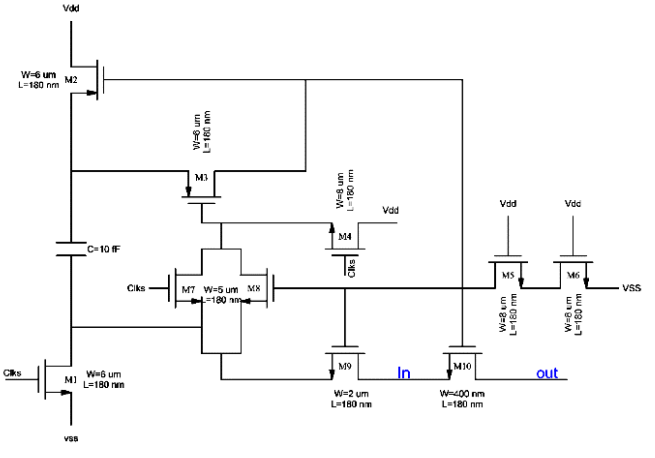


Fig.2. Bootstrap Switch

2.2. Dynamic Comparator

The schematic of a dynamic comparator with one current source is shown in figure.3. in order to have a proper function within the input common-mode voltage range, a p-type input pair is employed.

The outputs out_p and out_n are reset to high when clkc is high and when it goes to low M5 and M6 compares the two input. The offset voltage of Comparator follows equation (1).

$$V_{Offset} = \Delta V_{th,5,6} + \frac{(V_{GS} - V_{th,5,6})}{2}\left(\frac{\Delta S_{5,6}}{S_{5,6}} + \frac{\Delta R}{R}\right) \qquad (1)$$

$\Delta V_{th,5,6}$ is the threshold voltage offset of the differential pair M5, M6. $(V_{GS} - V_{th,5,6})$ is the effective voltage of the input pair and ΔS is the physical dimension mismatch between these differential pair. M3 keeps the effective voltage of the input pair near a constant value when common mode voltage changes.

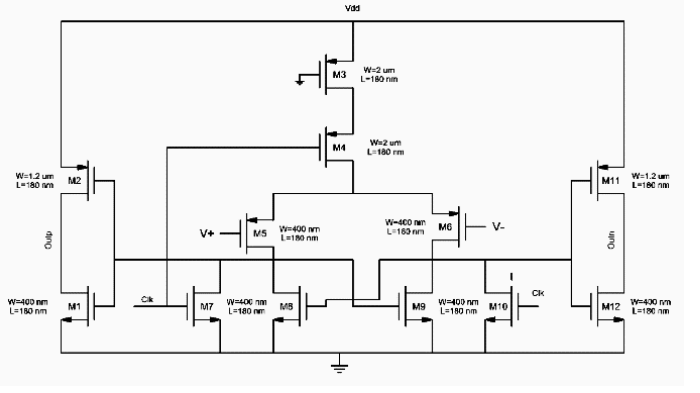


Fig.3. Dynamic Comparator with one Current Source

This is a common way to improve dynamic offset and minimizing its influence on conversion linearity.
There are also some other approaches to improve the offset voltage. enlarging the comparator size and reducing the effective voltage of pair are two of them, but they have the disadvantages of power consumption increase and comparison speed decrease respectively.

2.3. SAR CONTROL LOGIC

Fig.4 shows the schematic of SAR logic control and how the valid signal (the common clk for all Flip-Flops) is created. outp and outn are two outputs of fully differential comparator. Valid signal triggers the Flip flops in order to generate the clk_1-clk_{10} .
in the first 500 nano second of each cycle, valid is not generated because no comparison is done and no digital Bit is extracted, but in the rest of each period Valid is generated each 100nS and lasts for 50nS making a pulse with 50% duty cycle.

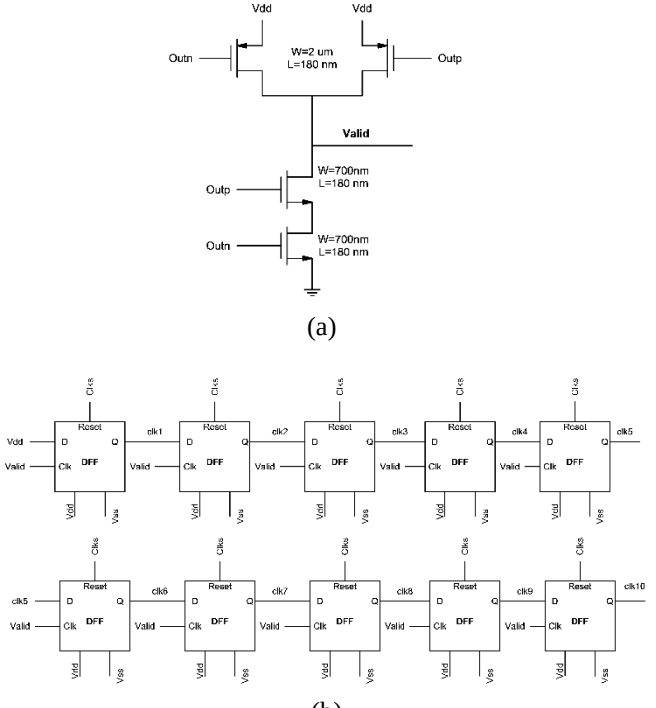


Fig.4. a) Generating valid signal b) Control Logic

2.4. DAC Control Logic

Figure.5 shows the schematic of proposed control logic and the new way of saving digital output bits of SAR ADC.

at the rising edge of CLK_i the comparator output is saved by a static flip-flop, consequently the relevant capacitor is switched from vdd to ground, or still remains connected to vdd (depends on result of the comparator, B_i). at the falling edge of CLK_i all capacitors are reconnected to V_{ref}. A common problem which previous designs suffer from, is that clk_i may triggers the AND gate before the output of Flip-Flop. in order to solve the mentioned problem in proposed circuit clk_i is not directly triggering the AND gate (made by a NAND and an inverter), but a delayed version of this signal named $Clkd_i$ triggers the AND gate. $clkd_i$ is simply generated by two inverters .

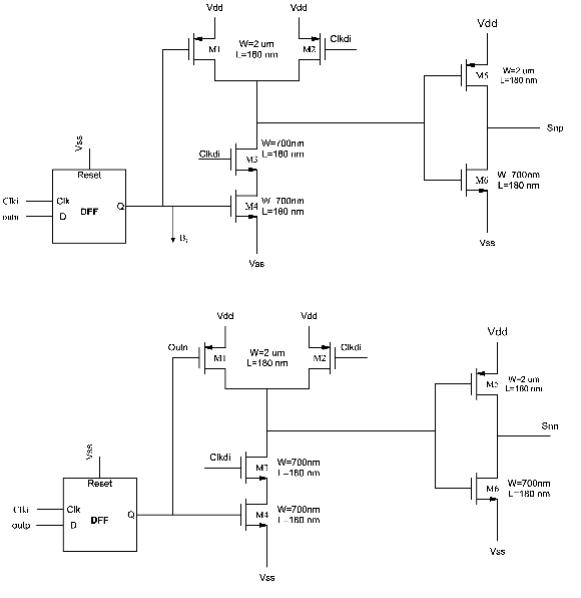


Fig.5 Proposed DAC Control Logic

2.5. D Flip-Flop

One of the most frequently used sub-circuits in SAR ADC is Flip Flop. Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption. The performance of the Flip-flop is an important element to determine the performance of synchronous circuit.
in proposed control logic two D Flip Flops are used to store each extracted bit and to control the switches, which increases the number of Flip Flops more. (30 Flip Flops are totally employed in this design) Since the proposed circuit is a low power ADC, its important to lower the power consumption of each D Flip Flop.

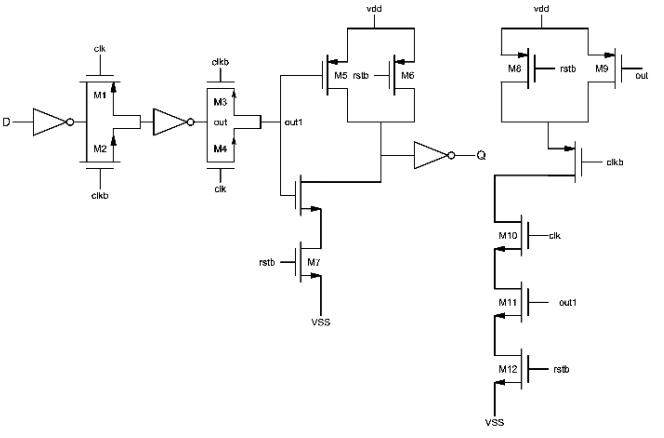


Fig.6 D Flip-Flop

Figure.6 illustrates the low power D Flip Flop designed for presented ADC.The minimum number of transistors are used in this design, in order to have the least power consumption.Clock to Q delay (t_{cq}) and D to Q delay (t_{dq}) of Dflip Flop are 160ps and 97ps respectively.

3. TIMING DIAGRAM AND SIMULATION RESULTS

Figure.7 demonstrates the timing diagram of proposed SAR ADC. The time of a full conversion is 1.5 us (since the sampling frequency is 666KS/Sec).in the first 500 nano Second of each cycle clks is in high level which resets all flip-flops in SAR and also makes the bootstrap switch on to pass the sampled analog signal. clkc is also high in this period, because no comparison is done and no valid signal is generated.

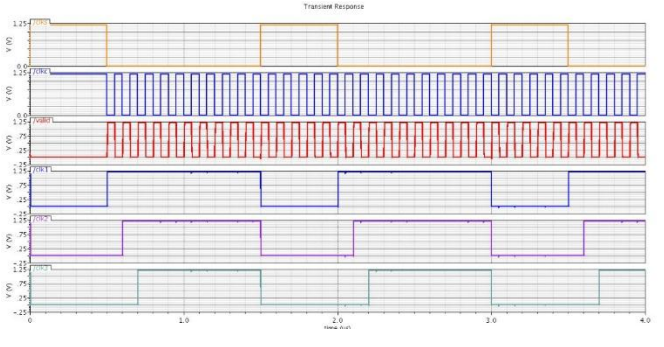
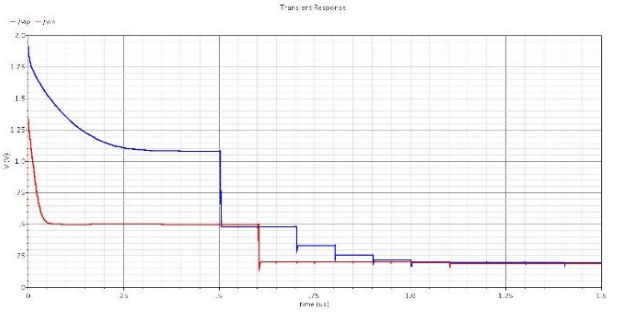
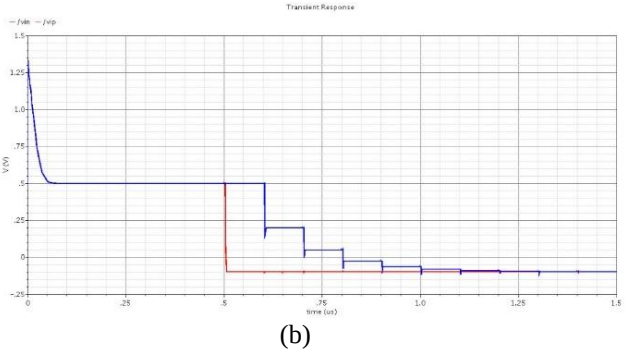


Fig.7 Timing Diagram of Proposed SAR ADC

In next 1u second the 10 digital bits are extracted. Each of these 100n seconds are divided into two parts. In the first 50nano second clkc in low and comparison is done and we have different values in outp and outn, One of the important differences between proposed architecture and conventional SAR ADC is that the common-mode voltage of DAC gradually decreases to ground. but in a conventional SAR ADC the common-mode is fixed .figure 6 show 2 example of constant input and extracting 10 digital bit.



(a)



(b)

Fig.8 converting 2 constant inputs to digital

(a) Vin+=1080m , Vin-=500m 1011110111
(b) Vin+=501m , Vin-=500m 1000000001

The frequency of sinusoidal input (shown in figure 7) is calculated using the following relationship:

$$p \times T_{in} = 2^K \times Ts \qquad (2)$$

where p is the number of input periods which is quantized, T_{in} is the input period, T_S is the sampling period and 2^K is the number of samples.
Assuming p=100, Ts= 1.5uS and 2^K =1024, Tin is 15.34us uS. So, the input frequency (f_{in}) is 65.1041Khz.

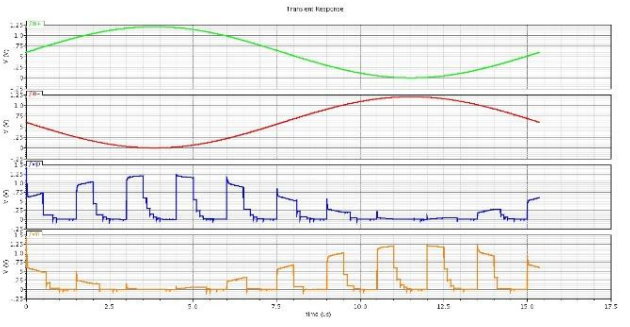
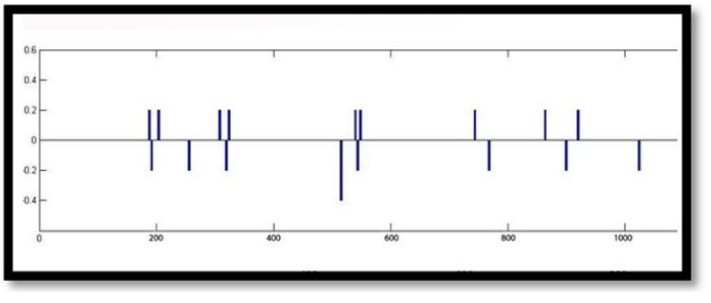
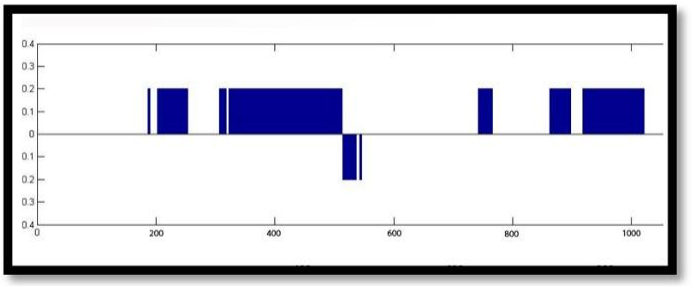


Fig.9 Input sinusoidal with frequency of 65.1041and 1.2 peak-to-peak voltage

Applying ramp input with proper duration, The DNL and INL of each code was calculated and the results are shown in figure 8. The measurements show maximum DNL and INL of -0.4/+0.2 and -0.2/+0.2 respectively.



(a)



(b)

Fig.10 Measured (a)INL (b)DNL of proposed SAR ADC

4. CONCLUSION

A 10-bit low power SAR ADC with a new logic control, using monotonic capacitor DAC array is proposed in this paper. the sampling rate is 666KS/Sec and total power consumption is 0.83mW. the SNDR of 53.6dB and ENOB 8.61 are achieved. The maximum DLN and INL for proposed ADC are 0.4 and 0.2 respectivly. all simulations are carried out in 0.18um CMOS technology using cadence simulating software

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