High efficiency class E power amplifier with a new output network

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ABSTRACT:

In this paper a new cascode class E power amplifier with a driving stage of class F and novel output network is proposed. Class F power Amplifier is able to produce square waves, used in driving of main stage, owing to use main frequency and third frequency harmonic. The proposed output network has also improved the parameters of circuit like efficiency, power added efficiency and output power with adding a capacitor and an inductor. In order to have more real results the circuit has been redesigned and simulated using spiral inductors.

The simulation has taken place using 0.18 μm CMOS technology in ADS simulator software based on IEEE 802. 11b utilized in 2.4 GHz and WLAN applications. Proposed circuit delivers 23.1 dBm power; out of a 1.8 supply voltage to a 50Ω load with 84.3% efficiency and 80.4 % power added efficiency in 2.4 GHZ operating frequency.

KEYWORDS: power added efficiency ,power amplifier, output network, driving stage, class E, class F.

1. INTRODUCTION

Class E Power amplifier was first introduced by Sokal in 1975. These amplifiers are nonlinear which could achieve 100% power efficiency when the whole power is delivered to the load. Class E, one of switching-mode amplifiers, consists of a load network and a voltage-controlled transistor as a switch. The conventional schematic of class E power amplifier is shown in figure1. An inactive network is employed in this circuit which could be a series resonant circuit (L-C) in the simplest way set in ω_0 frequency and used as a filter between drain and load. C_{shunt} consists of two capacitors: transistor intrinsic capacitor and a capacitor connected from drain to ground, added to reach better performance. Extra reactive element X has been used for providing some extra phase shift to achieve optimum operation. RF choke provides constant dc current to the circuit.

The maximum voltage and current of transistors are also other important figures of this amplifier which are calculated easily by driving the current and voltage of drain and equaling them to zero. A big amount of maximum drain voltage is considered as a great flaw for class E power amplifiers, Specially in CMOS technology we are facing a limitation in delivered output power or efficiency, because of low breakdown voltage of gate-oxide. The effect of ON- resistance transistor (R_{on}) in class E amplifier was investigated by *Choi* and *Long*. Increasing the width of transistor will lead to have less resistance for ON transistor and consequently less dissipation. On the other hand increasing the width of transistor will increase the input capacitor of transistor which also decreases the dissipation. In CMOS design there is a specific value for the size of transistors in which the power added efficiency is optimized.

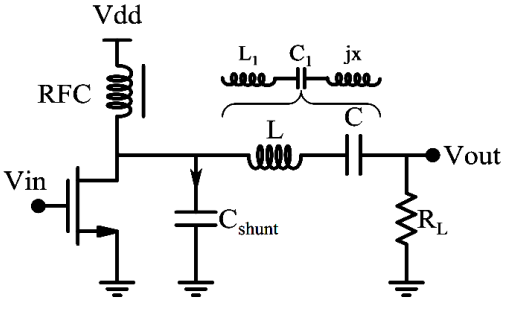

Fig1. Conventional class E power amplifier

2. PROPOSED CLASS E POWER AMPLIFIER DESIGN

A new design for improving the main parameters of a class E power amplifier like gain, efficiency and power added efficiency using 0.18μm CMOS technology has been proposed. It is used in 2.4 GHz frequency and WLAN applications based on IEEE802.11b standard. For this purpose a new network in output of the main amplifier (by adding some inactive elements to conventional output network) and

also a class F to drive stage of main amplifier (as stimulus input) have been added. In order to reach a better result cascode structure has been employed for both amplifiers. Class E Power amplifier with new output network in main amplifier is illustrated in figure 2. In order to have more real results the circuit has been redesigned and simulated using spiral inductors. The design of each element added to input and output of main amplifier and the advantages are discussed in following parts.

2.1. Preamplifier Stage Design

Class F Power amplifier is one of the employed methods for improving the efficiency of amplifiers (Figer2). Proposed cascode class-E PA with a driving stage of class F and novel output network using a load network is a common property in the output of these amplifiers which resonate in some other frequencies in addition to the fundamental frequency. This filter in output is actually put to control the harmonics of current and voltage of drain in order to form their waves which will cause to have less power dissipation on active devices of circuit.

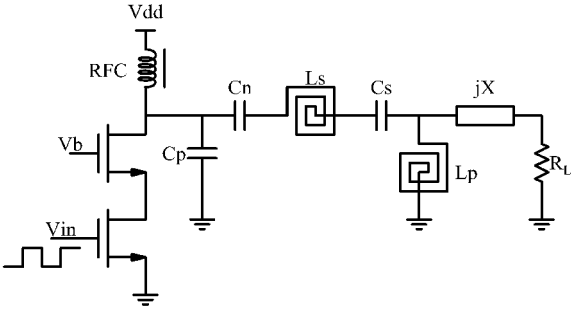

Fig2. Proposed class E power amplifier with new output network

This change will enhance the efficiency of circuit. The main purpose of using class F power amplifier as a drive stage is to provide sufficient gain for the small inputs and to shape the voltage waves in final stage. For an input of -10dbm power, the drive stage should be able to provide a 23 dB gain for final stage so that the final stage can be driven by an input of 13 dBm power, therefore the preamplifier stage should have high gain. Beside sufficient power preamplifier should also provide a suitable waveform for output stage. Trapezoidal wave is an ideal input for class E power amplifier. However it's hard to generate square wave signals at RF frequencies, one practical solution is to approximate the square wave by summing a finite number of harmonics which can be implemented in class F amplifiers. A practical solution for this problem is to approximate a square wave with combination of some frequency harmonics, which is achieved by designing amplifier class F. A class F power amplifier has been employed in proposed paper to drive the main stage. The amplifier is able to provide the square wave needed for driving the main stage by using the main frequency and the third harmonic. Figure 3 shows the whole class F drive stage used in this design.

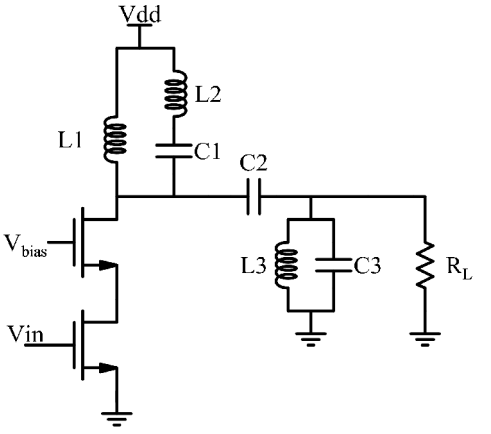

Fig3.Preamplifier stage of class F[12].

Resonance circuit, connected to power supply and drain of transistor, resonates at third harmonic frequencies. The transistor used in this stage should be biased in a way that amplifier works as a class-AB. The Cascode structure used here is for larger output impedance thus leading to higher gain.

2.2. A Design and analysis of matching network

The proposed output circuit in class E power amplifier is shown in Figure 2. This structure allows the amplifier to use higher load resistance and parallel capacitance and also improves the power capability of circuit. Increasing the efficiency of amplifier and parallel capacitance provides the enhancement of operating frequency for specific active device. Harmonic content level of resonant circuit are also decreased which provides higher quality coefficient compared to conventional class E structure. Parallel capacitor C_p comprises of linear output capacitor and intrinsic capacitor of transistor. Extra reactive element X has been used for providing some extra phase shift to achieve optimum operation. Capacitor C_n and inductor L_p, added to the circuit as a new design, have significantly enhanced the flexibility degree of circuit. For a transient analyze of presented circuit we have assumed the devices to be ideal and it's considered the switching-off and on periods are defined as:

$$\begin{cases} 0 < t \le \dfrac{\pi}{\omega} & OFF,\ R_{OFF} = \infty \\ \dfrac{\pi}{\omega} < t \le \dfrac{2\pi}{\omega} & ON,\ R_{ON} = 0 \end{cases} \quad (1)$$

The output voltage and current are:

$$i_o(t) = I_o \sin(\omega t + \varphi) \tag{2}$$

$$v_o(t) = I_o R \sin(\omega t + \varphi) \tag{3}$$

The voltage v_1 at the factious point is:

$$v_1(t) = V_1 \sin(\omega t + \varphi_1) \tag{4}$$

Where

$$V_1 = I_o R \sqrt{1 + \frac{X^2}{R^2}} \tag{5}$$

$$\varphi_1 = \varphi + \tan^{-1}\frac{X}{R} \tag{6}$$

At the drain, apply KCL and the result is given as

$$i_L(t) = i_C(t) + I_o \sin(\omega t + \varphi) + i_{SW}(t) \tag{7}$$

Where $i_L(t)$ and $i_c(t)$ are constrained by the physical characteristics of inductor and capacitor respectively, such as

$$V_{DD} - v_d(t) = L_1 \frac{di_L(t)}{dt} \tag{8}$$

$$i_C(t) = C_1 \frac{dv_d(t)}{dt} \tag{9}$$

When the switch is ON, $V_d(t)$ is kept zero. Hence $I_C(t)$ =0 during the ON state. And the relation between the supply voltage and the current flowing through the inductor is:

$$V_{DD} = L_1 \frac{di_{Lon}(t)}{dt} \quad for \quad \frac{\pi}{\omega} \le t \le \frac{2\pi}{\omega} \tag{10}$$

Inductor current while the transistor is ON, given by:

$$i_{Lon}(t) = \frac{V_{DD}}{L_1}\left(t - \frac{\pi}{\omega}\right) + C \tag{11}$$

In which C is a constant.
The capacitor current while the transistor is OFF is, given by:

$$i_C(t) = C_1 \frac{dv_d(t)}{dt} \tag{12}$$

The second- order differential equation is therefore obtained as:

$$L_1 C_1 i''_{Loff}(t) + i_{Loff}(t) = I_o \sin(\omega t + \varphi) \tag{13}$$

In which the inductor current while the transistor is OFF is:
(14)

$$i_{Loff}(t) = A\cos\omega_0 t + B\sin\omega_0 t + \frac{I_o}{1-\beta^2}\sin(\omega t + \varphi)$$

where $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$ $\beta = \frac{\omega}{\omega_0}$ $0 < t \le \frac{\pi}{\omega}$

To determine constants A,B and C certain boundary conditions should be applied .after computing the constants and putting needed conditions for optimized performance in a class E power amplifier including below conditions:

$$\begin{cases} v_d(t)\big|_{t=\pi/\omega} = 0 \\ \dfrac{dv_d(t)}{dt}\Big|_{t=\pi/\omega} = 0 \end{cases} \tag{15}$$

Solving some equations φ and I_o are calculated as below:

(16)

$$\cot\varphi = \frac{(1-\beta^2)\left(1-\cos\frac{\pi}{\beta}\right)^2 - \frac{\beta\pi}{2}\sin\frac{\pi}{\beta}\left(1+\cos\frac{\pi}{\beta}\right)}{\beta\sin\frac{\pi}{\beta}\left(1-\cos\frac{\pi}{\beta}+\frac{\pi}{2\beta}\sin\frac{\pi}{\beta}\right)}$$

$$I_o = \frac{V_{DD}(1-\beta^2)\left(1-\cos\frac{\pi}{\beta}+\frac{\pi}{2\beta}\sin\frac{\pi}{\beta}\right)}{L_1\omega_0\sin\varphi\sin\frac{\pi}{\beta}} \tag{17}$$

Output power and other parameters related to optimized design of class E power amplifier are too computable after finding output current equation, although the results of analytical equation is complicated for designing class E amplifier. For the same reason lots of researches have focused on offering design equation using numeric methods , but since there is a wide range for scattering coefficient (from zero to infinite) in designing Finite DC feed inductance (L_{dc}), interpolation methods don't offer acceptable results and so high degree differential equations are needed for analyzing. Because of parasitic resistance of inductor, Using a Finite DC feed inductance in power amplifier designing, would cause to a power dissipation in circuit.

The capacitor in output drain defines the maximum frequency of circuit. Smaller capacitors provide higher frequencies for power amplifier. Output drain capacitor (C_p) directly effects on performance of a class E power amplifier. Optimized condition for circuit is achieved if no charge of parallel capacitor is wasted while the transistor is ON, otherwise power dissipation is expected. Employing a parallel capacitor while the other parameters are constant will increase the charge and discharge time witch consequently enhance the power dissipation in power amplifiers. In an ideal power amplifier, power loss made by shunt capacitor is computed as:

$$P_{loss,switching} = \frac{1}{2} f C_1 V_{dsw}^2 \qquad (18)$$

In which v_{dsw} describes the drain voltage of transistor when the switch is OFF. The amount of other elements required for designing the amplifier have been calculated using proposed equations, table1 shows some of them. Cascode structure has been employed in this design in order to increase the bandwidth, reach a higher output power and overcoming the problems made by breakdown voltage of transistor.

Table1. Initial circuit parameters used in power stage

Name	Value
Operation frequency (f)	2.4 GHz
Required output power (P_0)	23dBm
Supply voltage(V_{DD})	1.8 V
Finite DC feed inductor (L_{dc})	3.807 nH
Optional load resistance (R)	8.1 Ohms
Excess reactance(X)	7.561 Ohms

Bias voltage for gate of upper transistor in cascode structure is computed as below:

$$V_{GG} > 3.6V_{DD} - BV = 1.2^{v} \qquad (19)$$

In cascode structure, the common gate transistors work in triode region. The drain capacitance consists of overlap capacitance, junction capacitance and sidewall capacitance.

Output power dissipated in load is:

$$Po = \frac{1}{2} . \frac{Vo^2}{R} \qquad (20)$$

Input DC power is define as:

$$P_{dc} = V_{dc} . I_{dc} \qquad (21)$$

The efficiency and power added efficiency of circuit are respectively calculated as below:

$$\eta = \frac{P_O}{P_{dc}} \qquad (22)$$

$$PAE = \frac{P_L - P_{in}}{P_{dc}} = \eta(1 - \frac{1}{G}) \qquad (23)$$

In witch the η is efficiency and G is the gain of amplifier.

3. SIMULATION RESULTS

Simulation results of proposed circuit, class E power amplifier, are discussed in this section. Simulations have been first done using ideal inductors and secondly by spiral ones. The results of both simulations are illustrated in table 2.

Simulations have taken place using 0.18µm CMOS technology in ADS simulator software, benefited in 2.4 GHz frequency and WLAN performance based on IEEE802.11b. It must be mentioned that the values of elements used in this design have been changed or optimized in ADS software after theoretical calculation in order to reach the best performance.

The proposed circuit is almost stable before input power changes and is able to deliver a constant power of 23dBm to load, so the amplifier shows an appropriate performance for variant inputs. Figure4 demonstrates the output power and PAE of proposed circuit and conventional class E versus input power.

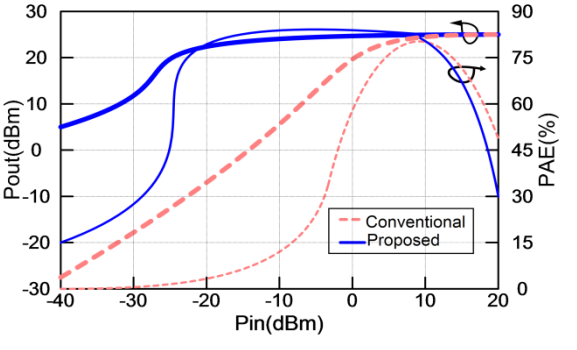

Fig4. Output power and power added efficiency of proposed and conventional class-E PA versus input power.

The presented amplifier is able to deliver a 23.1 dBm output power to 50 Ω load and 80.4% power added efficiency which are respectively 19dBm and 60% for conventional class E. Figure5 demonstrates the gain and efficiency of proposed circuit and conventional class E versus input power.

Proposed amplifier is able to deliver a 23.2 dB gain and 84.3% efficiency which are respectively 20dBm and 60.6% for conventional class E. As it's shown and described previously all parameters have been significantly improved in proposed circuit. Because of transistor switching, class E power amplifier is

considered as a nonlinear one, but in this paper choosing optimized sizes for active elements has significantly reduced this problem. as it was mentioned previously the size of active elements in class E power amplifier with 0.18µm CMOS technology play an important role in performance of circuit.

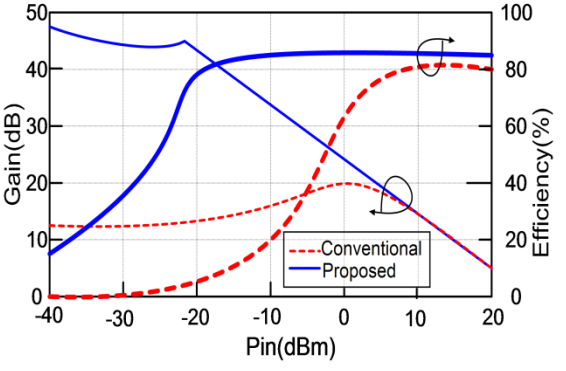

Fig5. Gain and efficiency of proposed and conventional class-E PA versus input power

In order to reach the best width for active elements the optimized size is calculated to be 1500 µm. considering parameters like Output power and power added efficiency may be important for selecting the best size.

A brief of results reached out of simulating proposed circuit is shown in table2. Also a comparison between simulation results of proposed class E (with ideal and spiral inductors), conventional class E power amplifier and results reported in references 5 and 12 is made in table 2.

Table2. Performance summary of CMOS class E PA

Results	802.11b Standard	Conv Class E	REF [5]	REF [12]	Proposed	
					spiral	*ideal*
Tech(µm)	--	0.18	0.13	0.18	0.18	0.18
fc (GHz)	2.4	2.4	2.4	2.4	2.4	2.4
Pout(dBm)	23	19	25	23	17.1	23.1
Gain(dB)	23	19.9	N/A	31	17.2	23.2
η(%)	--	61	N/A	N/A	69.5	84.3
PAE(%)	>50	60	38.8	42	62.1	80.4

4. CONCLUSION

Design and simulation of a cascode class E power amplifier with class F input stimulus stage and new output network is proposed in this paper. Proposed output network has improved circuit parameters like efficiency, power added efficiency and output power, adding some inactive elements. Designs have been done using spiral inductors In order to achieve more real results. Simulations have taken place using 0.18µm CMOS technology in ADS simulator software, benefited in 2.4 GHz frequency and WLAN performance based on IEEE802.11b.

The circuit is simulated for 2.4 GHz frequency with 1.8v supply voltage. Cascode structure has been employed for both class E and F power amplifiers in order to reach a higher output power and overcoming the problems like transistor breakdown voltage. 1500 µm has been chosen as an optimized width of active elements analyzing the performance of circuit.

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