Efficient Adder Cell Using GDI Structure

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ABSTRACT:
adder block is one of the major block in circuit design. inserting efficient adder block will cause having more efficient final design. In this paper improved GDI based adder will be designed. Proposed GDI based adder is more efficient compared to [2] and [4] in delay, performance and PDP. at last an adder/subtractor circuit will be designed.

KEYWORDS: adder, GDI cell, digital circuit

1. INTRODUCTION

The performance of the integrated circuits is influenced by how the arithmetic operators are implemented in the cell library. As more complex arithmetic circuits are presented each day, the power consumption becomes more important. The arithmetic circuits grow more complex with the increasing processor bus width, so energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on a chip and faster clock. Increasing demand for fast growing technologies in mobile electronic devices such as cellular phones, PDA's and laptop computers requires the use of a low-power Full Adder in VLSI systems since it is the core element of arithmetic circuits [1].

Addition is a very basic operation in arithmetic. Subtraction, multiplication, division and address calculation are some of the well-known operations based on addition. These operations are widely used in many VLSI applications, since the full adder cell is the building block of the binary adder, enhancing the performance of the 1-bit full adder is a significant goal and has attracted much attention [2].

The design criteria for full adder are usually multifold. Transistor count, which is one of the attributes, determines the system complexity of arithmetic circuits like multiplier, Arithmetic Logic Unit (ALU), etc. Power consumption and speed would be the other two important criteria when it comes to the design of full adders. Power delay product or energy consumption per operation has been introduced to accomplish optimal design tradeoffs. The performance of digital circuits can be optimized by proper selection of logic styles. Different logic styles tend to favor the accomplishment of one performance aspect at the expense of others. The logic styles are varied in the method of computing intermediate nodes, the number of transistor count, though they are implementing the same function. Numerous full adder designs in the classes of static CMOS, dynamic circuit, transmission gate, GDI logic and Pass Transistor Logic (PTL) are existed. The well-known static CMOS adders with complementary pull up PMOS and pull down NMOS network require 28 transistors for generating sum and carry outputs. PTL is an alternative to CMOS and offers most functions implementations with fewer transistors [3].

GDI logic is introduced as an alternative to CMOS logic. It is a low power design technique which offers the implementation of the logic function with fewer numbers of transistors. GDI gates provide reduced voltage swing at their outputs, i.e. the output high (or low) voltage is deviated from the VDD (or ground) by threshold voltage Vt. The reduction in voltage swing is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation. At low VDD operation, the degraded output may even cause circuit malfunction. Therefore, special attention must be needed to achieve full swing operation. [3]in next section we will introduce GDI structure with more details. proposed adder based on GDI structure will be introduced in section 3.

2. GDI STRUCTURE

Gate diffusion input (GDI) is a novel technique for low power digital circuit design in an embedded system.

This technique allows reduction in power consumption, delay and area of the circuit. This technique can be used to reduce the number of transistors compared to conventional CMOS design. GDI is very flexible for digital circuits. Although GDI has the above advantages, it still has some difficulties that are needed to be solved. The major problem of a GDI cell is that it requires twin-well CMOS or silicon on insulator (SOI) process to realize. Thus, it will be more expensive to realize a GDI chip. However, if only standard pwell CMOS process can be used, the GDI scheme will face the problem of lacking driving capability which makes it difficult to realize a feasible chip.

The basic GDI cell is shown in Fig. 1. Though it resembles a conventional CMOS inverter the source/drain diffusion input of both PMOS and NMOS transistor is different. In conventional inverter circuit, source and drain diffusion input of PMOS and NMOS transistors are always tied at VDD and GND potential, respectively. On the other hand, the diffusion terminal acts as an external input in the GDI cell. It helps in the realization of various Boolean functions such as AND, OR, MUX, INVERTER, F1 and F2, as listed in Table 1. This feature gives the GDI cell two extra input pins to use which makes the GDI design more flexible than a usual CMOS design. However, this feature is also the major cause of its disadvantage: special CMOS process required. To be more specific, the GDI scheme requires twin-well CMOS or silicon on insulator (SOI) process to implement which is of course more expensive than the standard p-well CMOS process [5].

The main drawback of GDI gate is that it suffers due to threshold voltage drop. This reduces current drive and affects the performance of the gate. The output voltage reduction can be compensated by the use of swing restoration buffers at the output.

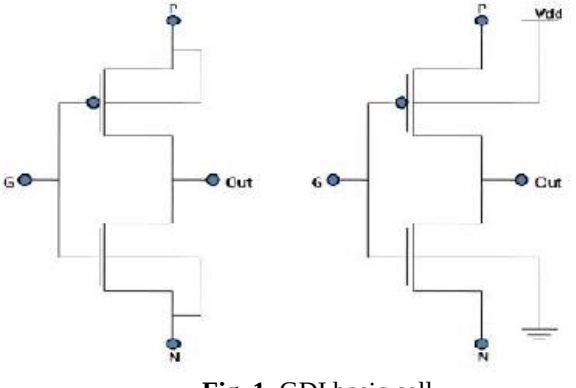

Fig. 1. GDI basic cell

Table 1. Different logic function realization using GDI cell

N	P	G	OUT	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	A + B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

Table 2. Various functions of GDI

FUNCTION	*GDI*	*CMOS*
INVERTER	*2*	*2*
FUNCTION1	*?*	*6*
FUNCTION 2	*2*	*6*
OR	*2*	*6*
AND	*2*	*6*
MUX	*2*	*12*
XOR	*4*	*16*
XNOR	*4*	*16*
NAND	*4*	*4*
NOR	*4*	*4*

It can be seen from table 2 that using GDI technique AND, OR, Function1, Function2, XOR, XNOR can be implemented more efficiently than CMOS structure. However, to implement NAND, NOR it requires 4 transistors as that in Static CMOS design. [4]. Figure2 and 3 show different circuit for full adder which is designed by [4].

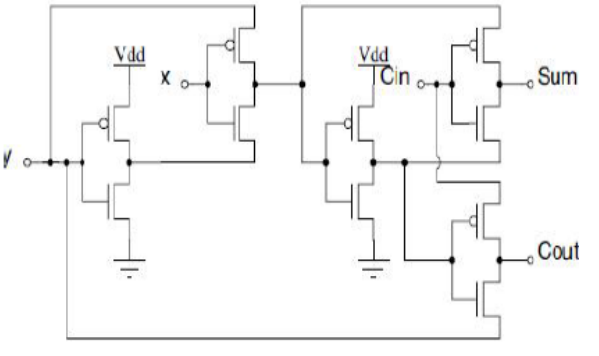

Fig. 2. GDI XOR full adder [4]

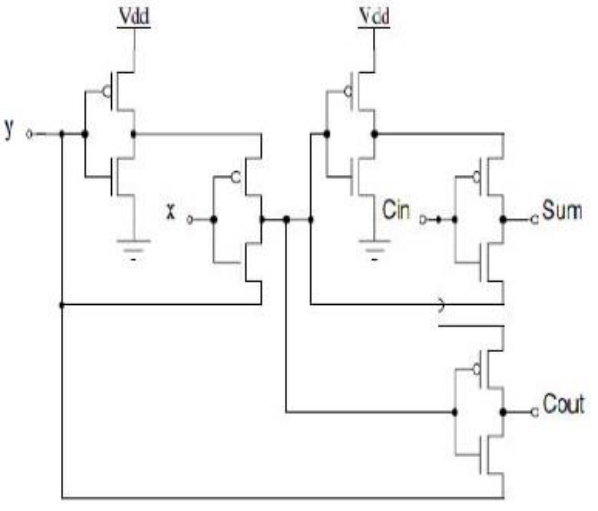

Fig. 3. GDI XNOR full adder [4]

Adder formula in [4] is:

Sum= Cin (A XNOR B) OR not (Cin)(A XOR B) (1)

Cout = Cin(A XOR B) + B(A XNOR B) (2)

The simulation analysis in [4] shows that the GDI technique is novel and an effective technique for reducing power consumption, delay, power delay product (PDP) area and the Transistor count which will effectively reduce the size of the chip. GDI will allow high density of Fabrication as now a day's chip area is very important parameter. With respect to chip area, power consumption and transistor count, GDI technique is significantly advantageous over CPL and DPL [4].

Simulating [4] in Hspice in 90nm*40nm dimension and with capacitance 0.3 ff and voltage 1.7 shows below results;

Delay: 2.1 *e-11

Power: 9.1* e-1

PDP: 1.9 * e-11

However, the presence of inverters in the buffers increases the transistor count and also increases the static power consumption when they are connected in cascade. This approach utilizes low threshold transistors in the places where a voltage drop is to occur and also high threshold transistors for the inverters. Though this hybrid threshold voltage method minimizes power consumption, it becomes a bottleneck at the transistor fabrication process.

one method of swing restoration of GDI based is full adder output, using an Ultra-Low Power Diode (ULPD) technique. This technique configures the MOS transistor to work as a diode and uses 8 additional transistors for providing full swing. It mitigates the problem of static power dissipation as a conventional swing restoration buffer but still the complexity issue in the fabrication of ULPD is to be taken into account [3].

in [2] new structure for GDI based full adder is presented using ULPD. By considering the full adder's Truth-Table, it can be seen that Cout is equal to (A AND B) when Cin='0', and Cout is equal To (A OR B) when Cin='1'. Thus, a multiplexer can be used to obtain the Cout output. Following the same criteria, the SUM output is equal to (A OR B OR Cin) when Cout='0', and SUM is(A AND B AND Cin) when Cout='1'. Again, Cout can be used to select the respective Value for the required condition, driving a multiplexer. Hence, an alternative logics scheme to design a full adder cell can be formed by AND, OR and MUX logic blocks as shown in Fig. 4.

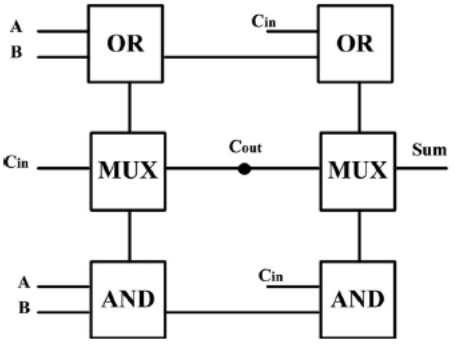

Fig.4. Novel and alternate logic scheme for designing full adder cell [2]

As can be seen ULPD level restorer is used to provide full swing output. This novel design takes advantage of using GDI technique which is proved as one of the effective structures in designing Low-Power circuits. This new approach minimizes both static and dynamic power consumption. This design uses ULPD level restorer to eliminate the leakage current and also providing good driving capability which is necessary in a cascaded situation. Using ULPD as level restorer eliminates the need for output buffers which are the main source of static power consumption. This design also uses 20 transistors and has low dynamic power dissipation due to its low switching capacitance. Figure 5 shows use of ULPD level restorer in figure 4 [2].

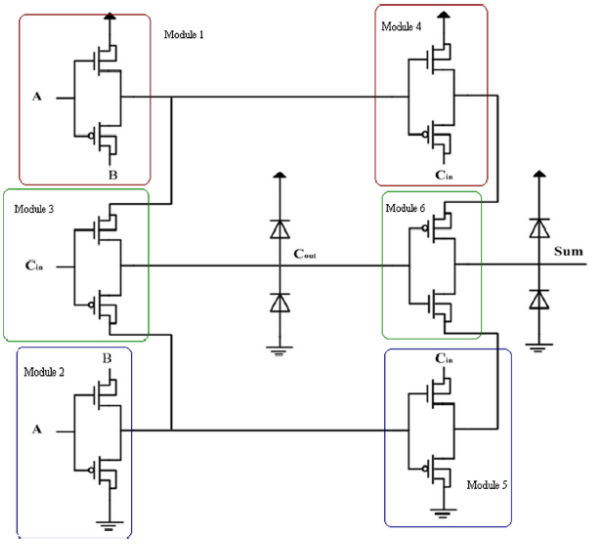

Fig. 5. Proposed GDI-MUX full adder [2]

Simulating [2] in Hspice in 40 * 90 nm dimension and capacitance 0.1 ff and valtage 1.2 shows belw results:

Delay: 3.4 *e-11

Power: 3.3* e-4

PDP: 1.1 * e-14

In next section proposed adder will be defined and comparison with [2] and [4] will be presented.

3. PROPOSED GDI ADDER CIRCUIT

Figure 6 shows proposed adder circuit using GDI structure which reduced level of cascading and restoration. This circuit in compare to figure 5 has many advantages. The first advantage is that 'select' pin of last mux is not cascaded from another mux and it is connected to 'cin'. So there is no need to add ULPD diode to restore voltage level. next advantage is decrease in number of transistor. Figure 6 in compare to figure 3 has less delay which is equal to 3 GDI cell but figure 3 has delay equal to 4 GDI cell.

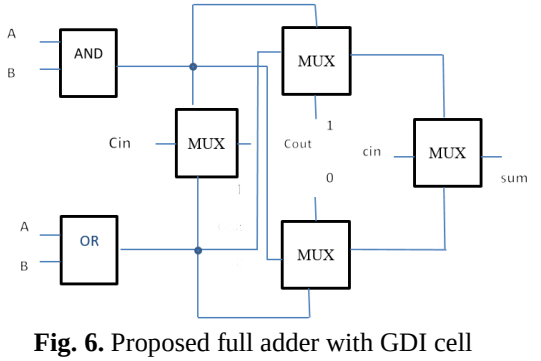

Fig. 6. Proposed full adder with GDI cell

The logic function of proposed full adder can be represented as:

Sum= Cin (A XNOR B) OR not(Cin) (B XOR A) (3)

Cout = (B AND A) not (Cin) + (A OR B)Cin (4)

From Eqs. (4) and (3) three basic gates are needed for implementing the function i.e., AND, OR and XOR.

Result of simulation in Hspice for proposed adder with 1.2 voltage and 90 * 40nm dimension and 0.1ff capacitance presented in table 3.

proposed addr is better than [2] and [4] in delay, power consumption and PDP according to Hspice result in table 3.

Table 3. Comparison between [2], [4] and proposed adder

	Proposed GDI based adder	[2]	[4]
Delay	2*e-11	3.4*e-11	2.1*e-11
Power	1.3* e-4	3.3* e-4	9.1*e-1
PDP	2.7 * e-15	1.1 * e-14	1.9*e-11

We can modify figure 6 in order that addition and subtraction done in parallel. Figure 7 shows this circuit. There are many applications that need to add and subtract in parallel to improve the speed. According to table 4 we can see that add and subtract has same truth table for carry out and borrow out pin. Table 4 shows the truth of figure 7.

One of the application of circuit in figure7 is in Residue Number Systems (RNS). Two common module in RNS is 2n-1 and 2n+1. Every input in these two modules will be calculated with one addition and one subtraction concurrently. Figure8 shows this circuit which can be implemented with one modules of figure7 [6]. As a result of using figure7 in implementing figure8, 9 GDI module will be consumed but if figure6 be used, 12 GDI will be needed.

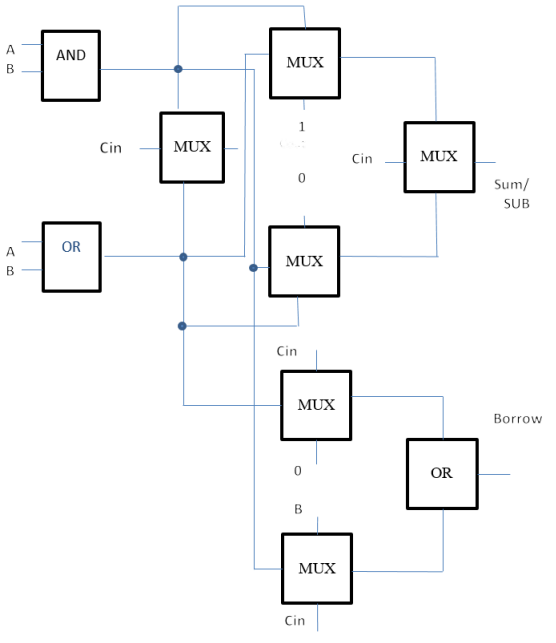

Fig. 7. Proposed adder/ subtractor circuit

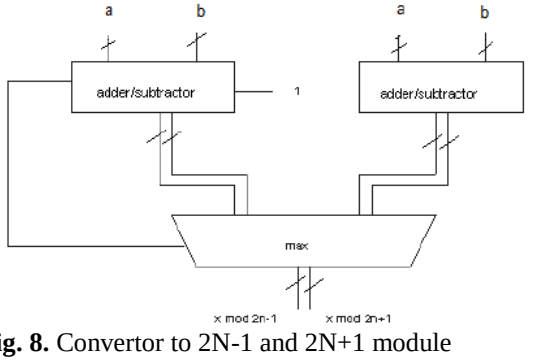

Fig. 8. Convertor to 2N-1 and 2N+1 module

Table 4. Truth table of add and subtract operation

A	B	Cin/Bin	Sum	Cout	Sub	Bout
0	0	0	0	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	1	0	0
1	1	1	1	1	1	1

4. CONCLUSION

One of the major module which effect the performance of circuit is adder. In this paper we proposed an efficient adder based on GDI module and improved that proposed adder was better than [4] and [2] in power, delay and PDP. At last an adder/subtractor circuit based on GDI was proposed for speed up an application which needs both addition and subtraction. Proposed adder circuit/subtractor improve both delay and price.

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