Design of a Sigma Delta modulator for wireless communication applications based on ADSL standard

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ABSTRACT:
This paper proposes and simulates a fourth order single-loop modulator with feed forward structure which covers the ADSL-standard bandwidth. Design of this modulator employs a low distortion structure suitable to target bandwidth to achieve its objectives. To achieve the required specifications of target standard, a fourth order modulator with oversampling rate of 14, bandwidth of 1.2 KHZ, SNR of 87 dB, and accuracy of 14.2 bits is designed and simulated. Block diagram of the proposed structure is also presented.

KEYWORDS: Analog to Digital Converter, Sigma-Delta Modulator, Low-power components, Low voltage, Wideband

1. INTRODUCTION

Data converters are one of the most important blocks in telecommunications and computer systems as well as other applications, and cover a wide range of accuracies and bandwidths. In most communication standards, high dynamic range, high bandwidth, low distortion and low noise level are of the utmost importance. On the other hand, wide use of portable communication devices have increased the importance of integrating higher number of communication channels on smaller chips with lower power consumption. Sigma-Delta converter is a low cost converter which offers high integration, high dynamic range, and most importantly high signal to noise ratio (SNR). Another important advantage of sigma delta converter is an important function called noise shaping, which distinguish it from other converters. Also, the advancement of related technologies and integration of analog to digital converters (ADC) on low-power small chip has encouraged the researchers to design new suitable structures that would be able to process large input signals without any problem. Power loss, signal to noise ratio and output bit rate (accuracy) are the most important standard characteristics of an ADC. In Sigma Delta (SD) converters, usually a reduced oversampling rate (OSR) is implemented to achieve a higher bandwidth, which leads to increased sensitivity, increased non-ideal circuit effects and reduced performance of converter. But a number of measures such as increasing the order of modulator and increasing the bits of quantizer can be taken to overcome these challenges. SD-based converters have several components including the integrator, adder, discretizer and at least one digital to analog converter in the feedback section. This paper designs and simulates a SD modulator with feed forward topology to provide minimum specifications required by a ADSL system. In the second section the structure of wideband systems is discussed and in the third section the proposed structure is presented. The results are presented in the fourth section.

2. THE WIDEBAND STRUCTUREHNICAL WORK PREPARATION

Figure 1 shows an overview of the structure of a wideband receiver designed to meet the standard specifications of wireless communications such as ADSL. This standard needs a high resolution average speed converter. For signals with relatively moderate to high bandwidth (in ADSL for example) achieving the required specification requires using a small oversampling rate (OSR) [7][5], and only an appropriate design can meet such specifications. To achieve the desired accuracy, one can increase the number of discretizer's bits, the order of modulator, or oversampling rate (OSR), but in broadband standards

such as ADSL, OSR cannot be increased over a certain amount [5], [6].

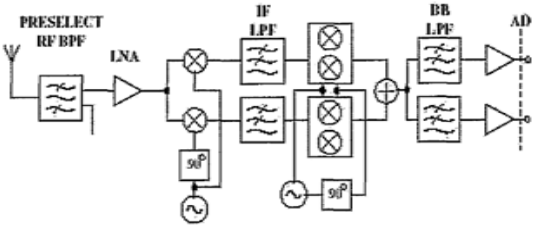

Fig. 1. Wideband receiver [6]

3. THE PROPOSED STRUCTURE

In this paper, a single-level fourth order structure with Feed forward topology is designed to cover the bandwidth corresponding to the ADSL standard. This design is presented in Fig.2. The proposed design employs a three-bit discretizer and four integrators, two delayed and two undelayed. Design uses a low distortion structure because of very high suitability for wideband applications. Output Swing of the amplifier used in the integrator is limited by the power supply; in practice this amount is less than ideal because of a voltage drop in the output transistors that are in saturation region. In this structure, since input signal does not directly enter into modulator loop, output swing of the integrator of direct path from the of first integrator's output to the input is obtained using equations (1) and (2) ,noise transfer

4. SIMULATION RESULTS

Figure 3 shows the ideal modulator output spectrum for ADSL standard for input frequency of 0.6 MHZ, bandwidth of 1.2 MHZ and sampling frequency of 33.6 MHZ.

However, non-ideal effects such as sampling jitter or deviation from the ideal sampling, sampling noise or the which is due to sampling capacitor of modulator's first level and also OP-AMP non-ideal effects including limited gain, limited bandwidth, rotation speed and OP-AMP noise all can have negative effects on the performance of the modulator [6].

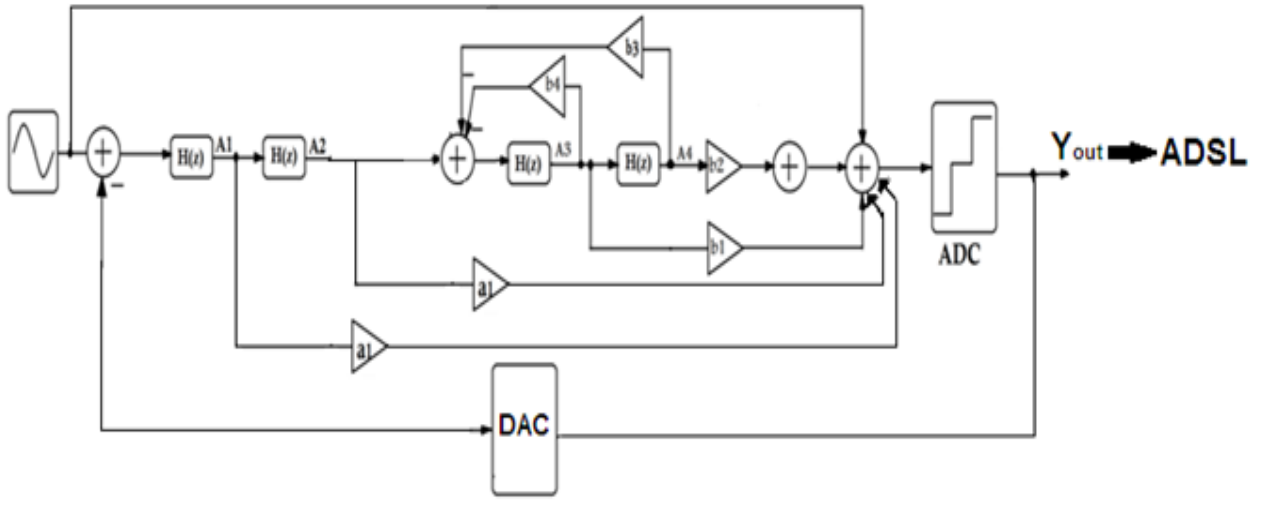

Fig. 2. the proposed structure for ADSL standard

Function (STF):

$$STF=1 \quad (1)$$

$$NTF=(1-Z^{-1})^4 \quad (2)$$

Also, the signal to noise ratio is in the form of equation (3):

$$SNR=6.02N+1.76-12.9+50\log OSR \quad (3)$$

where OSR is the oversampling rate and N is the number of modulator output bits. According to the equation (3), it is clear that doubling the OSR, increases the SNR by 15 dB and consequently improves the accuracy by 2.5 bits. Also, the modulator coefficients are optimized such that we can expect the best output from modulator.

Figure (4) shows the output after applying jitter non-ideal effects. This figure indicates that as jitter or deviation decreases, output comes closer to the ideal state. Also, Figure (5) shows the output after applying non-ideal effects of sampling noise. This figure indicates that sampling capacitor should be much smaller or much larger than a certain limit, because

when it gets too large, modulator consumes too much power, and when this capacitor is too small effect noise becomes significantly high, and both scenarios have adverse effects on the modulator output. Table 1 presents the results of simulation after applying all non-ideal effects. Figure 6 shows the diagram of the proposed structure for the ADSL standard.

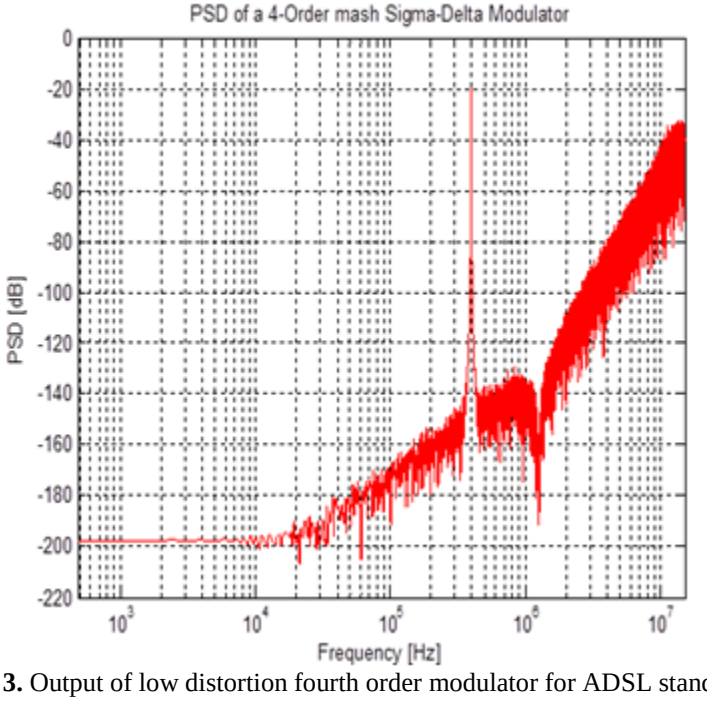

Fig. 3. Output of low distortion fourth order modulator for ADSL standard

Table 1: simulation results

Standard	ADSL
Bandwidth	۱.۲ MHZ
Sampling Rate (OSR)	۱4
Sampling frequency	33.6 MHZ
Input Frequency	.6 MHZ
Signal to Noise Ratio	87 db
Accuracy	14.2

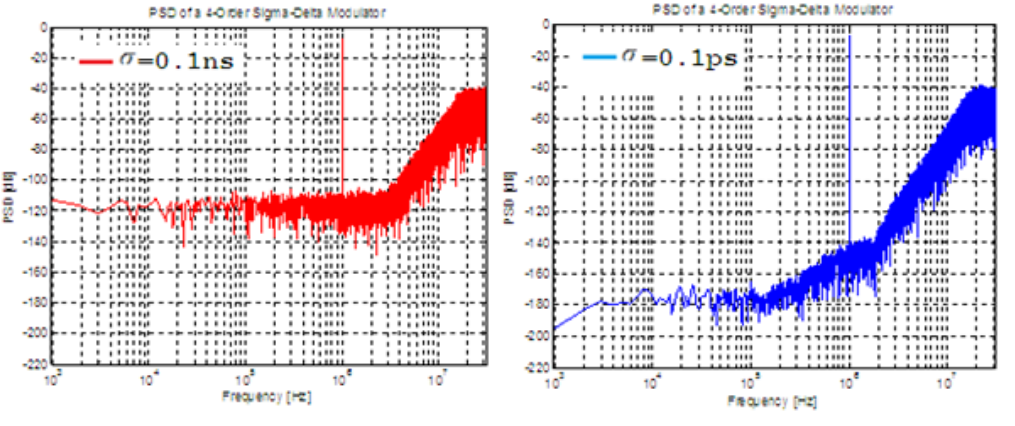

Fig. 4. The effect of clock jitter on modulator: a) deviation of 12 ps b) deviation of 12 µs

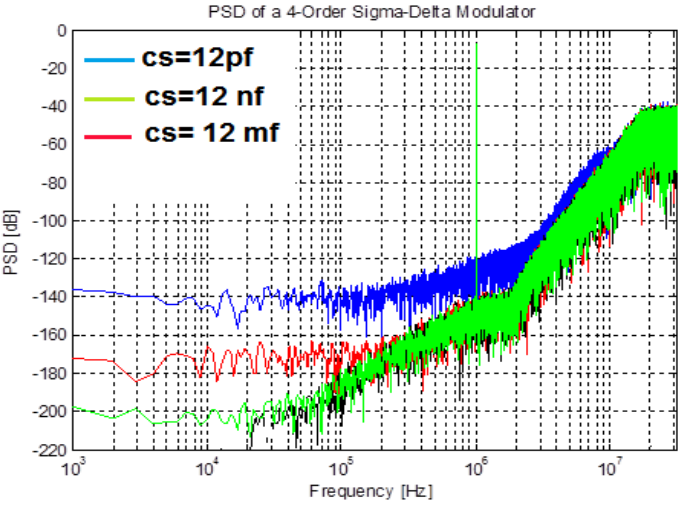

Fig. 5. The effect of sampling capacitor noise on the modulator

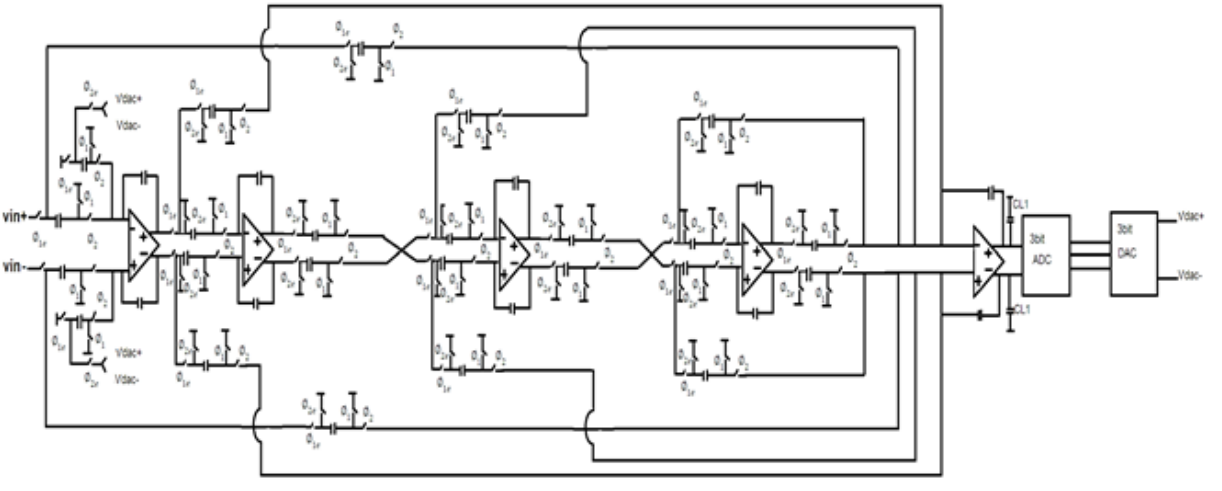

Fig. 6. Diagram of the proposed structure for ADSL standard

5. CONCLUSION

Nowadays, the wide use of small power supplies for integrated circuits and the increased need of new systems to more bandwidth have highlighted the importance of designing new Analog-to-digital converters for this type of applications. Reducing the power consumption and achieving the desired accuracy for different standards are the major objectives in designing this type of converters. Therefore design and fabrication of Sigma Delta modulators can be one of the most important academic and industrial projects in this regard. This paper proposed a fourth order single loop modulator with feed forward structure, which operates with an oversampling rate of 14, bandwidth of 1.2 MHZ, and accuracy of about 14.2 bits.

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