A 0.5V, 900uW CMOS OTA Using Bulk Driven and Hybrid Compensation Technique

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ABSTRACT
An ultra-low-voltage ultra-low-power operational transconductance amplifier (OTA) is presented in this paper. The proposed topology based on a bulk driven input differential pair. Two separate capacitors have been used for compensation of the opamp where one of them is used in a signal path and another one in a non-signal path. The circuit is designed in the 0.18µm CMOS technology. The simulation results show that the amplifier has a 84.1dB open-loop DC gain and a unity gain-bandwidth of 81 KHz while operating at 0.5V supply voltage. The total power consumption is as low as 900nW which makes it suitable for low-power bio-medical applications.

KEYWORDS:-Ultra Low Power, Ultra Low Voltage, Operational Transconductance Amplifier, Bulk Driven, Hybrid Compensation.

1. INTRODUCTION

As the size of modern CMOS processes scale down, the maximum allowable power supply continuously decreases. The main drawback on implementing low-voltage CMOS circuits is the threshold voltage which does not scale down as the same rate as power supply reduction. To combat this conflict without requiring the development of expensive CMOS technologies with lower threshold voltages, novel circuit design techniques must be developed that are compatible with future CMOS technologies [1].

A promising approach in low voltage analog circuits is the "bulk-driven" MOSFET method. In this method, the gate to-source voltage is set to a value sufficient to form an inversion layer, and an input signal is applied to the bulk terminal. In this manner, the threshold voltage of a MOSFET can be reduced or even removed from the signal path. One important drawback of the bulk-driven method, however, is that the body transconductance g_{mb} is approximately five times smaller than the gate transconductance g_m. Thus, when the input differential pair of an amplifier is composed of bulk-driven transistors, the resulting DC gain is relatively low.

In this paper, a 0.5 volt OTA using weak inversion MOSFETs is presented. The presented OTA is also designed using bulk-driven method and the simulation results are compared to each other.

I. WEAK INVERSION OPERATION

The drain current I_{ds} of a MOS transistor in weak inversion is based on the channel diffusion current and can be given by (1), when referred to source voltage [1];

where I_s is the characteristic current, T the absolute temperature, n the inclination of the curve in weak inversion, K the Boltzmann constant, q the charge of the electron or hole. This expression is a consensus among the model BSIM3v3 [1]

$$I_{DS}=I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}}{nKT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{KT}\right)\right] \quad (1)$$

Observe that if $V_{ds} \geq 3KT/q$ then the transistor will be saturated in weak inversion [3]. The transconductance g_m can be found as presented in (2), which is a function of current I_{ds} and factor nkT /q only

$$g_m=q\frac{I_{DS}}{nKT} \quad (2)$$

The dc parameters of the MOS transistor in weak inversion operation can easily be found using the minimum square method given by [4]. The transconductance gmb can be found as given in (3), where γ is the body efffect coefficient and φ_f is the Fermi potential [2]

$$g_{mb}=\frac{\gamma}{2\sqrt{2\phi_F-V_{SB}}}g_m \quad (3)$$

The transconductance g_{mb} varies from 20% to 30% of g_m for the same transistor in a CMOS process [2]. Therefore, it is possible to predict g_{mb} from g_m , and thus obtain the sizes of the transistors working in weak inversion.

2. DESIGN OF THE PROPOSED BULK DRIVEN OTA

The circuit of the proposed operational transconductance amplifier (OTA) is shown in Fig. 1.

A bulk driven differential pair allows low-voltage operation of Miller OTA. Observe that transistor pairs M_{3a}-M_{3b} and M_{4a}-M_{4b} form composite transistors. They allow the differential pair active load and the common gate amplifier to be biased by the same potential, without the use of additional biasing sources. From the composite transistor equations, it is possible to conclude that V_{ds3} is given by (4)[5]. An analogous expression is obtained for V_{ds4a}.

$$V_{ds\,3a} = \frac{KT}{q}\ln\left(1 + 2\,\frac{(W/L)_{3b}}{(W/L)_{3a}}\right) \tag{4}$$

In terms of dc analysis, voltages V_{ds3a} and V_{ds4a} are equal and constant. Therefore, voltages V_{ds1} and V_{ds2} should be equal and constant, thus optimizing matching of differential pair M_1 and M_2, consequently reducing the differential offset voltage. The dimensions of transistors M_8 and M_9 should be carefully matched in order to avoid unbalance in the structure of the differential pair. In order to avoid any systematic offset it is possible to derive an equation as follows.

$V_{gs6} = V_{ds4b} + V_{ds4a}$. (5)

And

$V_{gs3a} = V_{ds3b} + V_{ds3a}$. (6)

So

$V_{gs6} = V_{gs3a}$. (7)

With respect to (6) and (7) we can write

$I_{ds3a} = (W/L)_{3a} / (W/L)_6 \times I_{ds6}. = I_{ds8} + I_{ds5}/2$ (8)

Therefore,

$$(W/L)_6 = \frac{2(W/L)_{3a}(W/L)_7}{2(W/L)_8 + (W/L)_5} \tag{9}$$

There will be no systematic offset voltage as long as (9) is satisfied. Although, the weak inversion operation implies large transistors dimensions, it minimizes the noise effect, especially flicker noise which is important in a MOS transistor in low-frequency applications . Now, the open loop gain is given by

$$A_0 = \frac{g_{mb1}\,g_{m6}}{g_{o67}\left(\dfrac{g_{oB} + g_{o9}}{g_{m4b} + g_{mb4b} + g_{o4b}}\,g_{o24a} + \dfrac{g_{o11}\cdot g_{o9}}{g_{m11}}\right)} \tag{10}$$

Clearly, a disadvantage of the Miller frequency compensation technique is the inconvenience of the right half plane (RHP) zero. This RHP zero degrades the phase margin and leads to instability of operational amplifiers.

In this work, the output impedance of the first stage is increased, mainly thanks to the employed transistor M_{4b}, thus, the DC gain is improved. The unity-gain bandwidth is also enhanced using two gain-stage (common-gate) in the Miller capacitor feedback path. Consequently, the gain-bandwidth product (GBW) is considerably enhanced.

Fig.1 shows a two-stage OTA composed of folded-cascode as the first stage and the common-source amplifier as the second stage that employs hybrid cascode compensation. It is worth mentioning that this OTA structure has been chosen for its simplicity and the compensation method can be applied to the other two-stage OTAs. As shown in Fig. 1 two separate capacitors, C_2 and C_1, have been used for compensation of the opamp where C_2 is used in a signal path and C_1 in a non-signal path. In Fig. 2 the small signal equivalent circuit for differential inputs is shown. The small signal equations of the circuit shown in Fig.1 are as follows:

$$g_{mb1}v_{in} + \frac{v_a}{R_A} + sC_A v_a + (g_{m4b} + g_{mb4b})v_a + sC_2(v_a - v_{out}) = 0 \tag{11}$$

$$\frac{v_b}{R_B} + sC_B v_b - (g_{m4b} + g_{mb4b})v_a - g_{m11}v_c = 0 \tag{12}$$

$$\frac{v_c}{R_C} + sC_C v_c + g_{m11}v_c + sC_1(v_c - v_{out}) = 0 \tag{13}$$

$$g_{m6}v_b + sC_1(v_{out} - v_c) + \frac{v_{out}}{R_L} + sC_L v_{out} + sC_2(v_{out} - v_a) = 0 \tag{14}$$

Where R_A, R_B, R_C, R_L and C_A, C_B, C_C, C_L are the resistances and capacitances seen at the nodes A, B, C, and output, respectively.

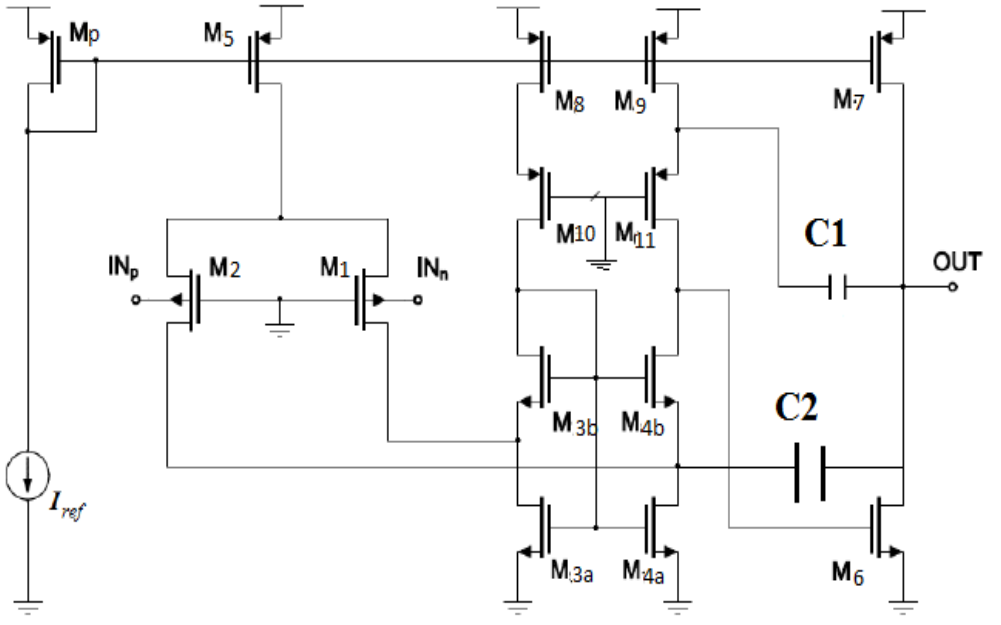


Fig. 1. Schematic of the proposed OTA circuit

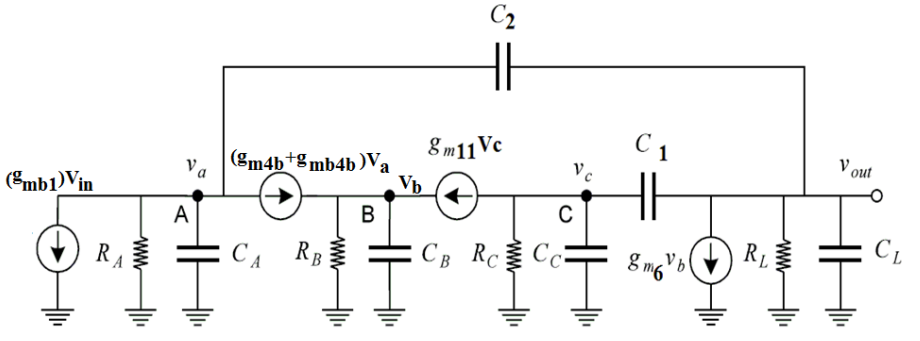


Fig. 2. the small signal equivalent circuit for differential inputs

After lengthy derivation, the system has three zeros and four poles [8]. The zeros are obtained as follows:

$$s_{z1} = -\frac{g_{m11}}{C_2 + C_c} \tag{15}$$

$$s_{z2,3} \approx \pm\sqrt{\frac{(g_{m4b} + g_{mb4b})g_{m6}}{C_1 C_B}} \tag{16}$$

Two zeros are at the left half plane and one is located at the right half plane. But, since the right half plane zero is at a high frequency, it does not affect the system behavior.

To obtain the dominant real pole it is assumed that its value is much smaller than the other poles. The poles are obtained as follows:

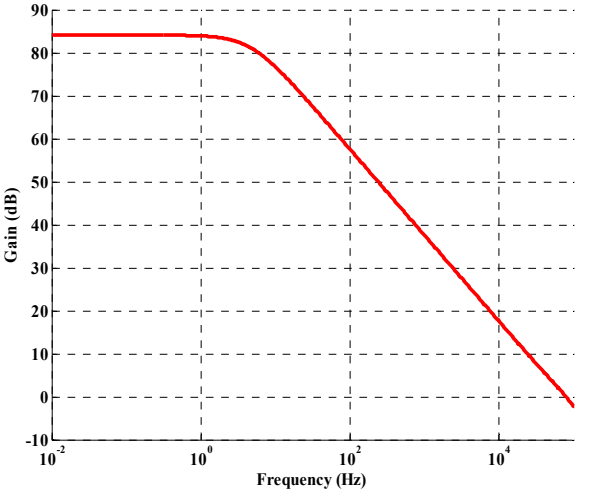
$$s_{p1} \approx -\frac{1}{(g_{m4b} + g_{mb4b})(C_2 + C_1)R_L R_B} \tag{17}$$

$$s_{p2} \approx -\frac{(g_{m4b} + g_{mb4b})g_{m11}(C_2 + C_1)}{C_2 C_1((g_{m4b} + g_{mb4b}) + g_{m11})} \tag{18}$$

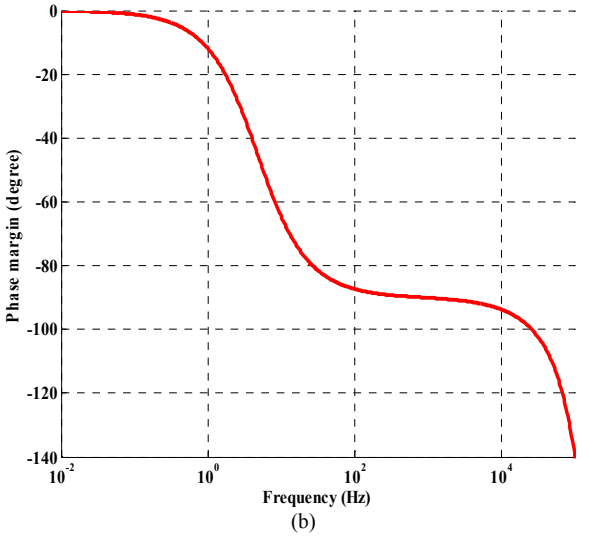
$$s_{p3,4} = -\frac{(g_{m4b} + g_{mb4b})C_1(C_2 + C_L) + g_{m11}C_2(C_1 + C_L)}{2C_L C_2 C_1} \pm j\sqrt{\frac{g_{m6}((g_{m4b} + g_{mb4b}) + g_{m11})}{C_B C_L}} \tag{19}$$

3. SIMULATION RESULTS

The proposed OTAs are simulated in HSPICE with BSIM3v3 model based on a standard 0.18 µm CMOS process. Figure 3 shows the simulated open loop gain. The simulation results shows a considerable increase in unity-gain bandwidth to the value of 81 KHz, the improved DC gain of 84.1 dB, and a phase margin of 55°. Figure 4 and 5 show slew rate and output swing, respectively. Simulation results shows the value of the slew rate is 44V/ms .The presented topology employing weak inversion transistors is capable of working at 500 mV of power supply and consuming only 900nW.



(a)



(b)

Fig. 3. Simulated open loop gain and phase margin

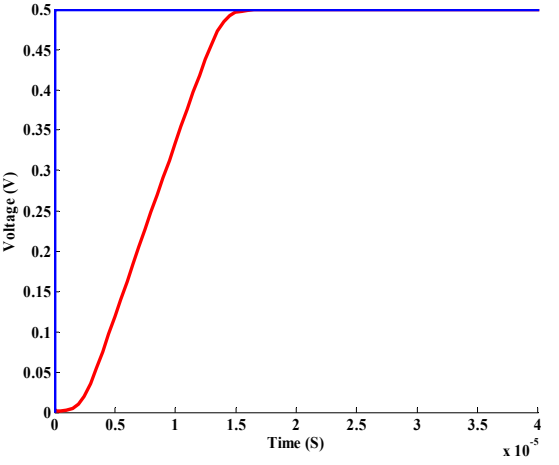


Fig. 4. Simulated slew rate

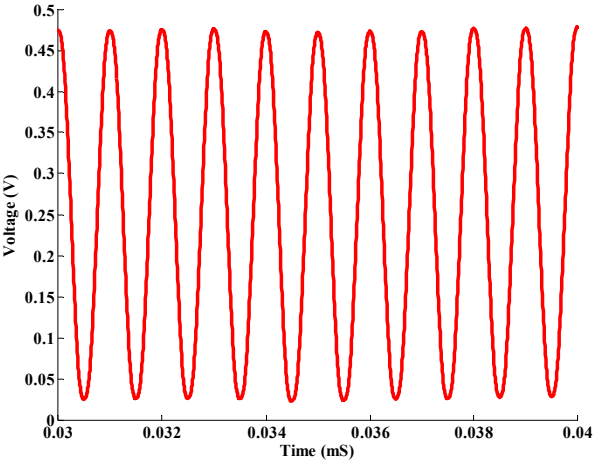


Fig. 5. Simulated output swing

The designed system demonstrates relatively suitable response in different process corners. Table 1 shows a comparison with other low-voltage and low-frequency operational amplifiers. To evaluate this work a figure of merit (FOM) can be defined as [1]:

$$\text{FoM}=\frac{(\text{Gain})(\text{Unity gain freq.})}{(\text{Power supply})(\text{Power consumption})}. \quad (20)$$

The proposed architecture shows a noticeable FOM even under the condition of ultra low supply voltage of 500 mV.

4. CONCULSION

A new ultra-low voltage ultra-low power operational transconductance amplifier design was described in this paper. The proposed OTA utilizes bulk driven technique. Simulation results have been presented to confirm the considerable improvement in unity-gain bandwidth and also the DC gain, when compared to other ultra-low power low frequency OTAs conventional RHP zero controlling techniques .The simulation results show that

the open loop gain of the presented amplifier is equal to 84.1dB while achieving unity gain bandwidth of 81 KHz. The total power consumption of the OTA is as low as 900nW and the supply voltage is as low as 0.5V which is much lower compared to the other presented works. This ultra-low power ultra-low voltage architecture is very useful in bio-medical applications in which the power budget is limited.

Table. 1: Comparison with other low-voltage and low-frequency operational amplifiers

	This work	[1]*	[5]	[6]	[7]	[10]
Tech(um)	0.18	0.18	0.35	0.18	0.35	0.35
Vdd(mV)	500	400	600	900	900	1400
P_{dc}(nW)	900	386	550	450	9900	840
Gain(dB)	84.1	78	73.5	70	62	95
PM(degree)	55	88	54	62	52	65
UGB(KHz)	81	16.6	13	5.6	540	14
CMRR(dB)	96	93	67.4	26	129	60
Slew Rate(V/ms)	44	20	14.7	N/A	N/A	3
FOM(dB.KHz/mV.uW)	15.14	8.38	2.9	0.96	3.76	1.13
M/S**	S	S	S	M	S	S

*Bulk driven results ,** Measurement/Simulation results

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