A Ultra Wideband (5–50 GHz) and Low Power Active Balun Using 0.18 µm CMOS technology

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ABSTRACT:
A new ultra wideband 5 to 50 GHz and low power single ended input, differential output active balun using 0.18µm CMOS technology is presented in this paper. Using a pair of common-source and common gate NMOS transistors with utilize active load PMOS transistors. Total power consumption of the proposed active balun circuit is 5mw at the supply voltages of ±1.2v much less than 11.5mw of the conventional active balun.

KEYWORDS: Balun, Differential Pair, Low Noise, UWB Active Balun, Low Power.

1. INTRODUCTION

A differential amplifier can be used in integrated circuits as an active balun circuit when single ended input to differential output is needed. For instance, the differential signals can enhance the fundamental rejection in the balanced frequency double, the port-to-port isolation in the mixer, and the bandwidth in the balanced amplifier.

Normally passive baluns are widely using of LC-CL network or transmission line transformers. Although they have low power consumption but using many Spiral Inductors and microstriplines in integrated circuits that lead to large physical size. Generally , the active balun is the better choice with less power consumption [1], [2].

Different types of configurations have been found in literatures for implementation of active balun circuits. The schematic of the conventional active balun without feedback compensation circuit is shown in Fig.1. Active baluns have lower losses than passive baluns.

The parasitic effects limit active balun circuits at the high-frequency and broadband applications. In this paper, a 5 to 50 GHz active balun in 0.18 CMOS process is demonstrated. The active balun using of differential amplifier for achieve in a broadband performance with the Feedback compensation technique. In order to is used of a capacitor feedback (C_{FB}) with value 2.5PF that decreases noise and S_{11} parameter improves and also can outputs balance.

The simulated results shows that the roposed active balun has a small signal gain between 0 to 1 dB from 5 to 50 GHz. The power consumption In conventional active baluns is about 12 mw.

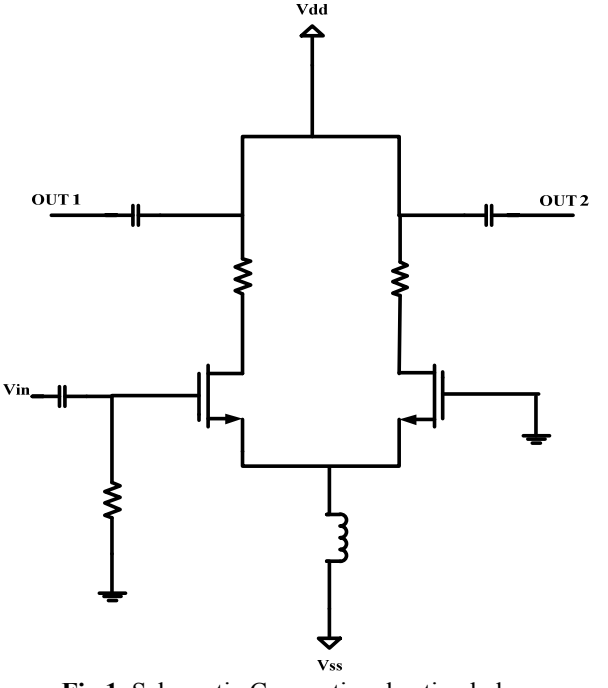

Fig.1. Schematic Conventional active balun

In this paper a new ultra wideband and low-power active balun is proposed that using of a configuration composite of a pair common-gate and common-source (CGCS) circuit. In Fig.2, an Capacitor feedback (C_{FB}) can used for compensate and remove mismatch

between differential pair and reduce noise figure [3], [4].
A common-source and common-gate FET pair active balun has broadband performance and low power Consumption [5].

2. BALUN DESIGN

Fig.1 shows the schematic of the conventional active balun circuit. conventional active balun consists of a common-gate and common-source circuit. We suppose the gate width and the electrical characteristic of the common-gate are the same as those of the common-source. Fig. 2 shows the schematic of the proposed active balun circuit. The active balun is simulated using TSMC 0.18 CMOS process. One input of the differential amplifier is single-ended, and the other is grounded through the inductor and capacitor.
For an ideal differential amplifier, the input impedance Z_S seen from the common node should be infinite. At high frequency, C_{ds} the parasitic capacitor acts as a low impedance so that Z_S has certain power consumption.
For increase impedance (Z_S) an inductor Ls is added. With this structure, the performance of the active balun improves. Inductor (L_g) and capacitor (C_g) in gate M_2 due to decrease noise figure and S_{11} parameter improve and balance two outputs.

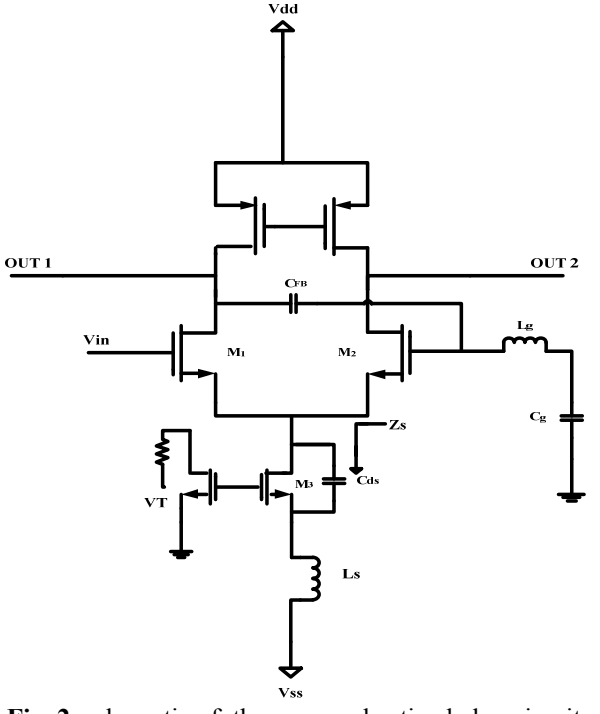

Fig. 2. schematic of the proposed active balun circuit

With decrease inductor in gate M_2 (L_g), S_{11} parameter improves and balanced two outputs, also with increase capacitor in gate M_2 decreased noise figure and S_{11} parameter improves and balanced two outputs. The values must carefully chosen for sustain proper biasing of the transistors in the saturation condition. Actually the biasing current must be small. at this design is used of supply voltages V_{dd}=1.2V and V_{SS}=-1.2V.
This proposed active balun achieved the highest operation frequency, the widest bandwidth and also suitable S_{11} parameter and noise figure better into the conventional active balun.

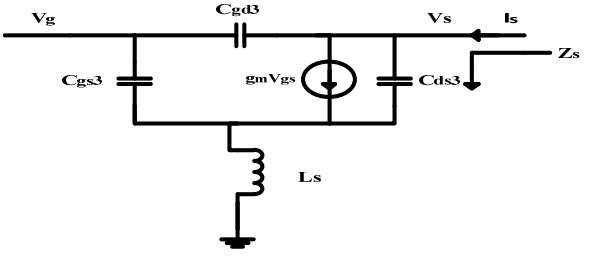

Fig. 3. Small-signal equivalent circuit model of the proposed active balun circuit for calculation Zs impedance

Z_S impedance following of this equation :

$$Z_s = \frac{1}{SC_{ds}}(1 + Sg_m L_s)$$

As shows L_S inductor proportionate is with Z_S impedance.

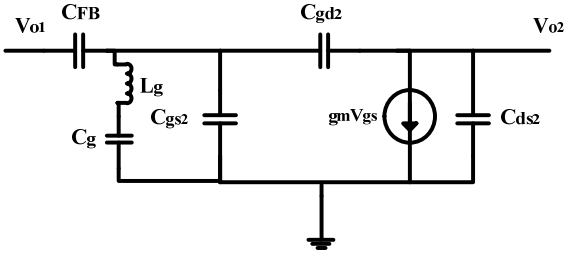

Fig. 4. Small-signal equivalent circuit model of the proposed balun circuit for calculation voltage ratio of the two outputs

if C_{FB} , $C_g \gg C_{gd}$, C_{gs} , C_{ds} voltage ratio of the two outputs is given by :

$$\frac{V_{o2}}{V_{o1}} = \frac{[S(1+S^2L_gC_g)] - \frac{(1+S^2L_gC_g)(SC_{gd}-g_m)}{SC_{gd}}}{(1+S^2L_gC_g)(\frac{SC_{gd}-g_m}{SC_{gd}})}$$

$$\frac{V_{o2}}{V_{o1}} = \frac{3(SC_{gd}) - (SC_{gd}-g_m)}{SC_{gd}-g_m}$$

A balanced output demands $vo_1 = -vo_2$. If biasing current is large, then $g_m >> mC_{gd}$ and the condition is fulfilled.

3. SIMULATION AND RESULTS

A balun circuit is designed in a standard 0.18 um CMOS technology. The load impedance at output ports is the same as the source of 50Ω. The performance of this proposed active balun is summarized in Table 1 and 2. This circuit operates with supply voltages ±1.2 V and reasonable balanced outputs. The power consumption of the proposed active balun circuit is under 5mw at the supply voltages of ±1.2v much less than 11.5 mw of the conventional active balun. Simulated parameters (S_{11}, phase difference, $|S21|, |S31|$, Gain difference, noise figure) of the proposed active balun respectively is shown in Fig. 5-9.

Table 1. Performance summaruy

	[1]		**[2]**		**This Work**	
Process	0.18µm CMOS		0.13µm CMOS		0.18µm CMOS	
Bandwidth[GHz]	8		2 - 40		5 - 50	
Noise Figure[dB]	<14		N/A		< 2	
	Max	Min	Max	Min	Max	Min
S11[dB]	N/A	N/A	0	-7.5	-10.03	-26.9
Gain[dB]	N/A	N/A	1	-1	≅1	0
Power Consumption[mw]	1.44*		40		5	
Source Impedance[Ω]	50		50		50	
Load Impedance[Ω]	50		50		50	
Voltage Supply[V]	1.2		2.8		±1.2	

Table 2. Forward gains of the proposed active balun

	10GHZ	25GHZ	50GHZ
$IS_{3,1}$[dB]-$S_{2,1}$[dB]I	4.8	0.2	0
∠$S_{2,1}$[deg]-$S_{3,1}$[deg]	180	177	174

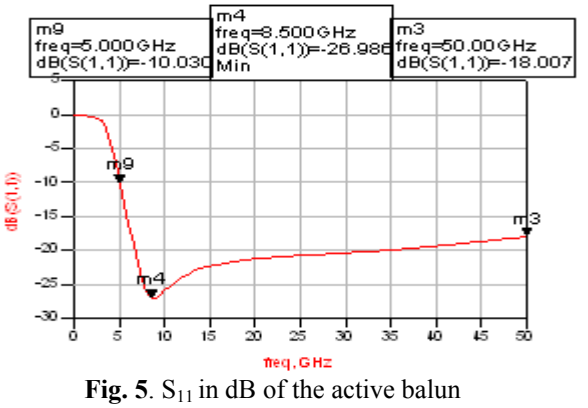

Fig. 5. S_{11} in dB of the active balun

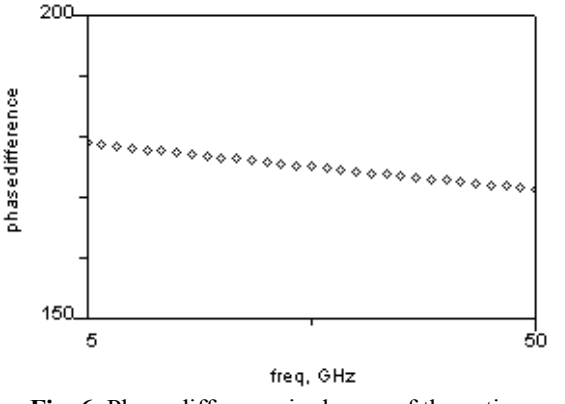

Fig. 6. Phase difference in degree of the active balun

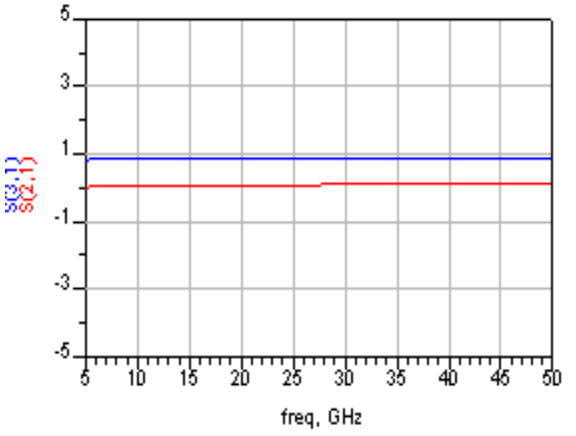

Fig. 7. |S21| and |S31| in dB of the active balun

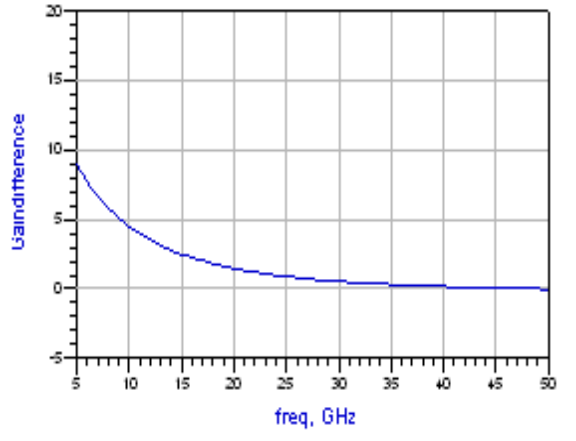

Fig. 8. Gain difference in degree of the active balun

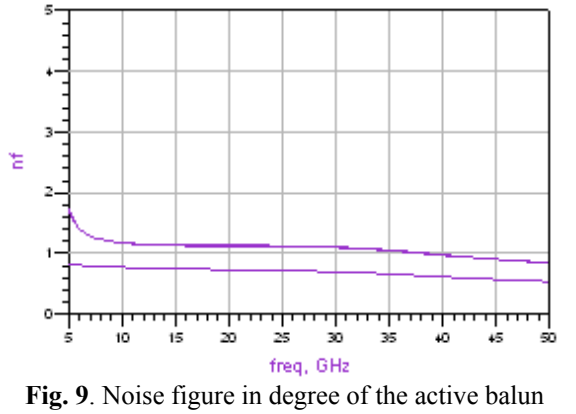

Fig. 9. Noise figure in degree of the active balun

4. CONCLUSION

A new ultra wideband 5 to 50 GHz and low power single ended input differential output Active balun using 0.18µm CMOS technology is presented in this paper. The proposed active balun is advantageous in low power and broadband performance. In this work the active balun using of differential amplifier for achieve in a broadband performance with the Feedback compensation technique. In order to is used of a capacitor feedback (CFB) with value 2.5PF that decreases noise figure and S11 parameter improves. power consumption of the proposed active balun circuit is under 5mw at the supply voltages of ±1.2v much less than 11.5mw of the conventional active balun. This proposed active balun achieved the highest operation frequency, the widest bandwidth and also suitable S11 parameter and noise figure better into the conventional active balun.

REFERENCES

[1] T.-T. Hsu and Ch.-N. Kuo, **"Low Power 8- GHz Ultra-Wideband Active Balun,"** IEEE SiRF, 2006.

[2] B.-J. Huang, B.-J. Huang, Student Member, IEEE, Kun-You Lin, Member, IEEE, and Huei Wang, Fellow, IEEE, **"A 2–40 GHz Active Balun Using 0.13 µm CMOS Process,"** *IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS,* Vol. 19, No. 3, MARCH 2009.

[3] H. Ma, S. J. Fang, F. Lin, and H. Nakamura, **"Novel Active Differential Phase Splitters in RFIC for Wireless Applications,"** *IEEE Trans. Microwave Theory Tech.,* Vol. 46, pp. 2597-2603, Dec. 1998.

[4] M. A. Do, W. M. Lim, J. G. Ma, and K. S. Yeo, **"Design of a Phase Splitter for 3rd ISM Band,"** *IEEE ISCAS, 2003.*

[5] M. Kawashima, Tadao Nakagawa, and Katsuhiko Araki, **"A Novel Broadband Active Balun,"** *33rd European Microwave Conference - Munich 2003.*

[6] D. Viveiros Júnior Marcos Aurélio Luqueze Denise Consonni, **"ACTIVE BALUNS IN MICROWAVE INTEGRATED CIRCUITTECHNOLOGY,"** *Journal of Microwaves and Optoelectronics,* Vol. 1, No. 1, May 1997.

[7] K. Jung, W. R. Eisenstadt, Senior Member, IEEE, Robert M. Fox, Senior Member, IEEE,Alvin W. Ogden, and Jangsup Yoon, **"Broadband Active Balun Using Combined Cascode -Cascade Configuration,"** *IEEE TRANSACTION ON MICROWAVE THEORY AND TECHNIQUES,* Vol. 56, No. 8, August 2008.

[8] H.-H. Chiang, Member, IEEE, Fu-Chien Huang, Student Member, IEEE, Chao-Shiun Wang, Member, IEEE, and Chorng-Kuang Wang, Fellow, IEEE, **"A 90 nm CMOS V-Band Low-Noise Active Balun With Broadband Phase-CorrectionTechnique,"** *IEEE JOURNAL OF SOLID-STATE CIRCUITS,* Vol. 46, No. 11, Nov. 2011.

[9] Ch.-H. Lai, and J.-R. Yang, **"A 3.1 - 10.6 GHz CMOS Low-Voltage Mixer with Active Balun Designed for UWB Systems,"** *2012 4th International Conference on Computer Research and Development IPCSIT*, Vol. 39, (2012) © (2012) IACSIT Press, Singapore.

[10] Y.-B. park, S.-H. Kim, H. Nah Joh, Y. Yun, K.-H. Park, and K.-H. Ahn, **"Miniaturized active balun MMIC employing active device,"** *The 23rd International Technical Conference on circuits/system, Computers and communications (ITC-CSCC 2008).*