RESEARCH ARTICLE

Performance Optimization and Sensitivity Analysis of Junctionless FinFET with Asymmetric Doping Profile

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ABSTRACT

In this paper, a novel junctionless fin field effect transistor (FinFET) with asymmetric doping profile along with the device from source to drain (ADJFinFET) is introduced and the electrical characteristics of the device are comprehensively assessed. Unlike the conventional junctionless FinFET, ADJFinFET has lower channel doping density with respect to the adjacent source and drain regions, which provides superior electrical performance in nanoscale regime. The impact of device geometry and physical design parameters on the device performance are thoroughly investigated via calculating standard deviation over mean value of main electrical measures. The sensitivity analysis reveals that metal gate workfunction, doping density and fin width are critical design parameters that may fundamentally modify the device performance. Furthermore, 2D variation matrix of gate workfunction and channel doping density is calculated for optimizing the device performance in terms of off-state and on-state current. The results demonstrate that the proposed device establishes a promising candidate to realize the requirements of low-power high-performance integrated circuits.

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INTRODUCTION

Generally, as the dimensions of conventional metal-oxide-field effect transistor (MOSFET) are scaling down, challenges better known as short channel effects have emerged, which eventually degrade the device performance in nanoscale regime [1-2]. It is to be noted that the punch through phenomenon is one of the critical problems of nanoscale MOSFET in which the extended drain side depletion region touches the depletion region of the source side, making the carriers tunnel through the entirely depleted channel, irrespective of the gate bias. Junctionless MOSFET employs a similar doping profile for the source, drain and channel regions which inherently provides simple and low power fabrication steps [3-8]. In addition, the usage of the same dopants along the device obviates the formation of source/drain-channel depletion regions, which fundamentally enables suppressed short channel effects arising from punch through event. Basically, similar to regular MOSFET, the gate electrode in junctionless MOSFET is responsible for modulating the carrier density in the channel. In the off-state, the workfunction difference between the gate material and the underlying channel depletes the carriers towards the source and drain regions, which ultimately blocks the current transport. However, in the on-state, increasing the gate bias reduces the depletion region width, allowing the carriers to flow towards the drain region. Despite the superior performance of junctionless MOSFET, there exists a trade-off between low off-state current, high on-state current and the lowest possible absolute value of threshold voltage. In [9], dual material gate structures are introduced for introducing an additional barrier in the channel. The proper combination of gate material and optimized length of channel for different gate workfunction are critical for improving the device performance. Graded channel doping is another technique that

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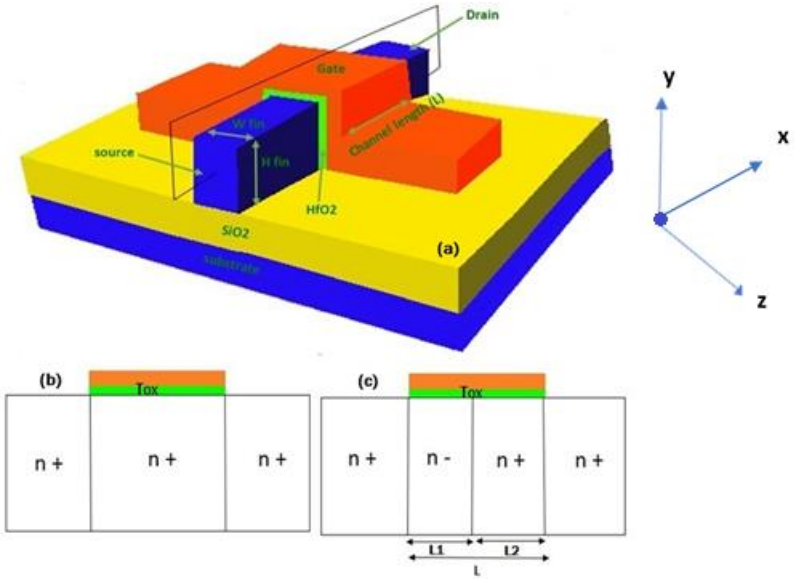

Fig.1. (a) 3D-Schematic of junctionless FinFET, (b) 2D cross section of the (b) conventional junctionless FinFET and (c) junctionless FinFET with asymmetric doping profile.

is introduced for reducing the off-state current. However, this method requires complex fabrication process [10-11]. The employment of multi-gate MOSFET with planar structure such as FinFETs introduces another technique for reducing short channel effects. This structure with top and sidewall gates provides extremely improved electrostatic gate control over the conducting channel and presents a reliable scaling track for low power digital applications [12-15].

The main goal of this paper is to combine the benefits of junctionless MOSFET and conventional FinFET for the introduction of junctionless FinFET structure with optimized performance. However, unlike the conventional junctionless structure, the doping density of the channel region is different from the ones in the source and drain regions, presenting the device naming as asymmetric doping junctionless FinFET (ADJFinFET) structure. The electrical performance and impact of critical physical and geometrical design parameters on the electrical characteristics of the device are comprehensively investigated. Furthermore, statistical data analysis is performed by calculating standard deviation over mean value of main electrical parameters in percentile including on-state current (I_{on}), off-state current (I_{off}), on/off current ratio, threshold voltage (V_{th}) and subthreshold swing (SS). The statistical analysis measures the variability of each data point among various sets of data. The paper is organized as follows: in section two, schematic of the devices as well as fundamental simulation models are introduced. Following that, in section three, electrical performance of the junctionless FinFET with asymmetric doping profile is comprehensively assessed. Furthermore, sensitivity analysis of the proposed device is discussed in this section. Finally, the paper is summarized in section four.

Device structure and simulation models

The schematic view of the proposed structure, a 3D asymmetric doping junctionless FinFET, is depicted in Fig.1(a) and the 2D cross section of the conventional junctionless FinFET and ADJFinFET are presented in Fig.1(b) and Fig.1(c), respectively. Basically, for the n-channel operation of the device, source, drain and channel regions are heavily doped with donor atoms, forming a junctionless transistor topology. In conventional junctionless FinFET, similar doping densities are considered for the whole region. However, in the proposed asymmetric doping junctionless FinFET, a non-uniform doping profile is designed along the device and the channel doping density is different from the source and drain regions. The primary design parameters are introduced in Table.1. Numerical simulations are performed by 3D ATLAS device simulator [16] and following models are implemented for calculating the drain current:

Table 1. Initial design parameters of conventional junctionless FinFET and ADJFinFET.

Design Parameter	Conventional junctionless FinFET	ADJFinFET
Gate Workfunction	4.9eV	4.9eV
Channel length-L	14nm	14nm
Source/Drain doping density	$2.5\times10^{19}cm^{-3}$	$2.5\times10^{19}cm^{-3}$
Channel doping density	$2.5\times10^{19}cm^{-3}$	varies from $1\times10^{18}cm^{-3}$-$2.5\times10^{19}cm^{-3}$
Gate oxide thickness-T_{ox}	2nm	2nm
Gate oxide permittivity	HfO_2-25	HfO_2-25
Fin height-HFin	20nm	20nm
Fin width-WFin	8nm	8nm

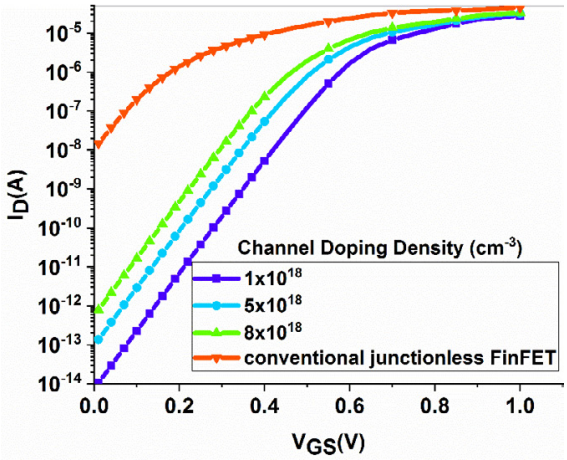

Fig.2. Transfer characteristics of conventional and ADJFinFET (L1=14nm, L2=0nm) as the channel doping density is parametrized.

• Drift-Diffusion models are activated for calculating the carrier transport equations.

• Band gap narrowing model is activated for considering the shrinkage of bandgap energy in the highly doped regions. Basically, donor impurities in the heavily doped regions rearrange the position of the valence band and conduction band, reducing the band gap energy.

• Essentially, as the doping density is increased, the carrier mobility is considerably deteriorated due to the scattering of carriers by the ionized impurity atoms. In addition, carriers are accelerated by the gate and drain vertical and horizontal electric fields but may miss the momentum due to different scattering mechanisms. Accordingly, proper mobility models are activated, considering all the scattering mechanism, for calculating the drain current.

• Density gradient quantum model is activated for considering the effect of quantum confinement on the carrier density, mainly in ultra-thin body devices with narrow fins.

• Auger and Trap-assisted generation-recombination models are activated for calculating the drain current in the vicinity of defects and traps.

It is worth to be mentioned that the design parameters are obtained from [17], in which lateral source and drain spacers are introduced for reducing short channel effects. However, one of the main drawbacks of the proposed device in [17] is the device scalability. The fabrication process of ADJFinFET first involves growing an oxide layer over the substrate. Next, silicon layer is grown over the oxide on which fins are etched out. Following that, ion implantation is employed for creating heavily doped source and drain regions. It is worth to be mentioned that required masks should be designed for the doping process. In the next step, the channel region with lower dopant density is created via ion implantation technique. Following that, an oxide layer is deposited on top of the fin as well as on the sidewalls of the fin. Finally, gate material is deposited over the gate insulator layer on all three sides.

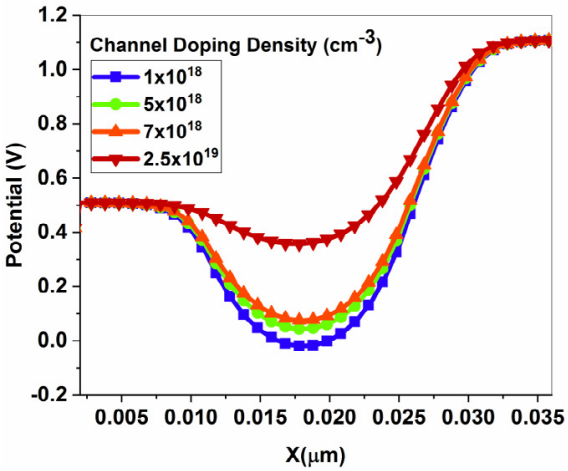

Fig.3. Electrostatic potential distribution of ADJFinFET in the off-state along the channel from source to drain for different channel doping density.

RESULTS AND DISCUSSIONS

By definition, in conventional junctionless FinFET, there exists no doping density gradient along the device for the source, channel and drain regions. In the absence of gate voltage, the metal gate-channel workfunction difference is exploited to discharge the channel from carriers to make the device off. Basically, depletion of carriers from the channel results in the distribution of space charge region through the channel, blocking the current transport towards the drain. However, as the positive gate voltage exceeds beyond the threshold voltage, electrons are accumulated in the channel and the current flow towards the drain. The operation of ADJFinFET is similar to that in the conventional junctionless FinFET. However, due to the lower doping density in the channel in comparison with the source and drain regions, a potential barrier is created at the source-channel interface which can reduce the off-state current. The transfer characteristics of conventional junctionless FinFET and ADJFinFET are illustrated in Fig.2 as the channel doping density is parametrized. Initially, the whole length of the channel has lower doping density in comparison with the source and drain regions (L1=14nm, L2=0nm). Evidently, the space charge region with ionized donor atoms becomes thicker as the electron density is reduced. This phenomenon can considerably decrease the off-state leakage current and can improve the on/off current ratio. The potential distribution of the ADJFinFET is illustrated in Fig.3 as a function of channel doping density, for V_{GS}=0V, V_{DS}=0.6V. The use of asymmetric doping profile in the channel region increases the minimum potential point at the source-channel nearby, which results in an improved gate control over the channel. In addition, modulation of space charge region by the channel doping density is a fundamental effect that is associated with the off-state drain current.

However, it is important to point out that doping density, gate workfunction value and surface potential can effectively modify the threshold voltage of the device. In this research, the threshold voltage is defined as the specific gate voltage value at which the drain current reaches 10^{-7} (A). Fig. 4 represents threshold voltage of ADJFinFET as a function of channel doping density. In principle, a tunable threshold voltage is demonstrated and the results are justified for different gate workfunction values. The results reveal that the threshold voltage is, in fact, highly sensitive to the doping variation for gate workfunction values below 4.8eV. Basically, metal gate work function and channel doping density of junctionless MOSFET should be precisely integrated to achieve optimum threshold voltage. The threshold voltage shift is mostly attributed to the channel dopant fluctuation, since the active channel region is not totally depleted for low gate work function values. It has been found that as the gate workfunction exceeds beyond 4.8eV, due to the dominant role of gate workfunction for the channel charge modulation, the threshold voltage variation is less susceptible to the channel doping density.

Basically, the height and width of the fins are

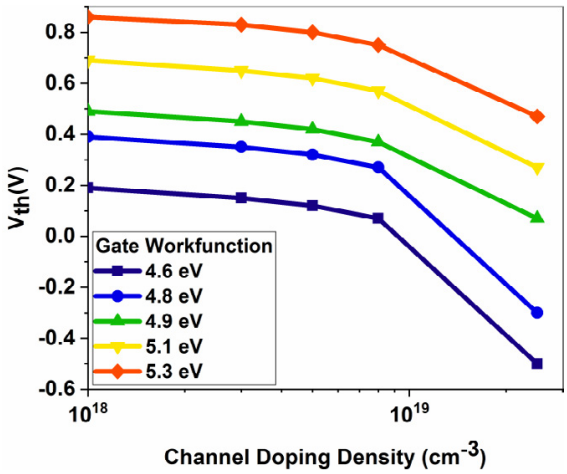

Fig. 4. Threshold voltage of ADJFinFET versus channel doping density for different metal gate workfunction values.

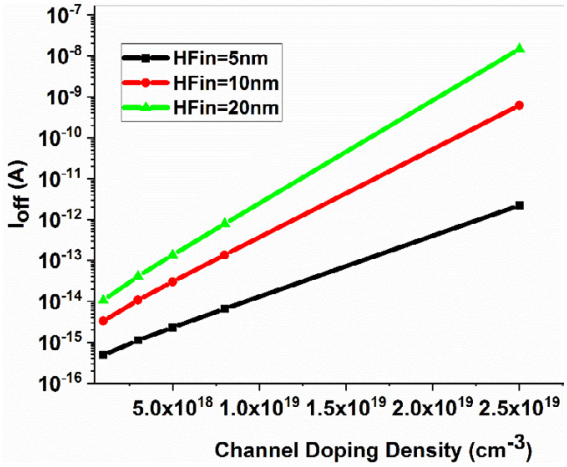

Fig. 5. off-state current versus channel doping density as the fin height is varied.

critical design parameters that may fundamentally affect the electrostatic gate coupling over the channel region. A detailed analysis is conducted for assessing the effect of asymmetric channel doping profile on the off-state current, while the fin height is parametrized, illustrated in Fig. 5. In principle, the channel doping density and geometry of the device can directly bring about off-state current variation. The results demonstrate that the off-state current is considerably reduced as the channel doping density is decreased. A detailed analysis of fin height variation manifests that for HFin=20nm, with lower level of gate controllability over the channel, the off-state current ratio of structure with symmetric doping profile over the related value of ADJFinFET with donor atom density of 1×10^{18} (cm^{-3}) is 1.41×10^{6}. However, in the similar case, reduction of the fin height to HFin=5nm shows the off-state current ratio of 4.6×10^{3}. This shows that gate coupling and channel doping are two main factors with competitive advantages for off-state current reduction. It is to be noted that weaker gate control over the channel in the structure with elevated fins leads to the dominant role of channel doping for variation of the off-state current. On the other side, the ADJFinFET structure with ultrathin fin height enables stronger gate coupling over the channel with suppressed short channel effects that diminishes the role of channel doping.

The width of the fin can significantly influence the device's performance and efficiency. Fig. 6 illustrates how different fin width affects the transfer

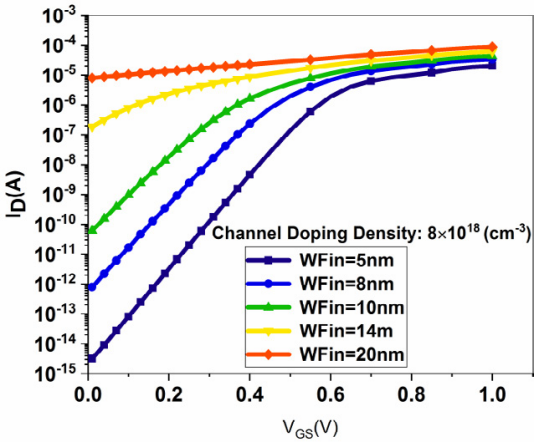

Fig. 6. Transfer characteristics of ADJFinFET as a function of fin width.

Table 2. Main Electrical parameters of ADJFinFET as a function of fin width for channel doping of 8×10^{18} (cm^{-3}).

WFin(nm)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	V_{th} (V)	SS(mV/Dec)
5	2.00E-05	3.17E-15	6.32E+09	0.5	67
8	3.35E-05	7.90E-13	4.24E+07	0.37	75
10	4.28E-05	6.13E-11	6.98E+05	0.27	92
14	6.11E-05	1.84E-07	3.32E+02	0.01	25
20	8.77E-05	7.89E-06	1.11E+01	0	92

characteristics of the ADJFinFET. The fin width can effectively modulate the carrier distribution in the channel and as a consequence, making the off-state current decrease as the fin width becomes narrower. It is to be noted that due to the robust gate coupling over the channel, a larger immunity of short channel effect for the thinner fin width can be expected. However, despite the asymmetric doping profile, the device performance is gradually degraded with high off-state current and poor switching speed for fin width above WFin=10nm. This effect is mainly justified as a consequence of reduced depletion region area in the channel, arising from the degradation of gate control over the channel. The overall main electrical parameters of ADJFinFET are summarized in Table 2. while the fin width is parametrized. Generally, high on/off current ratio with low subthreshold swing is mainly attributed to the dominant gate control in ultra-thin fins as well as asymmetric doping profile in the channel.

Fig. 7 illustrates the off-state current of ADJFinFET versus channel doping for different fin width values. It is observed that for WFin=5nm, the off-state current ratio of symmetric structure over the respected value of ADJFinFET structure with channel doping of 1×10^{18} cm^{-3} is 1.19×10^{3}. Moreover, this value is 9.48×10^{6} for WFin=10nm and 3.5×10^{2} for WFin=20nm, respectively. This is because for ultra-thin fins, the electrostatic gate coupling over the channel region is high enough for modulating the charge density in the channel, which may eventually diminish the role of asymmetric channel doping density. However, for WFin=10nm, since the gate controllability over the channel has not been completely degraded, the reduced channel doping effectively assists the modulation of off-state current modulation. However, for the case of WFin=20nm, as the depletion region in the channel area of ADJFinFET is mainly governed by the channel thickness, increasing the fin width diminishes the role of channel doping density. It can be concluded that as the fin width increases, proper combination of gate workfunction value and lower channel doping density are required to optimize the device performance.

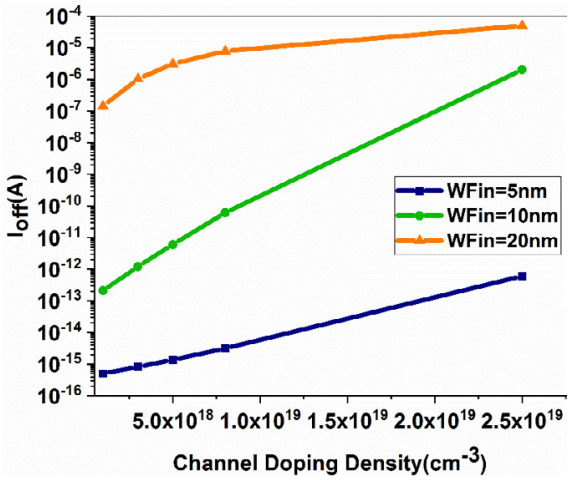

Fig. 7. Off-state current versus channel doping density as the fin width is parametrized.

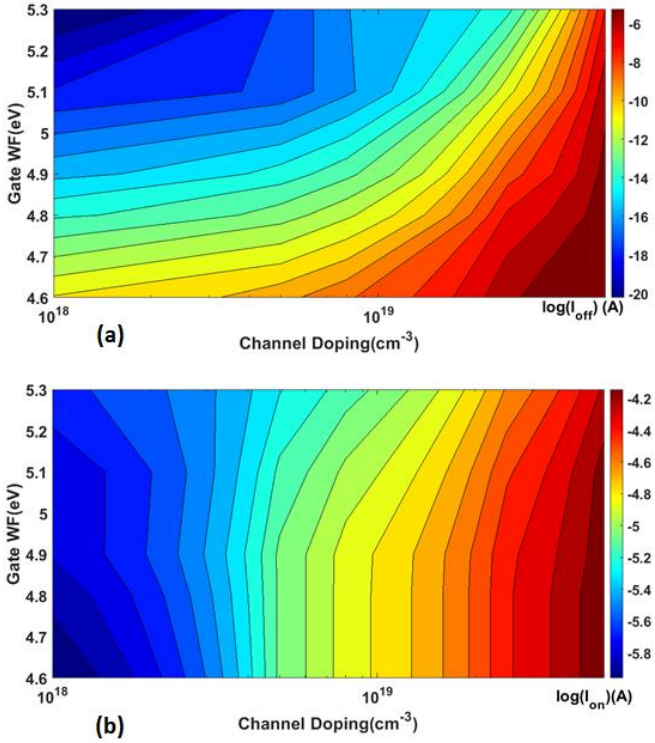

Fig. 8. 2D variation matrix of (a) off-state and (b) on-state current as a function of gate workfunction and channel doping density.

The 2D variation matrix of off-state and on-state current of ADJFinFET is calculated as a function of gate workfunction and channel doping density, illustrated in Fig.8(a) and Fig.8(b), respectively. The off-state current is significantly increased in the bottom-right corner of the contour in the case of the heavily doped channel region as well as reduced value of gate workfunction. It is important to point out that the presence of high volume of donor atoms in the channel helps to reduce the depletion layer width in the channel, leading to an increase in the leakage current. However, minimum off-state current can be achieved by higher metal gate workfunction values in low doped channel, which occurs in the top-left corner of the matrix. The variation matrix of on-state current is illustrated

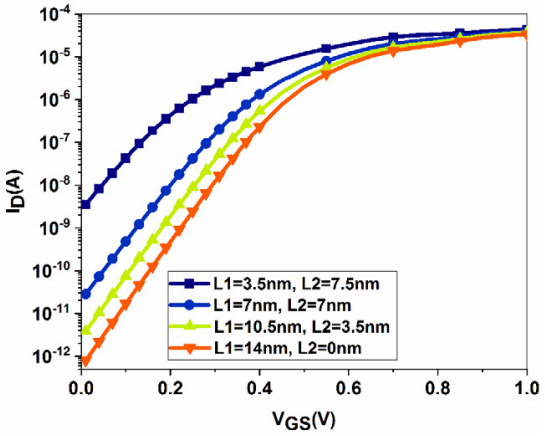

Fig. 9. I_D-V_{GS} curves of ADJFinFET as a function of length of the channel with asymmetric doping profile.

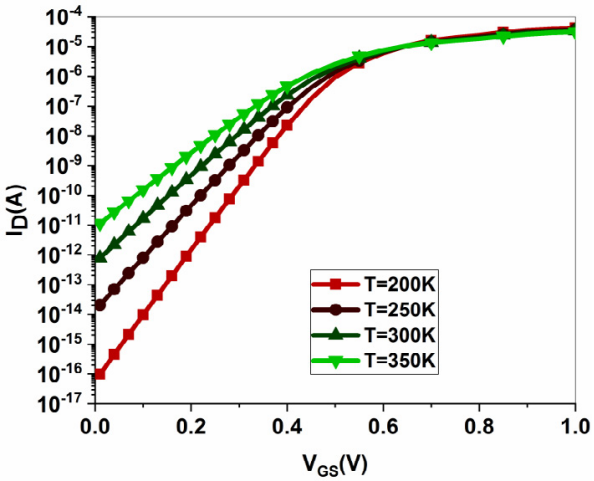

Fig.10. Transfer characteristics of ADJFinFET as the temperature is parametrized.

in Fig.8 (b). Clearly, for a constant doping density, the drain current is less sensitive to the variation of gate workfunction which implies the dominant role of gate bias for modulating the space charge region in the on-state. Despite this, the incapability to overcome the trade-off between high on-state current, low off-state current as well as lowest possible positive threshold voltage still exists and does not yet have reached a clear and fundamental solution. It is to be noted that the need for the efficient performance of the device signifies an appropriate choice of doping density and metal gate workfunction. Next, the transfer characteristics of the ADJFinFET as a function of length of the channel with asymmetric doping profile (L1) is illustrated in Fig.9. The results demonstrate that the off-state current is gradually decreased as the whole length of the channel has lower doping in comparison with the source and drain regions.

Fig.10 illustrates the impact of temperature (T) on the performance of ADJFinFET. The results demonstrate that temperature has a considerable effect on the enhancement of the off-state current and subthreshold swing. This effect originates from the diffusion section transport mechanism of ADJFinFET.

Following that, impact of geometrical and physical design parameters on the performance of the device is thoroughly assessed. Fig. 11 demonstrates a sensitivity bar chart of electrical parameters as a function of design parameters. Basically, standard deviation over mean value is a statistical measure that determines the deviation and scattering of the dataset with respect to

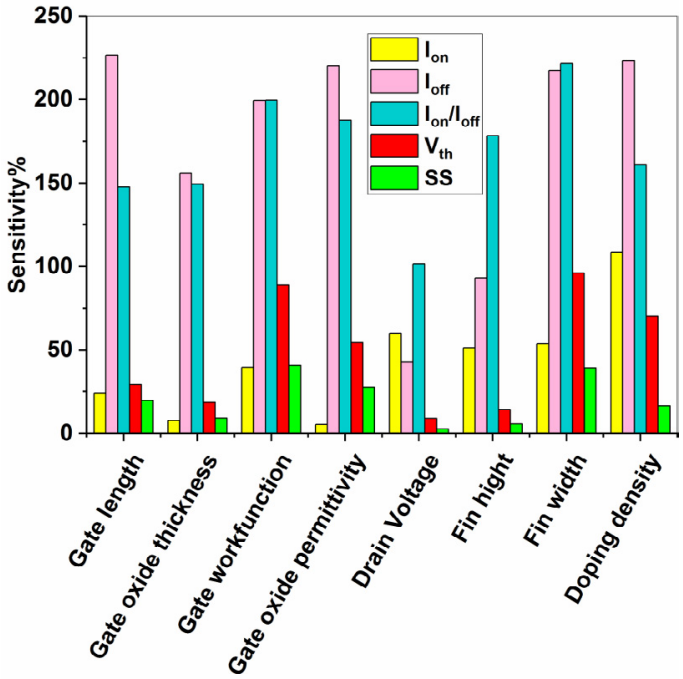

Fig. 11. Sensitivity bar chart of main electrical measures with respect to the variation of critical design parameters.

the mean value. Sensitivity of main electrical parameters are defined as follows:

$$Sensitivity\ \% = \frac{\sigma}{\overline{x}} \times 100 \quad (1)$$

In which σ denotes the standard deviation and $\overline{x}$ presents the average value of x as the specific electrical parameter. The highest value of sensitivity signifies the susceptibility of the specific electrical measure with respect to the related design parameter. The results demonstrate that the on-state current is highly correlated with the doping density, which implicates the precise tuning of the channel carrier accumulation. Next, in terms of off-state current, metal gate workfunction, fin width and gate oxide permittivity are critical issues that may fundamentally affect the device performance. Metal gate workfunction can crucially modulate the electron density and depletion width in the channel that as a consequence, enhances the sensitivity of the off-state current to the specific material of the gate. Furthermore, fin width and gate oxide permittivity can strongly modulate the gate coupling over the carriers in the channel. Clearly, suppression of off-state current arises from robust gate control over the depletion layer width in the conducting channel. One of the main features of ADJFinFET is the low susceptibility of threshold voltage and subthreshold swing to the variation of drain voltage and gate length, providing the possibility of potential application of the device in nanoscale regime.

SUMMARY

In this paper, the electrical characteristics of ADJFinFET are comprehensively investigated. The asymmetric doing profile of the channel region with respect to the adjacent source and drain regions establishes a feasible approach for extending the electrostatic gate potential via the sidewall gate electrodes. The computed 2D variation matrix demonstrates that the off-state current of the proposed device is modulated by optimizing the gate workfunction and the channel doping density. In addition, it is critical to be mentioned that fin width and fin height can fundamentally affect the proper channel doping concentration. Sensitivity analysis of the device reveals that the gate material, fin width, channel doping density and gate oxide capacitance are important design parameters that may affect the efficiency of the device. In principle, the results in this paper put forward a comprehensive analysis on the design and simulation of a nanoscale junctionless FinFET

with optimized electrical characteristics.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interest regarding the publication of this manuscript.

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