J. Nanoanalysis., 6(3): 193-198, Summer 2019

ORIGINAL RESEARCH PAPER

High-Speed Ternary Half adder based on GNRFET

Mahdieh Nayeri [1], Peiman Keshavarzian [1,*], Maryam Nayeri

[1] Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran
[2] Department of Electrical Engineering, Yazd Branch, Islamic Azad University, Yazd, Iran

Received: 2019-04-10 Accepted: 2019-05-22 Published: 2019-06-20

ABSTRACT

Superior electronic properties of graphene make it a substitute candidate for beyond-CMOS nanoelectronics in electronic devices such as the field-effect transistors (FETs), tunnel barriers, and quantum dots. The armchair-edge graphene nanoribbons (AGNRs), which have semiconductor behavior, are used to design the digital circuits. This paper presents a new design of ternary half adder based on graphene nanoribbon FETs (GNRFETs). Due to reducing chip the area and integrated circuit (IC) interconnects, ternary value logic is a good alternative to binary logic. Extensive simulations have been performed in Hspice with 15-nm GNRFET technology to investigate the power consumption and delay. Results show that the proposed design is very high-speed in comparison with carbon nanotube FETs (CNTFETs). The proposed ternary half adder based on GNRFET at 0.9V exhibiting a low power-delay-product (PDP) of ~10^{-20} J, which is a high improvement in comparison with the ternary circuits based on CNTFET, lately proposed in the literature. This proposed ternary half adder can be advantageous in complex arithmetic circuits.

Keywords: *Armchair- Edge Graphene Nanoribbon; High-Speed; Power Consumption; Ternary Half Adder*

How to cite this article
*Nayeri M, Keshavarzian P, Nayeri M. High-Speed Ternary Half adder based on GNRFET. J. Nanoanalysis., 2019; 6(3): 193-198. DOI: 10.22034/jna.****

INTRODUCTION

One of the most important blocks of the arithmetic circuit is adder circuit. Adder applies in the arithmetic logic unit (ALU), addition, multiplication, division, exponentiation, etc. [1-2]. The performance of these circuits is related to the number of transistors, delay, chip area, power consumption, and full swing output that called the figure of merits (FOM) parameter. Some circuit designs have been performed based on MOSFET [3-4]. Due to the short channel effects, increasing the gate leakage current and other challenges of MOSFET, new technologies have been replaced. These technologies are quantum computing, quantum-dot cellular automata (QCA), Spintronic-logic devices, carbon nanotube field effect transistor, single electron devices, [5], and graphene nanoribbon field effect transistors. GNRFET has excellent electronic properties that can be the best candidate for replacing MOSFET. Graphene is a monolayer of carbon atoms packed into a 2-D honeycomb lattice. The potential to produce wafer-scale graphene promises the high integration capability with conventional CMOS fabrication processes, which is a significant advantage over carbon nanotubes [6]. Unlike the CNT, the planar structure of graphene is compatible with the current CMOS technology, and it can be patterned both as a channel and interconnect in all-graphene circuits. The band gap of graphene can be opened with a nanoribbon shape. Graphene nanoribbon can open the band gap up to 400 mev [7]. The measurement of the graphene nanoribbon threshold voltage (Vth) is related to the band gap, which is dependent on the width. The quantum confinement effects in the graphene can be led to

* Corresponding Author Email: *Keshavarzian@iauk.ac.ir*

the potential for multiple transistor threshold voltages and new circuit configurations.

Interconnection occupies approximately 70 percent of the area in the digital circuit, which has led to many limitations of manufacturing and applying in binary circuit implementation. Multiple-valued logic (MVL) is the best approaches to enhance the capability of value and data transferring in binary circuits. The MVL circuit has a high circuit density and can perform complex operations with fewer interconnection problems [8]. For boosting the performance of CMOS technologies, MVL circuits have been inserted into binary logic ICs [9]. Many real applications, like process control and robotics, can be implemented more efficiently by using MVL systems [10].

Researchers describe two types of multiple-valued logic circuits, including voltage-mode and current-mode [11-12]. Design of voltage-mode MVL circuits has been performed based on multi-threshold CMOS design. In this paper, we suggest the voltage-mode circuit. Ternary logic has been interested because of its advantage over binary logic for the design of digital circuits. These logic levels include 0, 1/2 V_{DD}, and V_{DD} voltage levels [13]. The number of bits to process the information is decreased by using the ternary logic. For instance, to process the number 21, one uses five digits (10101) in binary, whereas three digits (210) are required in ternary logic [14]. The ternary adders require log_3^2 times less computation than binary adders, and when the number of digits increases, the less delay over the complementary adders becomes more remarkable. In the previous works, there are many techniques which are illustrated for designing MVL circuits, based on CNTFET [8-10]. A proposed ternary half adder based on GNRFET is presented in this work. Organization of this paper as follows: Section 2 describes a review of GNRFET. Two proposed of the ternary adder are scrutinized in section 3. The Next section discusses the simulation result and compares the proposed structures with the previous circuit. Finally, in Section 5, conclusions are given.

GRAPHENE NANORIBBON FET

The graphene is a single atomic plane of graphite which is known as a two-dimensional material [15]. It can be possible to make the devices with the ultra-thin channels and higher speeds without facing the adverse short channel effects which limit the performance of them. The devices with graphene channels cannot be switched off due to zero bandgap. Several approaches [7, 16] have been offered for opening the band gap as shaping large-area graphene into nanoribbon or applying electric field into bilayer graphene or applying strain to graphene. The graphene nanoribbon shows enough band gaps to perform as a channel for electronic devices.

The graphene nanoribbon is categorized into zigzag-edge (ZGNR) and armchair-edge (AGNR). The structure of AGNR is similar to the zigzag carbon nanotube. Due to electronic properties of AGNRs are known as the semiconductor, whereas ZGNRs depict magnetic and metallic behavior. Hence, AGNR has used in digital circuits [17].

The graphene nanoribbon is a suitable material for designing circuit, especially MVL design. The threshold voltage of GNRFET is appropriate with bandgap and inversely related to the width of GNRFET. The width of a GNR (W_{ch}) is obtained as follows [18]:

$$W_{ch} = (N-1)\sqrt{3}\frac{dcc}{2} \quad (1)$$

Where N means the number of dimer lines. The carbon-carbon bond length is dcc= 0.144. N is the number of dimer lines in the armchair orientation. The electronic properties of armchair nanoribbon vary depending on the number of atoms in edge. AGNR of type N = 3K+1 and N=3K are semiconductors, whereas AGNR of type N=3K+2 is metallic where K is a positive integer [19]. AGNRFET is realized by connecting both sides of the channel to metals which are known as Schottky contact and is called Schottky barrier GNRFET (SB-GNRFET). Moreover, ohmic contacts can be obtained by applying doped GNRs as a source and drain regions.

Fig. 1 demonstrates the structure of MOSFET-type GNRFET with a six-ribbon. MOSFET-type

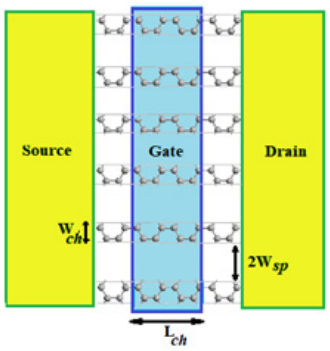


Fig. 1. The structure of a six-ribbon GNRFET.

Table 1. Logic symbols

Logic value	Voltage value
0	0
1	1/2 V_{DD}
2	V_{DD}

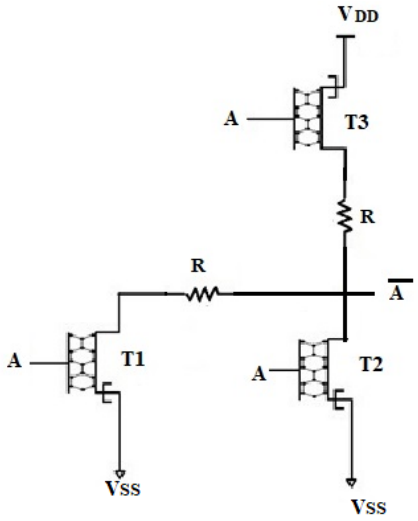


Fig. 2. Proposed ternary inverter circuit based on GNRFET.

GNRFETs enhance on/off current compared with SB-type one for the digital circuit applications [18]. So, we examine MOSFET-type GNRFET.

PROPOSED DESIGN

The First Design

The ternary logic includes ternary significant logic levels. These logic levels can be considered as 0, 1, and 2 symbols which are the counterpart to 0, 1/2 V_{DD}, V_{DD} voltage levels. Table 1 illustrates the ternary values [20]. The proposed ternary inverter circuit based on GNRFETs shows in Fig. 2.

If the A is 0V, all n-type GNRFETs are off, and only p-type GNRFET is on. Therefore, the output is V_{DD}. By increasing the input value to 1/2 V_{DD}, T2 and T3 are on. So, the output is 1/2 V_{DD}. Finally, if the voltage of A becomes V_{DD}, T1 is on, and the output will be 0V.

Table 2. Truth table of the ternary half adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

The adder circuit is a combinational digital circuit that is used for adding two ternary inputs and indicates ternary sum and carry in output. Table 2 demonstrates the truth table for the ternary half adder.

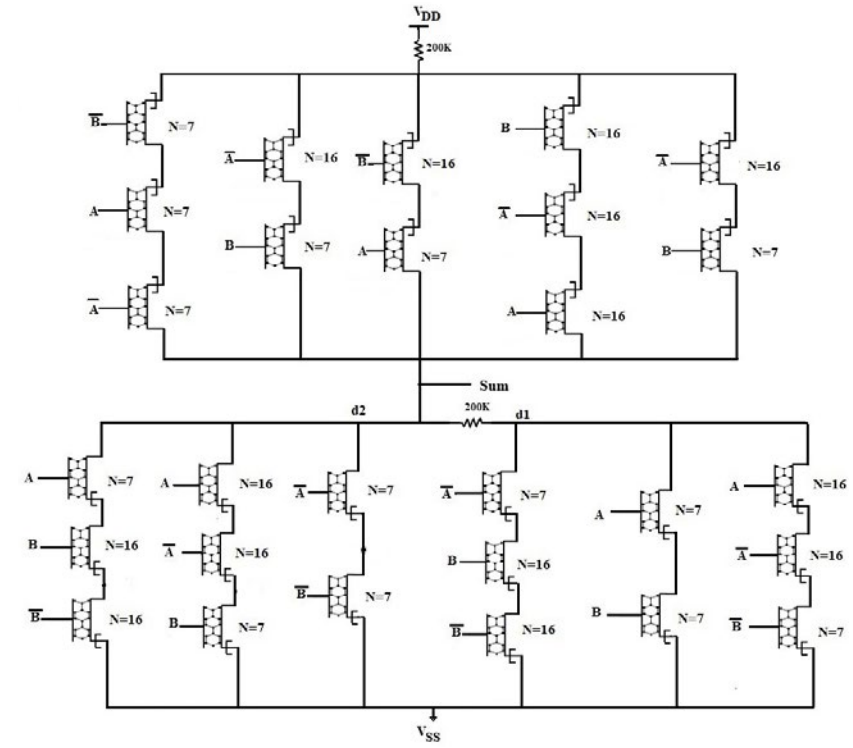
The parameters of the GNRFET model [21], their descriptions, and values are given in Table 3.

For the first time, half adder ternary is proposed based on GNRFET with low-power consumption, high–speed, and full swing output, as shown in Fig 3. This circuit consists of GNR transistors to provide sum and carry. Two resistors are applied to voltage division accurately. The power supply voltage is 0.9V. Three suitable paths cause to run all states containing V_{DD} to d2, d2 to GND, and d2 to GND. The logic value of the path from V_{DD} to d2 is 2, from d2 to GND is 0, and from d1 to GND is 1. In this proposed design, GNRFETs with two different widths are utilized to detect ternary logic. The dimer lines of transistors are 7 and 16.

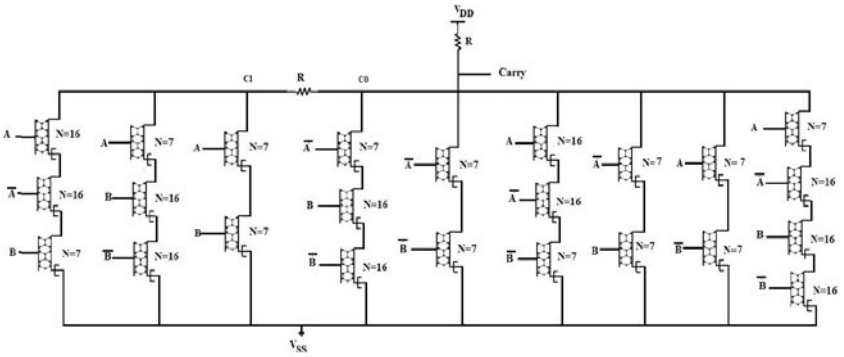
The P-GNRFET and N-GNRFET network can attain all states for various A and B inputs. Therefore, some transistors determine the eligible output logic. As seen in Fig. 3 (a), when the input value is 0V, all n-type GNRFETs are off and only p-type GNRFETs are on. Therefore, the output is V_{DD}. By increasing one of the input values to 1/2 V_{DD}, the voltage of the d1 node become 0 voltage and the output is 1/2 V_{DD}. Finally, if one of the input values is V_{DD}, the voltage of the d2 node becomes 0. So, the output is 0V. Fig. 3 (b) indicates the circuit

Table 3. The parameters of the GNRFET

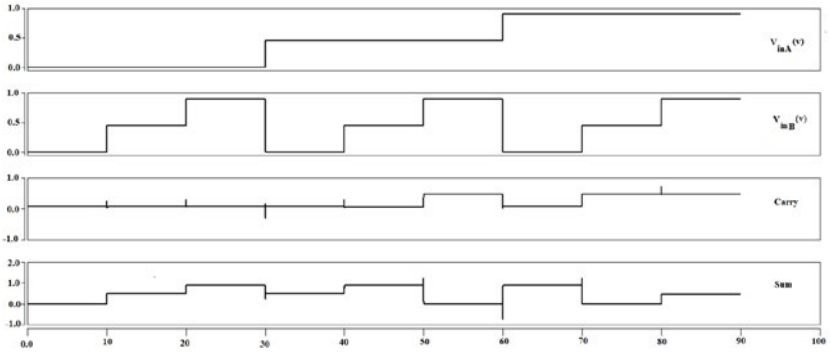
Device parameter	Description	Default value
L	Physical channel length	15nm
Tox	The thickness of the top gate dielectric material (planer gate)	0.95nm
2Wsp	The spacing between the edges of two adjacent GNRs within the same device	2 nm
NRib	The number of GNRs in the device	6
P	The edge roughness percentage of the device	0
Dop	Source and drain reservoirs doping fraction	0.001
Tox2	Oxide thickness between channel and substrate/bottom gate	20nm
Gates_tied	Whether gate or sub hold the same voltage	0



a)



b)



c)

Fig. 3. The first proposed design a) sum b) carry c) transient response of ternary half adder

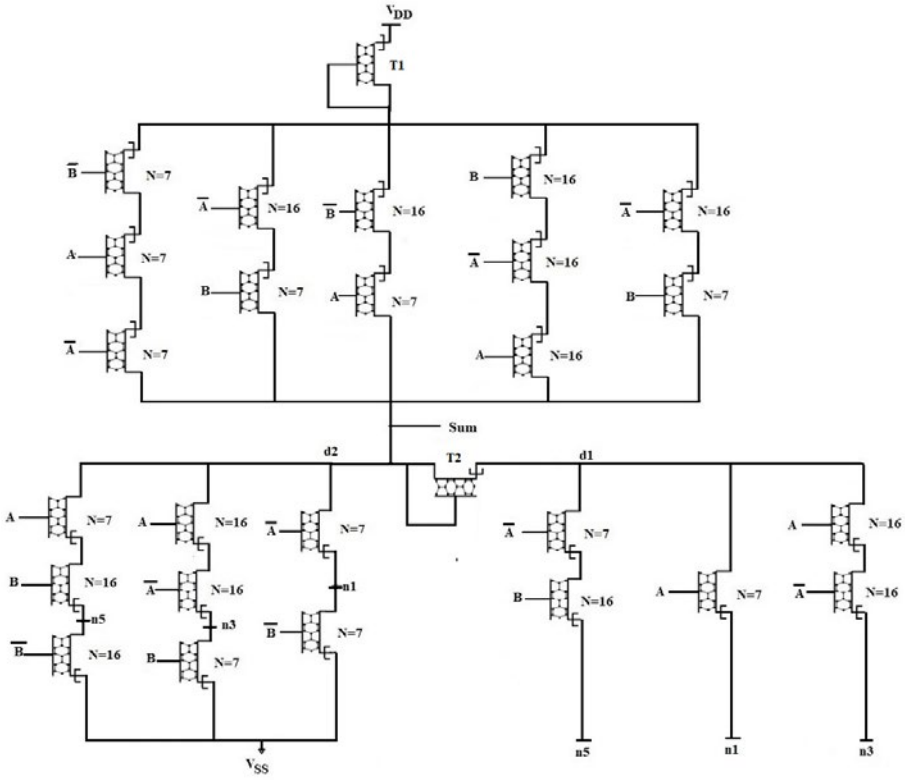


Fig. 4. The second proposed design

of carry. The carry output includes only two logic value, 0 and 1. Thus, only using N-type GNRFET can make the carry. C1 node from the carry with logic value 1 and C0 node create the 0 logic value. The transient responses of the proposed design are demonstrated in Fig. 3(c). The output is the full swing, and the value of them is accurate.

The Second Proposed Design

In this design, the transistors are applied rather than resistors. Using the transistors reduces delay and area chip significantly. The transistors of n1, n3, and n5 nodes were the same. For optimum designing, similar transistors have been omitted. Fig. 4 shows the schematic of the circuit design. T1 and T2 are the transistors that are replaced with the resistors. The dimer line of these transistors is 18.

Simulation Results and Comparison

In similar HSPICE parameter with the first design, the results of the FOM parameters are obtained in Table 4. As can be seen, the proposed ternary half adder based on GNRFET has a lower delay and PDP, and higher power consumption Compared to its counterpart CNTFET technology. The number of transistors is also reduced from 140 in ref [20] to 58 in the second proposed design. In the comparison of other references, using GNRFET for ternary design achieve the best improvement over in terms of PDP.

CONCLUSION

Graphene with wonderful electronic properties can be an alternative device for traditional transistors. Graphene in shape of nanoribbon has enough band gap to make the transistor on and off as well. Then, using GNRFET as the digital circuit design can be advantages. In this paper, the low power, high speed, and full swing output ternary adder circuits are proposed for the first time. These structures are suitable for use with a 0.9V supply voltage level at 33MHz. The first proposed circuit uses only 52 transistors and 8 resistors for complete operation. The second proposed design uses 58 transistors. The simulation results show that the proposed design has least delay. Moreover, the PDP term of sum and carry are lower than all previous circuits. Therefore, using GNRFET in circuit design can be lead to create the ultra-high-speed digital circuits.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

REFERENCES

[1] Ebrahimi SA, Keshavarzian P. Fast low-power full-adders based on bridge style minority function and multiplexer for nanoscale. International Journal of Electronics. 2013 Jun 1;100(6):727-45. https://doi.org/10.1080/00207217.2012.720948

[2] Bagherizadeh M, Eshghi M. Two novel low-power and high-speed dynamic carbon nanotube full-adder cells. Nanoscale research letters. 2011 Dec 1;6(1):519. https://doi.org/10.1186/1556-276X-6-519

[3] Pelayo FJ, Prieto A, Lloris A, Ortega J. CMOS current-mode multivalued PLAs. IEEE transactions on circuits and systems. 1991 Apr 1; 38(4):434-41. https://doi.org/10.1109/31.75400

[4] Zhang WC, Wu NJ. Compact voltage-mode multi-valued literal gate using nanoscale ballistic MOSFETs. Electronics Letters. 2008 Jul 31; 44(16):968-9. https://doi.org/ 10.1049/el:20080507

[5] Mahani AT, Keshavarzian P. A novel energy-efficient and high-speed full adder using CNTFET. Microelectronics Journal. 2017 Mar 1; 61:79-88. https://doi.org/10.1016/j.mejo.2017.01.009

[6] Choudhury MR, Yoon Y, Guo J, Mohanram K. Graphene nanoribbon FETs: Technology exploration for performance and reliability. IEEE transactions on nanotechnology. 2011 Jul; 10(4):727-36. https://doi.org/10.1109/TNANO.2010.2073718

[7] Schwierz F. Graphene transistors. Nature nanotechnology. 2010 Jul;5(7):487. https://doi.org/10.1038/nnano.2010.89

[8] Roy JN, Bhowmik P, Chattopadhyay T. Design of all optical ternary logic based half adder circuit and it's applications. Journal of Optics. 2015 Dec 1; 44(4):322-9. https://doi.org/10.1007/s12596-015-0279-0.

[9] Lin S, Kim YB, Lombardi F. A novel CNTFET-based ternary logic gate design. In Circuits and Systems, 2009. MWSCAS'09. 52nd IEEE International Midwest Symposium on 2009 Aug 2 (pp. 435-438). IEEE. https://doi.org/10.1109/MWSCAS.2009.5236063

[10] Moaiyeri MH, Mirzaee RF, Navi K, Hashemipour O. Efficient CNTFET-based ternary full adder cells for nanoelectronics. Nano-Micro Letters. 2011 Mar 1;3(1):43-50. https://doi.org/10.1007/BF03353650

[11] Lin S, Kim YB, Lombardi F. CNTFET-based design of ternary logic gates and arithmetic circuits. IEEE transactions on nanotechnology. 2011 Mar; 10(2):217-25. https://doi.org/10.1109/TNANO.2009.2036845

[12] Raychowdhury A, Roy K. Carbon-nanotube-based voltage-mode multiple-valued logic design. IEEE Transactions on Nanotechnology. 2005 Mar;4(2):168-79. https://doi.org/10.1109/TNANO.2004.842068

[13] Smith KC. The prospects for multivalued logic: A technology and applications view. IEEE Transactions on Computers. 1981 Sep 1(9):619-34.

[14] Rizvi AA, Zaheer K, Zubairy MS. Design of ternary half-adder and-subtractor using frequency modulation in grating structures. Optics communications. 1991 Aug 1; 84(5-6):247-50. https://doi.org/10.1016/0030-4018(91)90081-N

[15] Motamedi, M., Naghdi, A. The Molecular Mechanics Model of Carbon Allotropes. Journal of Nanoanalysis, 2017; 4(4): 334-342. doi: 10.22034/jna.2017.540019.

[16] Afshari, S., JahanbinSardroodi, J., Mohammadpour, H. (2017). 'Electronic Behavior of Doped GrapheneNanoribbon Device: NEGF+DFT', Journal of Nanoanalysis, 4(4), pp. 272-279. doi: 10.22034/jna.2017.539940.

[17] Choudhury MR, Yoon Y, Guo J, Mohanram K. Graphene nanoribbon FETs: Technology exploration for performance and reliability. IEEE transactions on nanotechnology. 2011 Jul;10(4):727-36. https://doi.org/10.1109/TNANO.2010.2073718

[18] Chen YY, Sangai A, Rogachev A, Gholipour M, Iannaccone G, Fiori G, Chen D. A SPICE-compatible model of MOS-type graphene nano-ribbon field-effect transistors enabling gate-and circuit-level delay and power analysis under process variation. IEEE Transactions on Nanotechnology. 2015 Nov 1; 14(6):1068-82. https://doi.org /10.1109/TNANO.2015.2469647

[19] Jiao L, Wang X, Diankov G, Wang H, Dai H. Facile synthesis of high-quality graphene nanoribbons. Nature nanotechnology. 2010 May;5(5):321. https://doi.org/10.1038/nnano.2010.54

[20] Keshavarzian P, Sarikhani R. A novel CNTFET-based ternary full adder. Circuits, Systems, and Signal Processing. 2014 Mar 1;33(3):665-79. https://doi.org/10.1007/s00034-013-9672-6

[21] Illinois University GNRFET model website. Illinois University, Available: http://dchen.ece.illinois.edu/tools.html

[22] Moaiyeri MH, Doostaregan A, Navi K. Design of energy-efficient and robust ternary circuits for nanotechnology. IET Circuits, Devices & Systems. 2011 Jul 1; 5 (4):285-96. https://doi.org/10.1049/iet-cds.2010.0340

[23] Shahrom E, Hosseini SA. A New Low Power Multiplexer Based Ternary Multiplier Using CNTFETs. AEU-International Journal of Electronics and Communications. 2018 Jun 7. https://doi.org/10.1016/j.aeue.2018.06.011