RESEARCH ARTICLE

An innovative method for estimating optimal Gate work function and dielectric constant of a nanoscale DG-TFET based on analytical modeling of tunneling length in ambipolar, Off and ON states

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ABSTRACT

In this paper, we propose an innovative and low computational cost approach that can be used to find optimal values of parameters of a nanoscale dual gate tunneling field-effect transistor (DG-TFET). In this way, after obtaining analytical expressions for potential and energy bands of the device using the Poisson equation, the tunneling length is extracted at source-channel and channel-drain tunnel junctions in the AMBIPOLAR, Off and On states. Due to the tunneling length equation, the different values of gate work function and dielectric constant of the device are swept to determine the minimum and maximum design limits. According to the above range, the necessary checks are made to reach the local optimal behaviors. These optimum points are explained based on the achievement of optimal device performance. The accuracy and consistency of the proposed model is validated with the TCAD simulation results. The present model can be a handful for the study of TFET performance.

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INTRODUCTION

Scaling of conventional CMOS transistors according to Moore's law is facing several challenges, such as high OFF-state current, high sub-threshold slope (SS) and other short channel effects (SCEs). The above-mentioned causes poor operation of the device and high power consumption in chips[1–5]. Hence, the proposal of a new device is inevitable. The tunneling field-effect transistor (TFET) is a decent choice because of energy efficiency and lower sub-threshold slope (SS) [6–8]. The major weaknesses of TFETs are low drain current due to poor band to band tunneling rate and conduction in the positive and negative voltages of the gate (ambipolarity). Several studies have been conducted to overcome these shortcomings that are beyond the scope of this paper [9–14]. One of the main areas of research in the field of semiconductor devices is analytical modeling. Analytical modeling can be useful in the rapid and low-cost evaluation of semiconductor devices. It is also used to offer a model for simulator software [15,16]. Some researchers proposed analytical modeling for TFET using the MOSFET model [17]. Many researchers study the Sub-threshold swing and the threshold voltage of TFET [18,19].

Several analytical studies try to offer a 2-D

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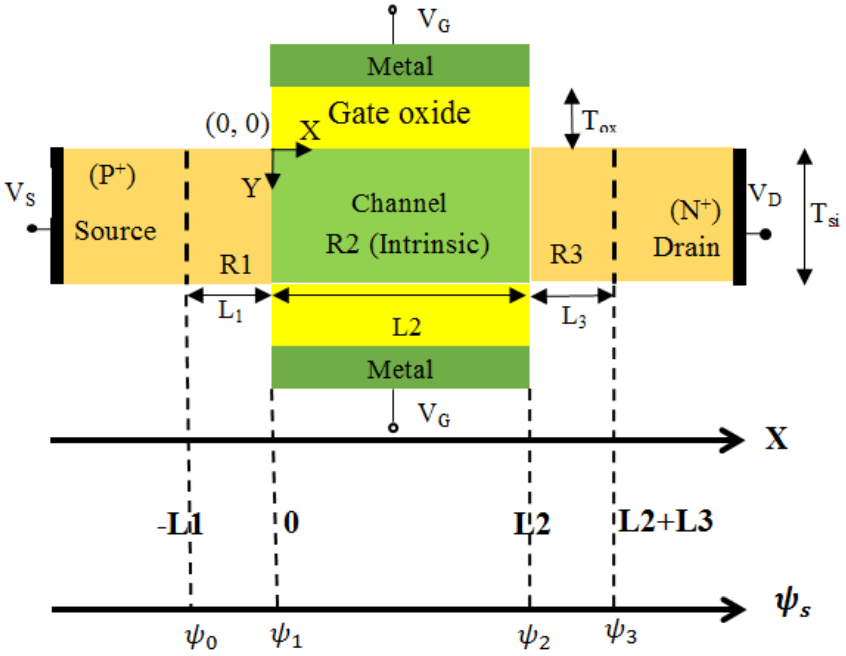


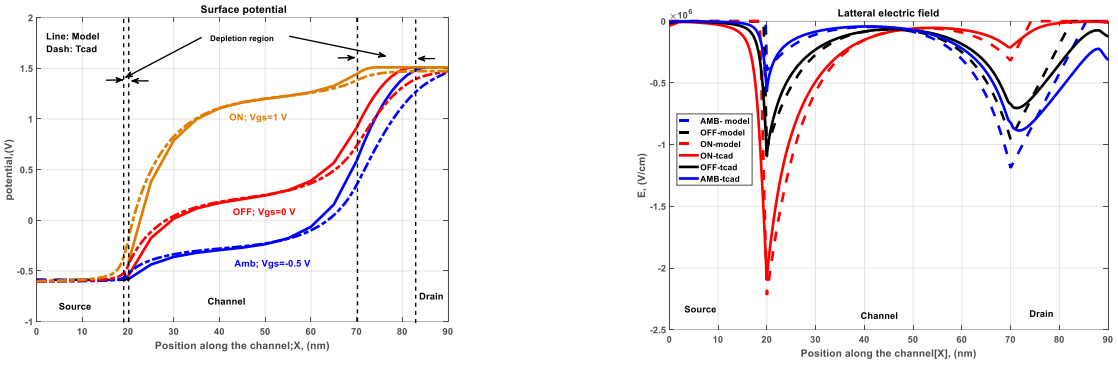
Fig. 1. Schematic view of DG-TFET.

or 3-D expression for TFETs with or without considering the impact of the depletion region, mobile charge and drain voltage. Many 2-D studies on TFET modeling analytically calculate the tunneling generation rate using a 2-D electric field and Some studies emphasize the modeling of different physical structures of the device[19–24]. While some other researchers consider device modeling according to the type of insulator and shape and number of gates. Investigating the performance of the TFETs by using the analytical modeling also did not exclude the attention of researchers. Many attempts have focused on analytical modeling of junction-less TFETs [25]. In this paper, we start with the modeling of the surface potential along the channel using a pseudo-2D model [26] considering the depletion regions at source-channel and channel drain junction. We then find the smallest tunneling length which is very essential to finding drain current and in our proposed method. The method presented in this paper is to find the proper values of the work-function of the gate and the dielectric constant with respect to the tunneling length. We derive the tunneling length for AMBIPOLAR, OFF and ON state at different values of the gate work-function and dielectric constant using our proposed method. The two-dimensional curve obtained from this step is analyzed in order to obtain the appropriate values of the parameters. The method of analysis is a combination of qualitative analysis, evaluation of maximum or minimum points of the curves, and also referring to the TCAD simulation results. We believe that this method while avoiding complex optimization procedures is useful in achieving the desired device efficiency. A 2-D dimensional numerical simulation validates accuracy of the proposed model.

The rest of the paper is organized as follows: In section 2, device structure and analytical modeling of surface potential will be discussed. The tunneling length in AMBIPOLAR, OFF and ON state also will be presented in section 3. The validation of our proposed method also is described in Section 4. Results and discussions and finally the conclusion will be presented in sections 5 and 6 respectively.

MATERIALS AND METHODS

Fig. 2. shows a 2-D structure of a dual gate tunneling field-effect transistor (DG-TFET). The total gate length is L2. The silicon body and oxide thicknesses are T_{si} and T_{ox} respectively. The Source and the drain are highly doped with p and n-type dopant at a concentration of N1 and N3. The channel region is lightly doped with N2. Regions R1, R2 and R3 demonstrate depletion region at the source side, channel region under the gate and drain side depletion region respectively. L1 and



(a) (b)

Fig. 2. Surface potential of DG-TFET (a) and Lateral electric field (b) for ON state: V_{gs}=1 V and V_{ds}=1 V; OFF state: V_{gs}=0 V and V_{ds}=1 V and AMBIPOLAR state: V_{gs}=-0.5 V and V_{ds}=1 V.

Table 1. Device design and material parameters.

Parameter name	Symbol	Value	unit
Gate oxide thickness	T_{ox}	3	nm
Silicon body thickness	T_{si}	12	nm
Source doping concentration	N_1	1×10^{20}	cm^{-3}
Channel doping concentration	N_2	1×10^{16}	cm^{-3}
Drain doping concentration	N_3	-5×10^{18}	cm^{-3}
Metal work-function	ϕ_m	4.5	eV
Source region length	L_S	20	nm
Gate length	L_G	50	nm
Drain region length	L_D	20	nm
Dielectric constant	ε_{ox}	3.9	-

L3 are depletion region length. The other Physical characteristics of the device are listed in Table 1

2-D Poisson's Equation in the Channel

Neglecting the mobile charge, the 2-D Poisson's equation in the channel region of the device is given by[27]:

$$\frac{\partial^2\psi_2(x,y)}{\partial x^2}+\frac{\partial^2\psi_2(x,y)}{\partial x^2}=\frac{qN_2}{\varepsilon_{Si}} \quad (1)$$

Where $\psi_2(x,y)$ demonstrates the 2-D electrostatic potential in the channel, q is the electronic charge, ε_{Si} is the permittivity of silicon and N_2 is the channel concentration. The potential distribution along the channel can be approximated by the second-order polynomial as [28–34]:

$$\psi_2(x,y)=a_0(x)+a_1(x)y+a_2(x)y^2 \quad (2)$$

Where a_0, a_1 and a_2 are channel length-dependent obtained from properly defined boundary conditions. Using boundary conditions, the surface potential of the channel $\psi_{s2}(x)$ can be found as:

$$\psi_2(x,y)=\psi_{s2}(x)+\frac{C_{ox}\left(V_{GS}-\varnothing_{ms}-\psi_s(x)\right)}{\varepsilon_{Si}}\times y-\frac{C_{ox}\left(V_{GS}-\varnothing_{ms}-\psi_s(x)\right)}{\varepsilon_{Si}.T_{Si}}\times y^2 \quad (3)$$

Where, $C_{ox}=\varepsilon_{ox}/T_{ox}$ and $\varnothing_{ms}=\varnothing_{metal}-\varnothing_{Si}$ are oxide capacitance and metal-silicon work-function difference. $\varnothing_{Si}$ Is the silicon work-function as $\chi+E_g/2q$, where χ is the electron affinity of the silicon. Substituting (3) in (1) yields the following1-D second orders differential equation:

$$\frac{d^2\psi_{s2}(x)}{dx^2}+K^2\psi_{s2}(x)=\sigma \quad (4)$$

Where

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$$\mathrm{K}=\sqrt{\frac{2C_{ox)}}{\varepsilon_{Si}.T_{Si}}};\ \sigma=\frac{qN_2}{\varepsilon_{Si}}+\frac{2C_{ox}}{\varepsilon_{Si}.T_{Si}}V_{GS}{}';\quad \text{and}\quad V_{GS}{}'=V_{GS}-\varnothing_{ms} \tag{5}$$

The general and particular solution of (4) is:

$$\begin{aligned}&\text{ø}_{s2}(\mathrm{x})=\mathrm{A}_2\exp(\mathrm{Kx})+\mathrm{B}_2\exp(-\mathrm{Kx})+\xi;\\&\xi=\sigma/K^2\end{aligned} \tag{6}$$

Hence using the potential continuity in the interfaces of two consecutive regions, the coefficients of (6) are:

$$A_2=\frac{-1}{2\sinh(KL_2)}\left[(\psi_1-\xi)\exp(-KL_2)-(\psi_2-\xi)\right] \tag{7}$$

$$B_2=\frac{-1}{2\sinh(KL_2)}\left[(\psi_2-\xi)-(\psi_1-\xi)\exp(KL_2)\right] \tag{8}$$

The interface potential of ψ_1 and ψ_2 are derived using the continuity of potential and electric field which will be discussed later.

Poisson's Equation in the Depletion regions

The precise modeling of channel potential involves the consideration of drain and source depletion regions. As is obtained from the TCAD simulation and according to report [35], the major changes in surface potential of region R1 and R2 are along the channel, therefore, we solve the Poisson equation in these regions one-dimensionally. The 1-D Poisson's equation inside the depletion regions of the device is expressed as:

$$\frac{d^2\psi_{s1}(x)}{dx^2}=\frac{qN_1}{\varepsilon_{Si}};\quad -L_1\le x\le 0 \tag{9}$$

$$\frac{d^2\psi_{s3}(x)}{dx^2}=-\frac{qN_3}{\varepsilon_{Si}};\quad 0\le x\le L_2+L_3 \tag{10}$$

Twice integrating the (9)-(10), we get the following expression for $\psi_{s1}(x)$ and $\psi_{s3}(x)$ given by:

$$\psi_{s1}(x)=\frac{qN1}{2\varepsilon_{Si}}(x+L_1)^2+A_1(x+L_1)+B_1 \tag{11}$$

$$\psi_{s3}(x)=-\frac{qN3}{2\varepsilon_{Si}}(x-L_2)^2+A_3(x-L_2)+B_3 \tag{12}$$

The extension of the depletion region in the source is as far as the electrostatic potential becomes a constant value of $\psi_0=\frac{K_B T}{q}ln\frac{N1}{n_i}$ which is called built-in potential (ψ_0). At this point, the electric field will be zero. Meanwhile, the extension of the depletion region in the drain side is as high as the potential reaches the value of $\psi_3=\frac{K_B T}{q}ln\frac{N3}{n_i}+V_D$ and the electric field becomes zero. (K_B is the Boltzmann constant). Using the above-mentioned boundary conditions the other coefficients are as follows:

$$A_1=\frac{(\psi_1-\psi_0)-\frac{qN1}{2\varepsilon_{Si}}\times L_1{}^2}{L_1} \tag{13}$$

$$A_3=\frac{(\psi_3-\psi_2)+\frac{qN3}{2\varepsilon_{Si}}\times L_3{}^2}{L_3} \tag{14}$$

$$B_3=\psi_2 \tag{15}$$

And the depletion region length at source and drain side will be derived using the value of the electric field at $x=-L_1$ and $x=L_2+L_3$ as:

$$E_1(x)=\left.\frac{\partial\psi_{s1}(x)}{\partial x}\right|_{x=-L_1}=0 \tag{16}$$

$$E_3(x)=\left.\frac{\partial\psi_{s3}(x)}{\partial x}\right|_{x=L_2+L_3}=0 \tag{17}$$

Solving equations (16)-(17) yields depletion region length as:

$$L_1=\sqrt{2\varepsilon_{Si}(\psi_1-\psi_0)/qN1} \tag{18}$$

$$L_3=\sqrt{2\varepsilon_{Si}(\psi_3-\psi_2)/qN3} \tag{19}$$

The intermediate potential (ψ_1 *and* ψ_2) can be calculated using the continuity of potential at channel-source and channel-drain interfaces as:

$$\psi_{s1}|_{x=0}=\psi_{s2}|_{x=0}\Rightarrow\tfrac{qN1}{2\varepsilon_{Si}}(L_1)^2+A_1(L_1)+B_1=\mathrm{A}_2+\mathrm{B}_2+\xi \tag{20}$$

$$\psi_{s2}|_{x=L_2}=\psi_{s3}|_{x=L_2}\Rightarrow\mathrm{A}_2\exp(\mathrm{K}L_2)+\mathrm{B}_2\exp(-\mathrm{K}L_2)+\xi=B_3 \tag{21}$$

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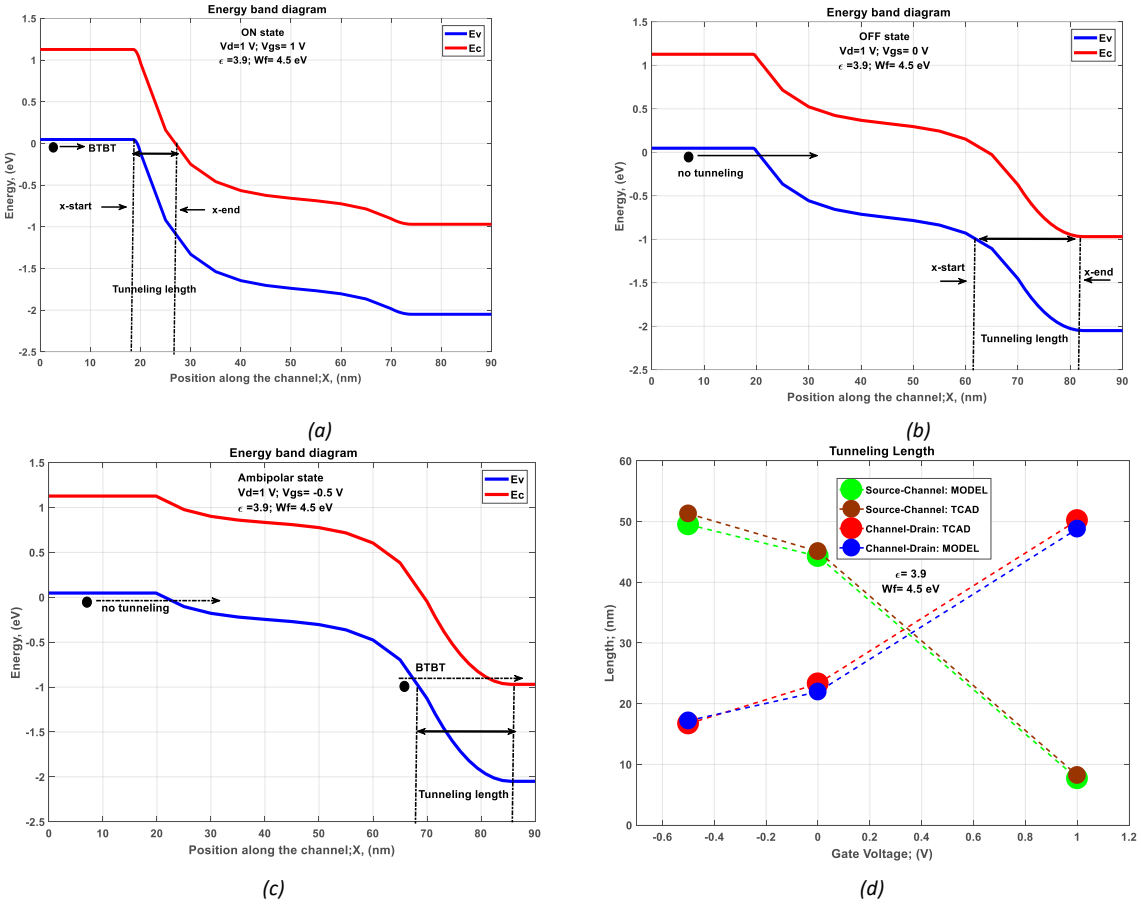

Fig. 3. Source-channel and Channel-Drain tunneling length of DG-TFET for AMBIPOLAR, OFF and ON state (a); Energy band diagram in the ON state (b); OFF state (c) and AMBIPOLAR state (d).

We find ψ_1, ψ_2 from above-mentioned system of nonlinear equations.

Tunneling length

The tunneling length is the physical path through which the band to band tunneling occurs. This path occurs in the ON, OFF and the AMBIPOLAR state. The difference is in the tunneling region and hence the starting and endpoint. The tunneling length is a path between the two equal potential points. To understand and analyze the tunneling length, we need the energy band diagram in different biasing conditions[36, 37] as:

$$E_C(x) = -\psi_s(x) + \frac{E_g}{2} \quad , \quad E_V(x) = -\psi_s(x) - \frac{E_g}{2} \quad (22)$$

The surface potential of the DG-TFET is shown in Fig. 2(a) for ON, OFF and AMBIPOLAR state. As we expect, an extension of the depletion region at the drain side is more because of higher reverse bias in this side. The lateral electric field is shown in Fig. 2(b). A good agreement between the model and TCAD results is seen.

Source-Channel Junction Tunneling length

The energy band diagram of the DG-TFET in the ON state is shown in Fig. 3(a). The closure of the Fermi level with the valence band of the source to the corresponding point in the conduction band of the channel is the minimum tunneling length. However, because of the high level of doping in the source, the difference between the Fermi and valence band can be ignored. Thus, the tunneling starts from the junction of the depletion region with the source and ends in a point in the channel conduction band which the energy value of the

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start and endpoints of the tunneling is equal. Accordingly, one can write:

$$E_{V-Source}(x)\Big|_{x=x_{start}} = E_{C-Channel}(x)\Big|_{x=x_{end}} \quad (23)$$

$$\left(-\psi_0 - \frac{E_g}{2}\right) = \left(-\psi_{S2}(x) + \frac{E_g}{2}\right) \quad (24)$$

Using (6) and $x_{start} = -L_1$ from (18), the tunneling length in the ON state is expressed as follow:

$$L_{Source-Channel} = \frac{Log\left(\frac{-(\xi-\psi_0-E_g)+\sqrt{(\xi-\psi_0-E_g)^2-4A_2B_2}}{2A_2}\right)}{K} - L_1 \quad (25)$$

Channel-Drain Junction Tunneling length

The energy band alignment between the channel valence band and the drain conduction band is also observed for OFF and Ambipolar state. The energy band diagram in the OFF and the Ambipolar state is shown in Fig. 3(b) and Fig. 3(c) respectively. The tunneling path starts from the channel valence band and ends to drain conduction band. The endpoint is the end of the depletion region extension at the drain side. To achieve the main equation, it is enough to equal the amount of energy at the start and endpoints of the tunneling, as below:

$$E_{V-Channel}(x)\Big|_{x=x_{start}} = E_{C-CDrain}(x)\Big|_{x=x_{end}} \quad (26)$$

$$\left(-\psi_{s2}(x) - \frac{E_g}{2}\right) = \left(-\psi_3 + \frac{E_g}{2}\right) \quad (27)$$

Using (6) and (12) one can write:

$$L_{Channel-Drain} = (L_2+L_3) - \frac{Log\left(\frac{-(\xi-E_{end}+E_g)+\sqrt{(\xi-E_{end}+E_g)^2-4A_2B_2}}{2A_2}\right)}{K} \quad (28)$$

Where

$$E_{end} = \left(-\frac{qN3}{2\varepsilon_{Si}}(L_3)^2 + A_3(L_3) + B_3\right) \quad (29)$$

The method for calculating the tunneling length in the Ambipolar state is exactly the same as the OFF state because the tunneling phenomenon occurs in the same region Fig. 3(c).

Model validation

The accuracy of the proposed model is verified by comparing the numerical modeling results with 2D numerical simulations. SILVACO ATLAS 2D 5.19.20 R is employed for all simulations. The models used include Shockley Read Hall (SRH) and Auger (AUGER) recombination models, Fermi-Dirac statistics and band-gap narrowing model (BGN) [45–47].

RESULTS AND DISCUSSIONS

The tunneling length at Source-Channel and Channel-Drain junction at Ambipolar, OFF and ON state is shown in Fig. 3(d). Good consistency between the model and TCAD is observed. After extracting an expression for tunneling length, we assign the different values of the gate work-function and the dielectric constant of the insulator. The result is a three-dimensional graph, which can be used to evaluate the performance of the device. The purpose of this assessment is to reach the optimal local points for the least OFF and Ambipolar current and the highest ON current. It should be noted that the basis of our judgment is the tunneling length in each case. The three-dimensional curves of the tunneling length in the source and drain side junction for various states are shown in Fig. 4. -Fig. 6. The preliminary study of 3D curves can be summarized as follows:

1. In the Ambipolar state, the tunneling length in the channel-drain junction is maximal when the work-function is equal to 4 eV (Fig. 4(b)). On the other hand, this amount of work-function minimizes the tunneling length at the source side, which is undesirable (Fig. 4(a)). Therefore, the work-function must be selected in such a way that both tunneling lengths are in the optimal position. Therefore, the intermediate values of the work-function, (e.g. 4.2 or 4.3 eV), are suggested.

2. In the OFF state, tunneling in the source-channel junction is more influenced by the gate work-function than the dielectric constant (Fig. 5(a)). In other words, it is necessary to avoid the lower values of the work-function. At the same time, the lower value of the gate work-function reduces the tunneling length in the channel-drain junction (Fig. 5(b)), which is not at all desirable.

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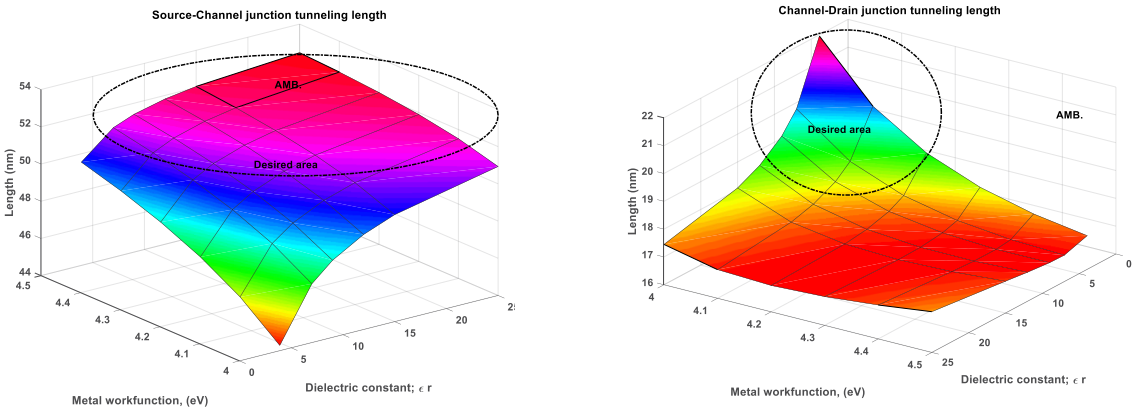

Fig. 4. The effect of dielectric constant and gate work-function on tunneling length of Source-Channel junction (a) and Channel-Drain junction (b) in the AMBIPOLAR state (V_{ds}=1 V and V_{gs}=-0.5 V).

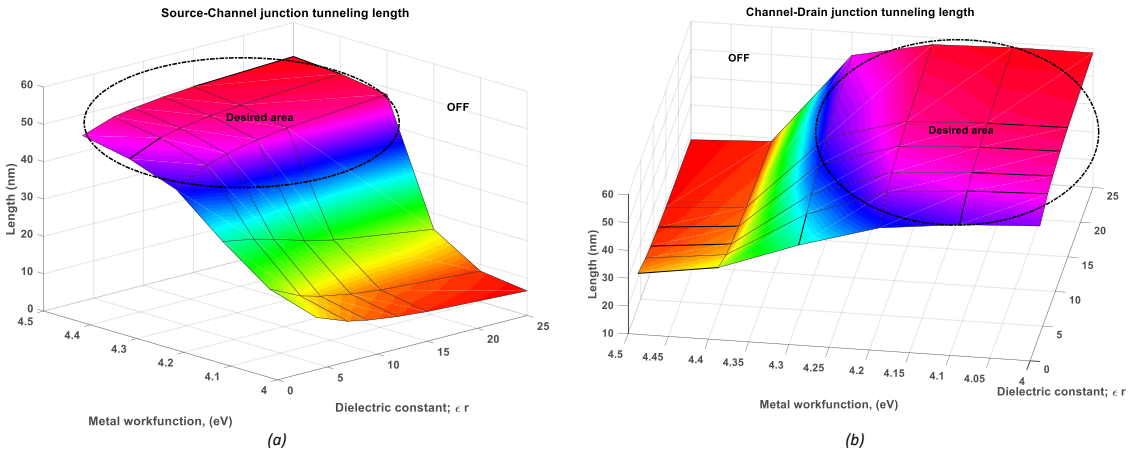

Fig. 5. The effect of dielectric constant and gate work-function on tunneling length of Source-Channel junction (a) and Channel-Drain junction (b) in the OFF state (V_{ds}=1 V and V_{gs}= 0 V).

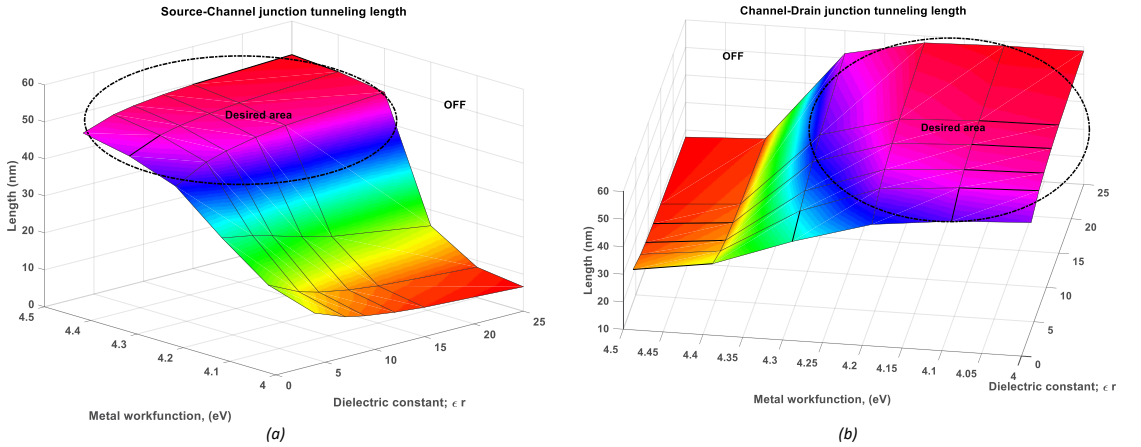

Fig. 6. The effect of dielectric constant and gate work-function on tunneling length of Source-Channel junction (a) and Channel-Drain junction (b) in the ON state (V_{ds}=1 V and V_{gs}=1 V).

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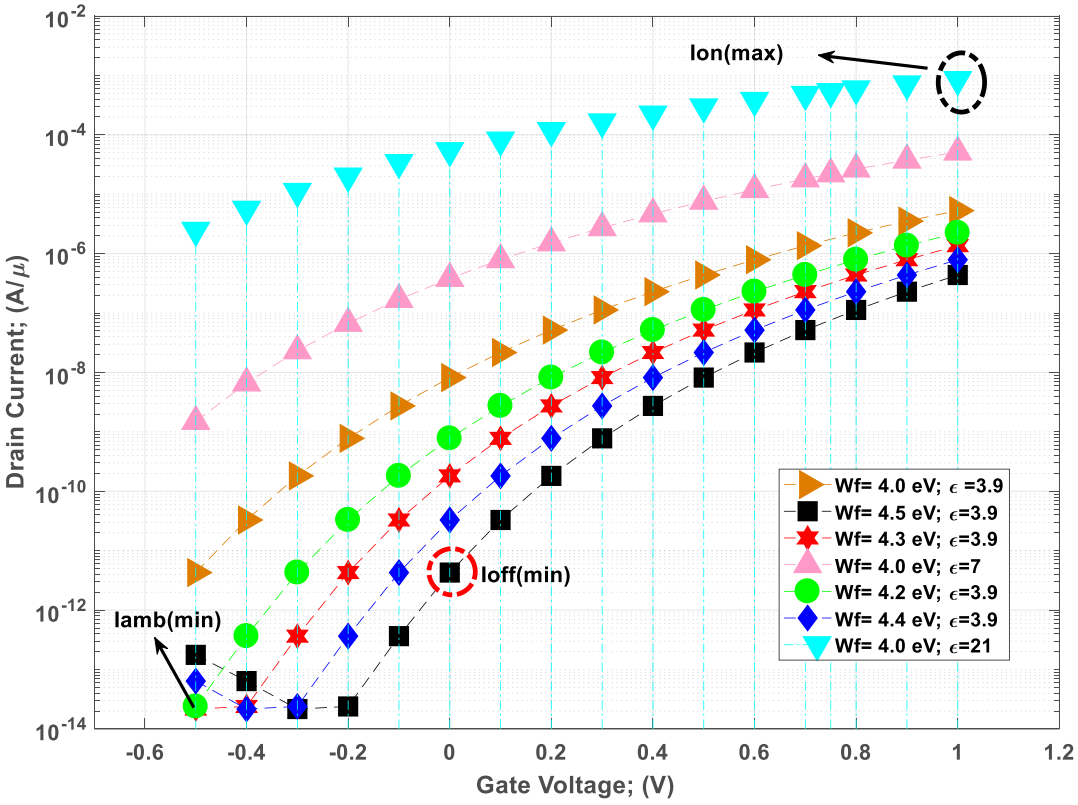

Fig. 7. Drain current of DG-TFET extracted from our model and SILVACO TCAD simulation tool.

Therefore, the higher values of the work-function are preferable. Taking into account simultaneously the realities associated with the tunneling length in the source-channel and channel-drain junction, the higher values of the work-function can be an optimal choice to keep the OFF current down.

3. In the ON state, the tunneling length in the channel-drain is so high that there is no band to band tunneling in this junction (Fig. 6(b)). In other words, the dielectric constant and the work-function do not interfere in the tunneling of this junction. Meanwhile, the effect of dielectric constant on the source-channel junction tunneling length is more than work-function (Fig. 6(a)). Therefore, selecting high values of dielectric constant reduces the tunneling length and, as a result, increases the drain current (I_{ON}).

In order to verify our proposed method, we examine the values of the gate work-function as well as the dielectric constant corresponding to each of the optimal states in the TCAD. The drain current corresponding to each of the above states is shown in Fig. 7. According to the above, high dielectric constant values with any value of work-function can improve the ON current. This is clearly shown in (Fig. 7) for (Wf=4 eV; ε_r=7) and (Wf=4 eV; ε_r=21). In these two samples, we have the highest ON current. In the case where the work unction is selected in range 4.2 eV to 4.3 eV, the Ambipolar current is very low. Also, with a work-function equal to 4.5 eV, the minimum OFF current is achievable.

CONCLUSION

The idea of analytical modeling of DG-TFET can extract a closed-form formula for tunneling length in source-channel and channel-drain junctions. From the perspective of the energy band diagram, surface potential and, lateral electric field, the model corresponds well to the simulation results. To achieve optimal conditions, simultaneous effects of different values of the gate work-function and dielectric constant on the tunneling length in Ambipolar, OFF and ON state have been investigated which has a good agreement with simulation results. Based on the results, the

allowable values of the gate work-function and dielectric constant are determined according to the principles of minimum Ambipolar and OFF current and maximum ON current. The simulation results confirm the correctness of this proposal.

CONFLICT OF INTEREST

All authors declare that no conflicts of interest exist for the publication of this manuscript.

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