JOURNAL OF SOUTHERN COMMUNICATION ENGINEERING
ISLAMIC AZAD UNIVERSITY BUSHEHR BRANCH

E-ISSN: 2980-9231
https://jce.bushehr.iau.ir

https://doi.org/10.30495/jce.2023.1996352.1223

Vol. 14/ No. 54/Winter 2025

Research Article

Low-Power Differential Voltage-Controlled Ring Oscillator Based on Carbon Nanotube Field-Effect Transistor (CNTFET)

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Received: 13 September 2023
Revised: 2 December 2023
Accepted: 20 December 2023

Abstract

Due to the better common-mode elimination of power supply voltage and sub-substrate noise, the differential ring oscillator (DRO) performs better than the single-ended ring oscillator (SERO) in both analog and digital integrated circuits. Also, it is easy to achieve high frequency performance with in-phase and quadrature outputs in a differential ring oscillator. For this purpose, in this research, the design and simulation of a three-stage differential voltage controlled circular oscillator (DVCRO) based on carbon nanotube field effect transistor (CNTFET) is presented, whose oscillation frequency can be changed by changing the control voltage of the proposed delay cell structure. A very wide range changed from 45.7 GHz to 110.18 GHz, and at the same time, its power consumption is in the range of 5.17 µW to 32.68 µW. Based on the results obtained at the supply voltage of 0.9 V, the proposed voltage controlled ring oscillator (VCRO) based on carbon nanotube field effect transistor shows promising characteristics compared to its counterpart based on metal-oxide-semiconductor field effect transistor (MOSFET). Also, it performs exceptionally well compared to other existing oscillators.

Keywords: Carbon Nanotube Field Effect Transistor (CNTFET), Power Delay Product (PDP), delay cell, Differential Voltage Controlled Ring Oscillator (DVCRO), Single Ended Ring Oscillator (SERO).

Highlights

- Presentation of a new 9-transistor delay cell based on carbon nanotube field effect transistor (CNTFET).
- The changeability of the delay characteristic in the proposed delay cell by changing the control voltage.
- Providing a three-stage differential Voltage Controlled Oscillator (VCO) based on carbon nanotube field effect transistor in the high frequency range and beyond.
- Achieving a wide adjustment range with low power consumption in the proposed voltage-controlled oscillator.

Citation: S. Naseri Akbar, "Low-Power Differential Voltage-Controlled Ring Oscillator Based on Carbon Nanotube Field-Effect Transistor (CNTFET)," *Journal of Southern Communication Engineering*, vol. 14, no. 54, pp. 47–68, 2025, doi: 10.30495/jce.2023.1996352.1223, [in Persian].

1. Introduction

The integrated circuit market is growing rapidly with advancements in semiconductor modeling, transistor miniaturization, progress in manufacturing processes, and the rapid development of computer-aided design (CAD) tools. The scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs) to the nanoscale reveals numerous challenges [1]. One of the ideas for utilizing the electronic properties of nanotubes is to use them as a replacement for silicon in electronic circuits [3]. The nanometric dimensions of these materials and the quantum theories governing this type of material have made carbon nanotubes (CNTs) a suitable candidate for semiconductor technology [3].

Differential ring oscillators (DROs) integrated into CMOS technology have been used in numerous products over the years. The differential ring oscillator is a good design choice for integrated circuit designers due to its consistent use in various CMOS technologies. In [4], a millimeter-wave ring oscillator based on carbon nanotube field-effect transistors (CNTFETs) in 32 nm technology is presented, operating in the frequency range of 150 GHz and beyond. With the expansion of portable electronic devices, along with technology scaling and the limitations of reducing the MOSFET channel length, the design of low-power ring oscillators with a wide frequency range and tunability is essential for many applications. Significant efforts have been made by designers in this area [5-12].

The trend towards low-power applications and increased integration requires new structures for circuits. In this study, we aim to introduce a novel DRO using CNTFETs and demonstrate the advantages of the proposed design in enhancing the key parameters of an oscillator.

2. Innovation and contributions

Due to the elimination of common-mode noise and improved substrate noise suppression, the differential ring oscillator (DRO) demonstrates better performance compared to the single-ended ring oscillator (SERO) in analog and digital integrated circuits. Additionally, achieving high-frequency performance with in-phase and quadrature outputs is easier in the differential ring oscillator. In this study, the design and simulation of a three-stage voltage-controlled differential ring oscillator (DVCRO) based on CNTFET are presented. The oscillation frequency can be varied over a very wide range by adjusting the control voltage. The proposed voltage-controlled ring oscillator (VCRO) based on CNTFET exhibits promising features compared to its MOSFET-based counterpart. Among the many features of the proposed design, the following key contributions can be highlighted:

- Introduction of a novel 9-transistor delay cell based on CNTFETs.
- The ability to vary the delay characteristics of the proposed delay cell by adjusting the control voltage.
- Develop a three-stage VCDRO based on CNTFETs that is capable of operating in the high-frequency range and beyond.
- Achieving a wide tuning range with low power consumption in the proposed voltage-controlled oscillator (VCO).

3. Materials and Methods

A ring oscillator (RO) is constructed using an even or odd number of open-loop inverting amplifiers or delay cells (delay stages) connected in a positive feedback loop. During operation, if one of the nodes in the ring oscillator is triggered, the pulse propagates through all the cells and eventually inverts the polarity of the originally triggered node. The delay cells in a ring oscillator can be either single-ended or differential. A single-ended ring oscillator (SERO) consists of a chain of inverters formed by an NMOS and PMOS transistor, where the number of delay cells must be odd. The differential delay cells of a differential ring oscillator (DRO) can have either an odd or even number of stages and are constructed by using a load (active and passive elements) with a pair of differential inputs formed by NMOS differential pairs or push-pull inverters. Both single-ended and differential topologies can be utilized in the design of fully integrated CMOS voltage-controlled oscillators (VCOs).

The proposed delay cell, based on CNTFETs, is designed for use in the structure of the proposed oscillator and allows delay adjustment through the control voltage (V_{CTRL}). The CNTFET used here is a MOSFET-like CNTFET. This choice is due to the superior device parameters and the ease of fabrication of MOSFET-like CNTFETs compared to Schottky-barrier CNTFETs, making MOSFET-like CNTFETs more suitable for high-frequency performance applications.

4. Results and Discussion

The proposed design was simulated using 32 nm CNTFET technology with a supply voltage of 0.9 V. The performance of the proposed DRO based on CNTFETs is compared with other low-power designs from recent studies in Table 1. As observed, the current research demonstrates improved performance compared to the latest studies, resulting in the lowest power-delay product (PDP) with a supply voltage of 0.9 V. At the same time, it offers a high oscillation frequency and a wide tuning range. It is noteworthy that the proposed design is the only one with differential outputs, while all the other compared designs are single-ended. In terms of the phase noise figure of merit (FoM), only the design presented in [13] shows a slight advantage over the proposed design. However, when evaluating the PDP figure of merit for the design in [13], it becomes clear that, despite being a three-stage structure, its PDP value is significantly high, and it exhibits high power consumption. Therefore, the proposed design in this study offers significantly better capabilities compared to the design in [13].

5. Conclusion

In this study, the design and simulation of a high-performance three-stage DRO based on CNTFETs is presented. The oscillation frequency of the proposed DRO, with a supply voltage of 0.9 V, can be adjusted from 110 GHz to 120 GHz by varying the number of nanotubes, while its power consumption ranges from 33.3 µW to 162 µW. Additionally, by adjusting the control voltage in the proposed delay cell structure, the oscillation frequency can be tuned over a wide range from 45.7 GHz to 110.18 GHz, with power consumption varying from 5.17 µW to 32.68 µW. The designed DRO based on CNTFETs exhibits promising characteristics compared to its MOSFET-based counterpart and demonstrates superior performance compared to other existing oscillators.

6. Acknowledgement

I am grateful to the esteemed Professor Mr. Amir Baghi Rahin, whose dedicated guidance made this research possible.

7. References

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Appendix

Table 1. Comparison of the proposed design with other previous works

Ref.	Technology	Supply Voltage (V)	$F_{osc.}$ (GHz)	Power (μW)	Phase Noise @ 1MHZ (dBc/Hz)	PDP (fJ)	FoM (dBc/Hz)
[6]	32nm DG-CNTFET	0.7	110.91	25.502	-	0.0162	_
			77.61	24.888	-	0.0222	_
			107.6-110.9	25.51-24.89	-	0.0189-0.0164	_
[5]	32nm CMOS-CNTFET	0.8	6.39	2.872	-	0.0748	_
			20.093	4.973	-	0.0412	_
			22.33	3.917	-	0.0292	_
			5.85	2.859	-	0.0813	_
[4]	32nm CMOS-CNTFET	0.8	0.62-1.85	5.31-20.18	-	1.425-1.816	_
			0.42-1.26	3.22-13.65	-	1.26-1.799	_
[11]	180nm CMOS	0.8	0.41-0.66	22.30-32.22	-	8.03-8.94	_
[8]	32nm CNTFET	0.8	274.56-348-29	92.49-120.96	-	0.0558-0.0578	_
			96.18-196.87	86.83-199.17	-	0.0877-0.125	_
			55.04-140.86	139.99-294.58	-	0.128-0.181	_
[7]	16nm GNRFET	0.8	192.07-264-38	3.11-3.46	-	0.00207-0.0027	_
			126.21-180.83	3.75-4.55	-	0.0021-0.0036	_
			94.70-129.61	4.23-5.86	-	0.0023-0.0044	_
[9]	32nm CNTFET		33.64-43.74	14.02-18.78	-	0.053-0.093	_
			16.69-40.86	15.44-18.06	-	0.059-0.180	_
			20.54-26.11	15.32-29.13	-	0.058-0.141	_
			9.56-25.37	16.98-29.55	-	0.0645-0.309	_
			15.61-19.15	16.63-43.80	-	0.062-0.20	_
			6.98-18.59	18.48-48.40	-	0.0692-0.495	_
[10]	16nm GNRFET	0.8	19.75-178.71	0.18-1.33	-	0.0939-1.098	_
[14]	180nm CMOS	1.8	0.261-1.32	1600	-98	-	-153.21
[15]	180nm CMOS	1.8	3.1-10	6010	-113	-	-181.60
[16]	65nm CMOS	1.2	0.001-13.8	785	-82	-	-157.30
[17]	180nm GFET	1	24.12	9980	-104.1	-	-181.74
[18]	180nm CMOS-CNTFET	1.8	3.12-5.26	625	-	-	_
[19]	32nm CNTFET	1	6-20	7500	-123	62.5-208.33	-202.13
[13]	CNTFET	1.5	0.46	60000	-116	-	-151.46
Proposed	32nm CNTFET	0.9	45.70-110.18	5.17-32.68	-88	0.0188-0.049	-200.68

Declaration of Competing Interest: Authors do not have conflict of interest. The content of the paper is approved by the authors.

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Author Contributions: All authors reviewed the manuscript.

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