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Research Article

A New Model for Enhancing Efficiency in On-Chip Optical Networks Based on Adaptive Routing Algorithm

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Abstract

The lower power consumption, larger communication bandwidth, and reduced latency are advantages of optical networks over electrical communications. However, there are challenges in these networks, such as routing and connectivity issues, which result in increased network size and wastage. As networks become more complex and larger, building on-chip networks brings problems like communication costs between components and the likelihood of unpredictable failures in communication circuits. Therefore, providing an error-tolerant routing algorithm plays a crucial role in the development of on-chip network architecture. In this article, an adaptive fault-tolerant routing algorithm will be presented, whose main objective is to create the ability to handle a reasonable number of faults without disrupting the healthy nodes in the network. The simulation results of message delay in the proposed method show a gradient norm equal to 1.1691E-5 and μ=1E-8 for epoch=280, demonstrating its capability to reduce delay in the network. A very slight change in message delay in evaluating the proposed method also indicates the acceptability of the proposed method. Moreover, the presence of a gradient of 1.527E-3 and μ=1E-7 for epoch=350 in the energy consumption value indicates a reduction in energy consumption compared to conventional methods in existing references, although the proposed system may incur additional overhead compared to some previous methods.

Keywords: Network-on-Chip, Adaptive Routing Algorithm, Fault-Tolerant Algorithm, Congestion-Aware Dynamic Routing.

Highlights

- Introducing an adaptive fault-tolerant routing algorithm in interconnection networks with torus topology.
- Enabling the network to handle a significant number of faults without disrupting the healthy nodes.
- Interact with a reasonable number of faults without the need to discard healthy nodes.
- Reduction in message delay, energy consumption, and network cost compared to conventional methods.

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1. Introduction

With the advent of large-scale integrated circuit manufacturing and technological advancements, network-based systems are unable to optimally manage information resources (including processors, memories, DSPs, etc.). Thus, the concept of Networks on Chip (NoC) was introduced to improve communication between network components [1]. Moreover, designing new low-power structures, including new optical technologies and new transistors like carbon nanotube field-effect transistors, has become a priority for designers [2, 3].

In addition to designing an appropriate architecture for the network and creating an orderly structure, the proposed routing algorithms also significantly impact the performance of NoCs. Essentially, the NoC is a new communication infrastructure for Systems on Chips (SoCs). Broadly, NoCs are used as a communication scheme in modern multi-core systems to ensure reliable communications. Consequently, effective fault-tolerant methods in NoCs are of high importance. Despite the high scalability and parallel integration provided by NoCs compared to traditional bus-based systems, an ideal solution for high-scale on-chip systems is still lacking.

As technology evolves, reliability has become one of the key challenges in NoCs. Numerous fault-tolerant algorithms in NoCs have been developed to overcome defects and ensure reliable transmission. However, the proposed routing algorithm does not place much emphasis on finding the shortest paths. Several fault-tolerant algorithms that employ methods such as dissemination states based on the farthest accessible router are reviewed in [4]. In the same reference, for fault tolerance in NoCs through routing mechanisms, a new efficient adaptive routing algorithm is proposed. This algorithm is based on weighted path selection and uses monitoring modules to observe the actual traffic on the NoC. The main objective of this algorithm is to use routing decisions to maintain system throughput under faulty conditions. In the proposed low-cost fault-tolerant routing algorithm, based on the idle/busy/faulty status of channels, port weights are calculated in real-time, and ports are ranked based on the optimal path closest to the packets. This approach enables the router to bypass congested ports and tolerate faulty ports.

To evaluate the latency and throughput of the proposed algorithm, several traffic patterns for both fault-free and faulty NoCs have been examined. The results show that low-cost routing offers higher throughput compared to other routing algorithms under various traffic patterns and error levels. Moreover, the hardware overhead is minimal, enabling the scalability of NoCs at large scales. To overcome permanent failures in packet routing and reduce failures, identifying faulty components is necessary.

Routing algorithms typically circumvent faulty regions by rerouting, so the chosen path is not always the shortest. In a two-dimensional mesh, each link has two direct neighbors (west and east or north and south) and four indirect neighbors (e.g., for north and south, these are northwest, northeast, southwest, and southeast). A link has a distance perimeter that includes all paths leading to or passing through it. Additionally, a fault-tolerant routing algorithm must be able to guide packets through a loop-free path around the problematic area to their destination. Deterministic and adaptive routing algorithms, path selection methods, and path detection methods based on the number of errors are significant [4-6].

A key characteristic of on-chip in multi-core systems is reliable communication. The NoC design must demonstrate this reliability. Since submicron-scale semiconductor technology and gigahertz frequency are being implemented, they are highly susceptible to failures. As a result, the reliability of NoCs is facing more stress [7, 8]. Re iability means that after examining loops, costs, and faulty and unusable paths if one path is replaced by another and l an error occurs in the new path, will the packet still reach its destination?

2. Innovation and contributions

In this paper, various methods are used to examine routing algorithms, including hybrid algorithms, neighbor routing, traffic-aware algorithms, dynamic payload routing, table-based routing, congestion-aware routing algorithms, and fault-tolerant dynamic routing. Ultimately, assuming centralized network error information, a pseudo-code for the adaptive routing algorithm is written. Then, with the assumption of an 8x8 network, the fault-tolerant static error routing algorithm in mesh topology interconnection networks is introduced in the presence of proposed convex and concave error patterns. The simulation results demonstrate the innovation of the proposed method, showing that it can handle a reasonable number of errors without deactivating healthy nodes. It achieves high performance using adaptive routing and only four virtual channels.

Among the innovations of this paper, the following can be stated:

i- Introducing an adaptive fault-tolerant routing algorithm in interconnection networks with torus topology, while considering stuck-at and bridging fault patterns. The main objective is to enable the network to handle a significant number of faults without disrupting the healthy nodes, thus creating the ability to interact with an acceptable number of faults.

ii- The proposed method can interact with a reasonable number of faults without the need to discard healthy nodes and still achieve high efficiency using adaptive routing with only 4 virtual channels.

iii- The acceptability of the proposed method is due to its reduction in message delay on the network, energy consumption, and network cost compared to conventional methods.

3. Materials and Methods

In this article, inspired by algorithms introduced in previous works, an adaptive algorithm for message routing in Networks on Chip (NoC) is introduced. Since we aim to achieve higher speeds without causing confusion in the algorithm, a semi-adaptive nature is considered. This algorithm, similar to the mentioned algorithms, attempts to increase speed and reduce delay by modifying the X-Y algorithm. The proposed algorithm is suitable for routing packets in mesh and torus topologies. For routing, this algorithm divides packets into two categories: some packets are routed deterministically according to the X-Y algorithm, and the rest are routed dynamically.

4. Results and Discussion

The simulation results have been examined based on the average message delay and the average power consumption of the network for both convex and concave patterns. The results indicate that the proposed method has a gradient or maximum rate of change

equal to 1.1691E-5, an expected mean of 1E-8, and a validation value of 0 for epotch=280 in terms of message delay. The very slight change in message delay in evaluating the proposed method, given the approximate state and results from different production methods (in both approximate and optimal states), indicates the acceptability of the proposed method. Additionally, the energy consumed in the proposed method has a gradient or maximum rate of change equal to 1.527E-3, an expected mean of 1E-7, and a validation value of 0 for epotch=350. These results demonstrate the acceptability of the method in terms of energy consumption compared to conventional methods in other references.

5. Conclusion

In this article, a fault-tolerant static error routing algorithm for interconnection networks with a mesh topology and in the presence of convex and concave error patterns has been designed and simulated. The proposed algorithm can support various static error patterns. The innovation of the presented method lies in its ability to handle a reasonable number of errors without deactivating healthy nodes, while still providing high performance through adaptive routing using only four virtual channels, thereby maintaining minimal network cost despite potentially increasing system overhead. As a continuation of the current work, developing fault-tolerant routing algorithms for dynamic errors can be considered noteworthy, as they can lead to a reduction in the fitness factor (including the product of delay, energy consumption, and system overhead).

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Appendix

Table 1. Coordinates of various combinations for evaluating the proposed method

Occupancy pattern	coordinates of failure points
U-Shape	(2،2) ،(2،3) ،(2،4) ،(3،4) ،(4،4) ،(4،2) ،(4،3) ،(4،4)
L-Shape	(2،1) ،(2،2) ،(2،3) ،(2،4) ،(3،4) ،(4،4) ،(5،4)
H-Shape	(2،2) ،(2،3) ،(2،4) ،(3،4) ،(4،4) ،(5،4)
T-Shape	(2،4) ،(3،4) ،(44،4) ،(3،4) ،(4،4) ،(5،4)
±Shape	(3،1) ،(4،1) ،(4،2) ،(4،3) ،(4،4)
Random	(2،1) ،(2،4) ،(5،4) ،(1،5) ،(4،5) ،(6،6) ،(5،3) ،(5،2)

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