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Research Article

# Low-Power and Reliable Approximate Subtractors for Image Processing Applications

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**Abstract**

In this paper, two new approximate subtractors are presented. The proposed circuits are implemented based on gate diffusion input (GDI) and dynamic threshold (DT) techniques and are named Proposed-1 and Proposed-2. The Proposed-1 subtractor has 10 transistors, while Proposed-2 has 12 transistors. Subtractors are implemented by 32 nm carbon nanotube field effect transistor (CNTFET) technology. Various studies have shown the high efficiency and performance of the circuits in different conditions without reducing their output voltage, which is caused by the use of DT in their implementation. The proposed circuits use XOR and NOT gates, which have 4 out of 8 error states. The presented subtractors can be implemented in an unsigned non-recovery divider with different structures including vertical, horizontal, square, and triangular, and finally, they can be used in image processing applications to detect the difference between two medical or standard images. The simulation results show the better performance of the proposed circuits, Proposed-1 and Proposed-2 save PDP of 88.36% and 83.25%, respectively.

**Keywords**: Approximate Computing, Subtractor, GDI technique, CNTFET

**Highlights**

- Using approximate computing and GDI techniques to reduce power consumption
- Integration of DT technique and CNTFET technology to solve problems of GDI gates
- Design of low-power and small-area approximate subtractors due to the use of only 10 and 12 transistors

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## 1. Introduction

Approximate computing (AC) is an emerging technique that can be used to design low-power circuits and systems. For many proposed approximate computing circuits, it is important to understand a design or approximation method. The properties of full adders (FAs), multipliers, and approximate dividers have been optimized for better performance. Approximate calculations are mainly suitable for arithmetic circuits such as addition, subtraction, multiplication, and division [1]. Compared to addition and multiplication, subtraction and division have received less attention [2]. Computational circuits can be evaluated in image processing, resolution enhancement, compression, and multiplication. In addition, circuits in image processing can be used as a fault-tolerant program [3-4]. The complete subtractor circuit (FS) performs the subtraction operation of three inputs and produces two outputs. The inputs of the circuit are X, Y, $B_{in}$, and D, where D represents the difference between X and Y, and $B_{in}$ is the borrowed bit. The outputs of the circuits are the difference and $B_{out}$.

The most important application of the subtractor is in the design of dividers, and dividers are used in image processing for pixel division, change detection, and background removal [3, 4]. In [5], several approximate subtractor schemes have been designed to replace exact subtractors in low-power recovery and non-recovery dividers. A low-power regenerative divider was designed using an approximate cell [6]. To solve some of the main problems of accurate subtractor circuits, designers have designed approximate circuits. In performing a subtraction, $B_{out's}$ accuracy is generally as important as D. The delay can be reduced by combining D and $B_{out}$. The replacement depth d is to indicate the number of AXSCs replaced by EXSCs. Of course, the higher the approximate bit depth in a cascading structure, the higher the error probability. Subtractor cells are presented in [7], which replace the exact subtractor cell in the divider, which reduces the energy. The combined approximate divider is designed by combining an approximate logarithmic divider with a recovery divider [8]. This paper introduces a new 4:2 approximation compressor with 12 transistors. Implementation of this compressor using 16 nm carbon nanotube field effect transistor (CNTFET) technology results in minimum area [9]. FAs and compressors are the cores of ICs such as multipliers, subtractors, and digital filters, and are known for their high power consumption [10,11]. In this article, two new approximate subtractors are presented and analyzed.

The proposed designs are based on the Gate Diffusion Input (GDI) technique along with the Dynamic Threshold (DT) technique using 32nm carbon nanotube field effect transistors (CNTFETs) technology. These subtractors form the main dividing cells that are used in image processing. The proposed designs perform better in terms of power, delay, and Power Delay Product (PDP) by performing Monte Carlo and fanout simulations. In this paper, nanoscale approximate computing circuits are designed for change detection applications.

The organization of the paper is as follows: Section 2 provides full details about the proposed circuits. The simulation results are presented in section 3. And finally, section 4 is the conclusion of the article.

## 2. Innovation and contributions

Among the innovations of this paper, the following can be stated:

In this article, two new approximate subtractors are presented and analyzed. The purpose of the proposed circuit design is to reduce the power, and delay and increase the speed of the subtractor circuits. The proposed designs are based on the Gate Diffusion Input (GDI) technique along with the Dynamic Threshold (DT) technique using 32nm carbon nanotube field effect transistors (CNTFETs) technology. The presented subtractors can be implemented in an unsigned divider with different structures, such as vertical, horizontal, square, and triangular, and finally, they can be used in image processing programs. It is used to distinguish between two medical or non-medical images. The standard images of the simulation results show the better performance of the proposed circuits, proposed circuit 1 and proposed circuit 2, saving 88.36% and 83.25% in PDP, respectively.

## 3. Materials and Methods

In this article, a compact model compatible with SPICE 32 nm is used [15]. Also, Synopsys HSPICE-H-2013.03-SP2 64-BIT tool with CNFETs Verilog-A Model v. 2.1.1 Stanford University is used for simulation. Technology simulation parameters are according to [15]. For constant simulation conditions, the chirality vector and tube are set as (0, 38) and 10 for each transistor, respectively. In this case, DCNT = 2.97 nm, and $V_{th}$ is equal to 0.144 V.

## 4. Results and Discussion

The average power consumption is calculated from 0.01 nanosecond to two periods under the operating frequency of 500 MHz for both the Monte Carlo Method (MCM) and load capability. Using MCM with 100 executions, which are very important parameters in the physical structure of CNTFETs, they are used to check the stability of circuits against possible manufacturing failures and reveal the changes of tubes and stages of transistors [15]. In this regard, the number of tubes is considered to be 20 with variations of ± 10, while the steps of the screws are determined to be 16 nm with variations of ± 6 nm. The Proposed-1 with power values of 0.102, 0.101, and 0.1 microwatts as maximum, minimum, and average, and the Proposed-2 with power values of 0.1244 microwatts, 0.1243 microwatts and 0.124 microwatts as maximum, minimum and average, respectively, have a significant difference with AXSC2. In contrast, AXS1-AXS3 exhibits high power consumption due to the use of multiple transistors, resulting in a large number of internal nodes in DGC cells. According to the simulation results, the AXSC1 circuit has the highest delay due to its structure. Because the two gates that produce the outputs are applied to the necessary signals produced by the XOR gate.

In terms of PDP and Power-Delay-Area Product (PDAP), the proposed designs have significant differences compared to other circuits, especially AXSC2, which is their closest competitor. The difference in PDAP value of the Proposed-1 compared to AXSC2 is about 43.72%, even though it has two more transistors than AXSC2. The obtained results in terms of standard deviation of power, delay, and PDP confirm the efficiency of the proposed designs. The PDP value of the first proposed circuit is 1.68, which shows the better performance of this circuit compared to other circuits. AXSC2, which has the closest results to the proposed designs in terms of simulation results, has a higher energy consumption of about 43.24% compared to the Proposed-1. For PDAP, the same conditions

have been obtained during the FO because the mentioned designs have the same area. Normalized Mean-Error-Distance (NMED) versus PDP the Proposed-1 and the Proposed-2 have the lowest values of PDP and NMED, which are suitable for high sensitivity applications. Also, the proposed circuits have the best Power-Delay-Area Product (PDAP).

## 5. Conclusion

In this article, two new approximate subtractors are presented and analyzed. The proposed designs are based on the Gate Diffusion Input (GDI) technique along with the Dynamic Threshold (DT) technique using 32 nm Carbon Nanotube Field Effect Transistors (CNTFETs) technology. These subtractors form the main dividing cells that are used in image processing. In this article, two new approximate subtractors are presented and analyzed. The proposed designs have 4 errors with very low complexity. The simulation of changes including Monte Carlo and fanout changes has been done and the results confirm the correctness of the mathematical relationships of power and delay and Power-Delay Product (PDP). In terms of saving in the average PDP, Proposed-1 and Proposed-2 have better performance. Different studies are compared with the presented designs and the effectiveness of the proposed designs is confirmed in different conditions without reducing the output voltage, which is due to the use of DT in their implementation.

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## Appendix

Table 1. Comparison of approximate subtractors

| Name | Difference (D) | Borrow ($B_{out}$) |
|---|---|---|
| AXSC1 [6] | $(X \oplus Y) \oplus B_{in}$ | $\overline{(X \oplus Y)}.B_{in} + \bar{X}Y$ |
| AXSC2 [6] | $X \oplus Y \oplus B_{in}$ | $D \ or \ B_{out}$ |
| AXSC3 [6] | $B_{out}$ | $\overline{(X \oplus Y)}.B_{in} + \bar{X}Y$ |
| AXS1 [12] | $\bar{B}_{in}(X + Y) + XY$ | $Y$ |
| AXS2 [12] | $B_{in}(X + \bar{Y}) + X\bar{Y}$ | $B_{in}$ |
| AXS3 [12] | $B_{in}(X + Y) + XY$ | $\bar{X}$ |
| ICS1 [3] | $B_{out}$ | $\bar{X} + YB_{in}$ |
| ICS2 [3] | $B_{out}$ | $Y + \bar{X}B_{in}$ |
| ICS3 [3] | $B_{out}$ | $B_{in} + \bar{X}Y$ |
| Apps [13] | $X \oplus Y$ | $B_{in}\overline{(X \oplus Y)} + Y(X \oplus Y)$ |
| SAPSC1 [14] | $B_{out} + X\overline{YB}_{in}$ | $\bar{X}(Y + B_{in}) + YB_{in}$ |
| SAPSC2 [14] | $B_{out}$ | $\bar{X}(Y + B_{in}) + YB_{in}$ |
| SAPSC3 [14] | $B_{out}$ | $\bar{X} + YB_{in}$ |
| SAPSC4 [14] | $X + (Y \oplus B_{in})$ | $Y$ |
| SAPSC5 [14] | $\bar{X} + YB_{in}$ | $Y$ |
| SAPSC6 [14] | $X + Y$ | $Y$ |

Table 2. The truth table of approximate subtractors.

| | EXACT | AXSC1 | AXSC2 | AXSC3 | ICS1 | ICS2 | ICS3 | Apps | AXS1 | AXS2 | *AXS3* | SAPSC3 | SAPSC4 | Proposed-1 | Proposed-2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $XYB_{in}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D_{iff}$ | $B_{out}D$ | $B_{out}D$ | $B_{out}D$ | $B_{out}D$ | $B_{out}D$ |
| 000 | 00 | 00 | 00 | 00 | 11 | 00 | 00 | 00 | 00 | 00 | 11 | 11 | 00 | 11 | 11 |
| 001 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 10 | 00 | 11 | 11 | 11 | 01 | 11 | 11 |
| 010 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 00 | 11 | 11 | 11 | 11 | 11 |
| 011 | 10 | 11 | 00 | 11 | 10 | 10 | 10 | 11 | 10 | 10 | 10 | 11 | 10 | 11 | 11 |
| 100 | 01 | 01 | 11 | 00 | 01 | 01 | 01 | 01 | 01 | 01 | 01 | 00 | 01 | 10 | 10 |
| 101 | 00 | 01 | 00 | 00 | 00 | 01 | 11 | 01 | 00 | 11 | 00 | 00 | 01 | 10 | 11 |
| 110 | 00 | 00 | 00 | 00 | 00 | 11 | 00 | 00 | 11 | 00 | 00 | 00 | 11 | 01 | 01 |
| 111 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 10 | 11 | 11 | 00 | 11 | 11 | 11 | 11 |
| ER | ----- | 0.25 | 0.25 | 0.25 | .125 | .125 | .125 | 0.5 | 0.25 | 0.25 | 0.25 | 0.375 | 0.375 | .5 | .5 |
| NMED | ----- | 0.0833 | 0.0833 | 0.0833 | 0.0416 | 0.0416 | 0.0416 | 0.1666 | 0.0833 | 0.0833 | 0.0833 | 0.125 | 0.125 | 0.1666 | .1666 |
| MRED | ----- | 0.1875 | 0.375 | 0.1875 | 0.375 | 0.375 | 0.375 | 0.2708 | 0.25 | 0.25 | 0.25 | 0.3125 | 0.3333 | .4375 | .4375 |

* blue numbers are the worst results

Table 3. Specification comparison between approximate subtractors

| Name | Tran. Count | Nu. of Errors | Technique | Tran. Level | Gate Level (VHDL) | Using Inverter at In/Out | Total Number of Inverter at In/Out |
|---|---|---|---|---|---|---|---|
| AXSC1 [6] | 8 | 2 | TG | YES | NO | Yes/No | 1 |
| AXSC2 [6] | 8 | 2 | TG | YES | NO | Yes/No | 2 |
| AXSC3 [6] | 12 | 2 | TG | YES | NO | Yes/No | 2 |
| AXS1 [9] | 14 | 2 | CMOS | YES | NO | Yes/Yes | 2 |
| AXS2 [9] | 14 | 2 | CMOS | YES | NO | Yes/Yes | 2 |
| AXS3 [9] | 12 | 2 | CMOS | YES | NO | Yes/Yes | 2 |
| ICS1 [3] | 28 | 1 | CMOS | YES | NO | Yes/Yes | 3 |
| ICS2 [3] | 28 | 1 | CMOS | YES | NO | Yes/Yes | 3 |
| ICS3 [3] | 28 | 1 | CMOS | YES | NO | Yes/Yes | 3 |
| Apps[10] | 22 | 4 | CMOS | NO | YES | Yes/Yes | 3 |
| SAPSC1 [11] | 44 | 1 | CMOS | NO | YES | Yes/Yes | 5 |
| SAPSC2 [11] | 26 | 2 | CMOS | NO | YES | Yes/Yes | 2 |
| SAPSC3 [11] | 14 | 3 | CMOS | NO | YES | Yes/Yes | 2 |
| SAPSC4 [11] | 18 | 3 | CMOS | NO | YES | Yes/Yes | 3 |
| SAPSC5 [11] | 14 | 5 | CMOS | NO | YES | Yes/Yes | 2 |
| SAPSC6 [11 | 6 (No $B_{in}$) | 4 | CMOS | NO | YES | No/Yes | 1 |
| Proposed-1 | 10 | 4 | GDI | Yes | No | Yes/No | 2 |
| Proposed-2 | 12 | 4 | GDI | Yes | No | Yes/No | 2 |

Table 4. The values of power, delay, PDP, and PDAP of the proposed reference circuits.

| Name | Power | Delay | PDP | Tran. Count | PDAP |
|---|---|---|---|---|---|
| AXSC1 [6] | 70.371 | 0.6332 | 36.438 | 8 | 291.5 |
| AXSC2 [6] | 66.787 | 0.3162 | 21.118 | 8 | 168.9 |
| AXSC3 [6] | 69.412 | 0.3154 | 21.892 | 12 | 262.7 |
| AXS1 [9] | 115.31 | 0.4271 | 49.248 | 14 | 289.4 |
| AXS2 [9] | 97.912 | 0.5147 | 50.395 | 12 | 604.7 |
| AXS [9] | 62.296 | 0.3705 | 23.080 | 28 | 646.2 |
| ICS1 [3] | 130.21 | 0.358 | 46.61 | 28 | 1304.8 |
| ICS2 [3] | 68.351 | 0.282 | 19.13 | 28 | 555.6 |
| ICS3 [3] | 67.692 | 0.252 | 16.923 | 28 | 473.8 |
| Apps [10] | 93.26 | 0.3075 | 28.677 | 22 | 630.7 |
| SAPSC3 [11] | 71.05 | 0.335 | 23.80 | 14 | 333.2 |
| SAPSC4 [11] | 75.69 | 0.45 | 34.06 | 18 | 613 |
| Proposed-1 | 87.65 | 0.122 | 10.51 | 10 | 105.1 |
| Proposed-2 | 91.02. | 0.14 | 12.74 | 12 | 152.8 |

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