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Research Article

A Multiplier-Less Discrete Cosine Transform Architecture Using a Majority Logic-Based Approximate Full Adder

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Abstract

This paper proposes a new approximate full adder (FA) based on the majority logic (ML) concept. The fundamental structure of the ML concept is a 3-input majority voter and is widely utilized in digital arithmetic cells. The ML-based proposed FA works at low power, small delay, and low power-delay-product (PDP). The carbon nanotube field-effect transistor (CNTFET) technology lowers the FA power, while the gate diffusion input (GDI) technique is used as the main technique. The swing issue of the GDI technique is resolved by the dynamic threshold (DT) technique. Compared with its exact circuit, the proposed FA saves 2 majority gates, 3 inverters, and a 4.02 ns delay. In the proposed FA, the PDP is improved by 53.73%. The product of the PDP and the normalized mean error distance (NMED) is called PDPE, and in the presented FA, it is reduced by 9.50%. Moreover, the proposed FA is embedded into a multiplier-less discrete cosine transform (DCT) design, which is an appropriate circuit for very large-scale integration (VLSI) systems. The 8-input DCT architecture consumed 2.2321 mW of power for each DCT operation. Also, the circuit has better performance in terms of PDP-area-product (PDAP). The results of DCT implementations confirm the efficiency of the FA.

Keywords: Approximate Full Adder, Majority Logic, Discrete Cosine Transform (DCT), Multiplier-Less DCT.

Highlights

- A new approximate full adder (FA) based on the majority logic (ML) concept is proposed.
- By reducing the number of majority gates and removing the inverter, the power, and delay of the proposed circuit is reduced.
- The carbon nanotube field-effect transistor (CNTFET) technology and gate diffusion input (GDI) technique are used to implement the proposed circuit.
- To compensate for the output voltages the dynamic threshold (DT) technique is used.
- The proposed FA is embedded into a discrete cosine transform (DCT) structure.

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1. Introduction

In this century, low-power, fast, and small-area devices are part of life [1,2]. Arithmetic circuits are the main parts of digital systems [3]. Over the past two decades, semiconductor-based factories have experienced excellent enhancements in integrated technology regarding high-speed, low-power, and small-area techniques [4]. Increasing the circuit density by complementary metal oxide semiconductor technology (CMOS) increases power consumption because, in this technology, two pull-up and pull-down networks are used, which increases the number of transistors. As a solution, using approximate computing can be a suitable alternative for error-resilient applications. Approximate-based arithmetic cells use a lower number of logic gates which consequently can reduce power consumption at the expense of accuracy. However, the approximate CMOS circuits are not immediately applicable to many new technologies [5], because the underlying logic structures of these devices are very different.

Modern systems are very dependent on ML[1] which is quite variously from traditional Boolean logic. A majority gate carries on a logical function with multiple inputs, such as A, B, and C and the output is F [6]. Research on the design of approximate ML-based circuits has been performed quite recently. In [6,7] the authors offered an approximate 1-bit full adder (FA) based on ML.

The FA serves as a key element in sophisticated arithmetic cells to carry out calculations such as addition, multiplication, and division [8-11]. These FAs are embedded in traditional DCT[2] structures to outperform sophisticated audio and image compression logic operations in digital signal processing [12]. Therefore, many researchers have proposed various DCT structures with high simplicity, low power consumption, and fast and high throughput [13]. The DCT designs are different in terms of logic style gesture, which impact different design parameters including power, transistor count, and speed [14,15]. The ordinary circuit relies upon the inversion levels, transistors' counts in series, transistor dimensions, and the way these components are wired as one of the most important factors when designing is under consideration [16]. The present DCT architectures are applied to the usage of numerous varieties of adder and multiplication units, which provide higher power consumption and lower speed. The proposed approximate-based FA is implemented in a DCT structure in a pipelined fashion multiplier-less [17]. Recently proposed FAs functioning as a block of the DCT implementations, along with a half-adder, half-subtractor, D flip-flop, and 1-bit left shift circuit.

This article proposes an approximate FA based on ML. The 32 nm carbon nanotube field-effect transistors (CNTFET) technology is used to demonstrate the feasibility of the FA and DCT. The proposed designs are low-power, high-speed, and small-area, and the DT[3] the technique causes full-swing outputs.

The remainder of this article is organized as subsequent details. Section 2 describes the approximate FA design (based on ML) and related work on the architecture of the DCT. Section 3 provides the construction of the suggested ML-based inaccurate FA. Simulation outcomes and comprehensive investigations can be found in Section 4. Section 5 concludes the paper.

2. Innovation and contributions

This paper proposes a new approximate full adder (FA) based on the majority logic (ML) concept.

Among the innovations of this paper, the following can be stated:

The purpose of the proposed circuit design is to reduce the power, delay, and increase the speed of the approximate full adder circuit, which was made possible by reducing the number of majority gates (compared to the Exact full adder and other references) to 1 gate and removing the inverter.

The carbon nanotube field-effect transistor (CNTFET) technology lowers the FA power, while the gate diffusion input (GDI) technique is used as the main technique. The swing issue of the GDI technique is resolved by the dynamic threshold (DT) technique. the proposed FA is embedded into a multiplier-less discrete cosine transform (DCT) design, which is an appropriate circuit for very large-scale integration (VLSI) systems and digital signal processors (DSPs). The 8-input DCT architecture requires a total of 1310 transistors and consumes 2.2321 mW of power for each successful DCT operation.

3. Materials and Methods

The proposed approximate circuit is designed at the transistor level and simulated by HSPICE 2013 software and SPICE-compatible compact model 32 nm Stanford University CNTFET technology. The frequency is considered 500 MHz, V_{DD} is 0.9 V, and the temperature is 27 ºC. the gate diffusion input (GDI) technique is used as the main technique. The swing issue of the GDI technique is resolved by the dynamic threshold (DT) technique.

4. Results and Discussion

The parameters of MV[4], INV[5], NMED, delay, power, and PDP[6] between the exact adders [18], AFA1 [7], AFA2 [6], PPA1, PPA2 [21], and the proposed AFA are compared and the results are provided in Table 3. Compared with the exact adder, the proposed circuit saves 2 majority gates, 3 inverters, and a 4.02 ns delay. The proposed design improves the PDP of the circuit by 53.73% compared with AFA1 [7]. Also, the PDPE[7] is used as a combined measurement of an approximate FA. As shown in Table 3, the proposed circuit reduces the PDPE by 9.50% compared with AFA2, which confirms the advantages of the proposed circuit in terms of overall performance.

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[1] Majority logic
[2] Discrete Cosine Transform
[3] Dynamic threshold
[4] Majority gate count (Mjority Voter)
[5] Inverter count
[6] Power Delay Product
[7] Product of the PDP and the NMED

To balance the hardware criteria and application level, a figure of merit (FoM) is established to involve both circuit and accuracy parameters. In Table 3, the FoM results of the proposed AFA and references are considered. The proposed AFA shows the best performance, while the AFA2 has the worst performance.
The proposed AFA is embedded as a basic component in a multiplier-less DCT [17]. Compared to counterparts' architectures described by other scholars, only 24 adder/subtractors are used. By reducing the number of adders and removing extra multiplexers and multipliers, power consumption and delay are significantly reduced. Additionally, the proposed AFA is applicable in DCTs with longer lengths [19,20]. There are many intermediate stages in the constructed architecture, so, higher voltages are required to drive the elements of delay and shift circuitry. Table 5 compares power, transistor count, delay, PDP, PDP and area product (PDAP), and average current. The proposed cell outperformed the other structures regarding power, area, and average current. The precise circuit and construction of the AFA1 draw maximum power and current with a large area and a high number of transistors. Each input was subjected to a discrete cosine transform to produce a transformed output. The 8-input DCT architecture design required a total of 1310 transistors and consumed 2.2321 mW of power for each successful DCT operation. Also, the circuit has better performance in terms of PDAP.

5. Conclusion

In this study, a new approximate full adder (AFA) with a small number of transistors, low power, and low delay is suggested. The proposed cell is designed based on considerable specifications of the majority logic. For better comparison, other well-known FAs are simulated to assess the functionality of the proposed design compared to other FAs regarding power, delay, and current. The suggested block is improved regarding its drivability and increased operational speed. The area and power consumption of the proposed design are also superior to other FA designs with high gate counts. Moreover, the proposed FA is used in the DCT architecture to further reduce power consumption and delay for a more optimized hardware implementation.

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Appendix

Table 1. The truth table of the proposed AFA.

ABC_{in}	Exact FA [20]	AFA1 [7]	AFA2 [6]	PPA1 [27]	PPA2 [27]	Proposed AFA
	C_{out} -Sum	C_{out} -Sum	C_{out} -Sum	C_{out} -Sum	C_{out} -Sum	C_{out} -Sum
000	00	01	01	00	00	00
001	01	01	10	01	00	00
010	01	01	01	00	01	00
011	10	10	10	11	10	10
100	01	01	01	00	01	01
101	10	10	10	11	10	11
110	10	10	01	10	11	11
111	11	10	11	11	11	11
ER	-	0.5	0.25	0.5	0.25	0.5
NMED	-	0.166	0.083	0.166	0.083	0.166

Abbreviations: ER, error rate; NMED, normalized mean error distance.

Table 2. The considered parameters for CNTFET technology.

Parameter	Value	Definition
L_{ch}	32 nm	Physical Channel Length
L_{geff}	100 nm	Mean Free Path: Intrinsic CNT
L_{ss}	32 nm	Source Side Extension Regions
L_{dd}	32 nm	Length of Doped CNT Drain
K_{gate}	16	Gate Dielectric Constant
T_{ox}	4 nm	Oxide Thickness
C_{sub}	40 pF/m	Coupling Capacitance between Channel and Substrate
E_{fi}	0.6 eV	The Fermi Level of the Doped S/D Tube
Pitch	5 nm	The Distance Between Tube Centers
Chirality Vector	(38,0)	Arrangement of Carbon Atoms Angle
Tubes	10	For each Transistor

Table 3. Performance comparison of different approximate FAs.

Frequency=500 MHz, Temperature=27 °C, V_{DD}=0.9 V. CNTFET 32 nm Technology.								
Adder Type	MV	INV	Delay (ns)	Power (µw)	PDP (fJ)	NMED	PDP*NMD	FoM
Exact [20]	3	**2**	7.13	5.36	38.216	-	-	-
AFA1 [7]	1	1	5.16	4.55	23.478	0.083	1.94	25.60
AFA2 [6]	1	1	5.13	4.68	24.008	0.083	1.99	26.18
PPA1 [27]	1	0	3.15	3.87	12.190	0.166	2.02	14.61
PPA2 [27]	1	1	5.15	4.67	15.150	0.083	1.99	26.22
Proposed AFA	**1**	**0**	**3.11**	**3.79**	**10.862**	**0.166**	**1.80**	**13.02**

Table 4. Simulation results against VDD variation.

Temperature=27 °C, Load Capacitance =1 fF, Frequency=500 MHz.									
	0.7 V			**0.9 V**			**1.2 V**		
Designs	**Power (µW)**	**Delay (ns)**	**PDP (fJ)**	**Power (µW)**	**Delay (ns)**	**PDP (fJ)**	**Power (µW)**	**Delay (ns)**	**PDP (fJ)**
Exact [20]	5.86	7.10	41.60	5.36	5.36	38.21	6.72	7.15	48.04
AFA1 [7]	3.09	5.14	15.88	4.55	4.55	23.47	5.47	5.18	28.33
AFA2 [6]	3.54	5.11	18.08	4.68	4.68	24.08	5.38	5.15	27.70
PPA1 [27]	3.18	3.17	10.08	3.87	3.87	12.19	5.89	3.17	18.67
PPA2 [27]	3.71	5.17	19.18	4.67	4.67	24.05	6.22	5.19	32.28
Propose AFA	**3.14**	**3.08**	**9.67**	**3.79**	**3.11**	**10.86**	**4.21**	**3.15**	**13.26**

*Bold numbers mean better results.

Table 5. Simulated results of DCT architecture by implementing the FAs.

Adder Type	Power (mW)	Delay (ns)	Area (#)	PDP (fJ)	PDAP	I_{dd} (mA)
DCT_Exact [20]	3.2467	29.30	1528	95.12831	145356.1	12.01
DCT_AFA1 [7]	2.7291	29.95	1428	81.73655	116719.8	9.77
DCT_AFA2 [6]	2.5213	29.98	1420	75.58857	107335.8	9.20
DCT_PPA1[27]	2.3512	29.40	1438	69.12528	99402.15	9.12
DCT_PPA2[27]	2.5417	29.50	1445	74.98015	108346.3	8.99
DCT_Proposed AFA	**2.2321**	**29.20**	**1310**	**65.17732**	**85382.29**	**6.78**

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