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Research Article

Design and Implementation of a 16-bit Multi-Mode Delta-Sigma Digital-to-Analog Converter with Time-Interleaved Structure, Multi-Channel, and Compensation of Non-Idealities Based on FPGA

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Abstract

In this research, a 16-bit multi-mode second-order Delta-Sigma Modulator-Digital-to-Analog Converter (DSM-DAC) with a time-interleaved (TI) structure operating at a center frequency of 4 GHz and a bandwidth of 20 MHz has been implemented using VHDL on an FPGA platform. The proposed architecture utilizes a single clock frequency for generating RF signals. The second-order DSM is reconfigurable, offering three filter modes: LP, BP at Fs/4, and HP for signal synthesis. Since the coefficients remain simple for all modes, multiplication operations can be achieved using a shifter block. To investigate the effect of duty-cycle-error (DCE) and its compensation, various error values are applied to the modulator and compensation is performed. A novel solution is proposed to overcome the DCE by adjusting the filter and unilaterally narrowing the signal passband without adding extra hardware complexity. This approach significantly enhances the SNDR and SFDR of the DSM output, even for the BP mode. Another challenge is the mismatch error in DAC cells. This error is simulated and compensated using two methods: DWA and SDEM. Simulation results in ISE demonstrate that the SNDR values for LP, BP, and HP modes are 106.10, 105.65, and 104.95 dB, respectively.

Keywords: Delta-sigma modulator, Duty-cycle-error, Error-feedback, FPGA, Mismatch, Time-interleaved.

Highlights

- A 16-bit multi-mode digital-to-analog converter with a time-interleaved structure at a frequency of 4 GHz.
- Only one clock frequency is used to generate the radio frequency signal.
- There are simple coefficients for all cases, the multiplication operation can be performed using a shifter block.
- Two dominant errors in TI-DSM-DACs (mismatch and duty-cycle-error (DCE)) have been compensated
- A new method is proposed to remove the effect of signal image in BP mode, instead of using complex circuits.

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1. Introduction

In recent years, there have been significant advancements in the design of Digital-to-Analog Converters (DACs) for wireless communication systems. The growing need for high-speed data transfer and adaptable system designs has placed a particular emphasis on software-defined radios (SDRs) [1-4].

Wireless communication standards have created radio frequency digital-to-analog converters (RF-DACs) to comply with stringent noise level specifications [3]. Nonetheless, attaining high resolution in Nyquist frequency DACs raises the complexity of both analog and digital circuits, resulting in mismatches and decreased linearity [5-7]. Various calibration and correction techniques have been suggested [8-12], but they typically demand a significant number of cells and extensive calibration time, which restricts the performance of the designs [13, 14]. This study provides a concise overview of novel DAC structures and techniques aimed at addressing the shortcomings of earlier designs.

Time-interleaved DACs (TI-DACs) remove image signals and reduce harmonics by integrating several DACs with phase shifts [15, 16]. This method enhances bandwidth and resolution, but it also presents challenges such as increased chip size and greater energy usage [3, 15, 17-19].

Methods like interleaving [17-20], digital feed-forward extrapolation [21], dynamic element matching (DEM) [22], and digital pre-distortion (DPD) [23] are employed to enhance performance and linearity. The aim of the suggested architectures is to achieve high data rates, cover a broad frequency spectrum, and simplify hardware design.

Time-interleaved delta-sigma modulator DACs (TI-DSM-DACs) have become popular in flexible radio transmitters because they enhance the speed of digital modulators for high clock rates while reducing analog complexity [20]. Additionally, their oversampling capability allows for a lower order of the analog reconstruction filter that follows the DAC [24]. As a result, they are essential in the development of modern communication standards like WiGig (IEEE 802.11ad) [25], ECMA-387 [26], Wireless HD [27], and more recently, fifth-generation (5G) wireless communications, which operate in high gigahertz frequency bands such as 28, 38, 64, and 71 GHz [28, 29].

2. Innovation and contributions

The proposed design has been developed and implemented for three specific center frequencies. For each frequency, the TI-DSM coefficients must be modified, and a filter is applied after the 4-bit TI-DSM according to the center frequency. This method successfully achieves bandwidth splitting by shifting the passband of the TI-DSM signal to both sides of the center frequency (Fs/4) without requiring additional hardware or increasing circuit complexity. The upper frequency band spans from 1000 to 1020 MHz, while the lower band ranges from 980 to 1000 MHz.

In BP mode, two distinct filters are employed for the upper and lower sub-bands. When the input signal falls within the lower sub-band, its image appears in the upper sub-band. By using a band elimination filter for the upper sub-band, this image can be eliminated. Conversely, if the input signal is in the upper sub-band, its image will be found in the lower sub-band. Thus, applying a band elimination filter to the lower sub-band effectively reduces this image. This filtering technique ensures that the signals are properly filtered and that any unwanted images are removed from their respective sub-bands. Essentially, this method requires just two filters with narrower bandwidths at the output to eliminate signal images.

3. Materials and Methods

This research is based on innovation in structural design and the presentation of a complete system model for a sigma-delta digital-to-analog converter, which will be simulated and implemented. Then, potential errors in this proposed model will be examined and simulated in the Simulink environment of MATLAB. After system simulations and ensuring the correctness of the proposed structure, the hardware of the sigma-delta modulator with a time-interleaved structure will be described in VHDL in the ISE software. This description will be optimized in terms of power consumption, performance speed, and use of hardware resources. The behavior of the circuit will also be examined in this section.

4. Results and Discussion

The SNDR values in the LP, BP, and HP modes are 62.25, 36.07, and 96.78 dB, respectively, while the SFDR values in the LP, BP, and HP modes are 61.94, 25.12, and 96.31 dB, respectively. The results indicate that the SNDR and SFDR values have experienced a significant drop due to the DCE error. The reason for this sharp decline in the BP mode is the presence of signal images in the modulator's frequency band. The SNDR values in the LP, BP, and HP modes are 56.23, 30.05, and 91.30 dB, respectively, while the SFDR values in the LP, BP, and HP modes are 55.92, 19.10, and 93.41 dB, respectively. The reason for the smaller drop in the HP mode is the significant frequency distance of the signal image from the main signal and the modulator's frequency band. In the LP mode, after compensation using the LP-FIR filter, the SNDR values for errors of 1% and 2% are 106.12 dB and 106.13 dB, respectively, while the SFDR for both error values is the same at 91.80 dB. Then, a second-order HP-FIR filter with the expression

(1-z-1)2 is considered. In the HP mode, after compensation using the HP-FIR filter, the SNDR values for errors of 1% and 2% are the same at 105.34 dB, while the SFDR values are 94.42 dB and 94.44 dB, respectively. Terminally the simulation results and the output spectrum of the DAC for a 1% error due to a mismatch of the DAC cells using the SDEM method with a second-order filter to compensate for errors of 1%, 2%, and 3% in the LP, BP, and HP modes have been shown. By comparing the results of the DWA and SDEM methods of the first and second order, it can be concluded that the compensation sorting method with a second-order filter provides the required SNDR for a 16-bit ENOB.

5. Conclusion

In this article, a second-order delta-sigma modulator (DSM) with a 16-bit multi-state structure based on Time-Interleaving (TI) was implemented in VHDL and FPGA at a frequency of 4 GHz with a bandwidth of 20 MHz. The proposed architecture uses only one clock frequency for generating radio frequency (RF) signals. The second-order delta-sigma modulator with reconfigurable capability has three modes: LP, BP at frequency Fs/4, and HP for signal synthesis. To increase the sampling frequency (Fs), a 4-channel time-interleaved (TI) structure was proposed. Each of the channels operates at a frequency of 4/Fs. Since simple coefficients are available for all modes, multiplication operations were performed using a shift block. This led to simplification in design, reduced power consumption, smaller area occupancy, and higher speed. A major challenge in designing such structures is duty cycle error (DCE), especially in the time-interleaved mode. To investigate the effect of DCE and compensate for it, various error values were applied to the modulator, and compensation was performed. In this article, a new solution was proposed to overcome the effect of DCE by adjusting the filter circuit and unilaterally shaping the passband of the signal without adding extra hardware and circuit complexity. This method significantly increased the SNDR and SFDR output values of the delta-sigma modulator, even for the BP mode, by eliminating the image effect of the signal. The use of TI-FIR filtering in compensating for DCE is effective in LP and HP modes, but it does not achieve much success in compensating DCE in BP mode. However, the proposed compensation method is highly effective in addressing DCE in BP mode, significantly improving results to the point of approaching ideal values. Since in BP mode, the SNDR after compensation using the proposed method reached approximately 95 dB, the effective number of bits (ENOB) is 15.5 bits. Another challenge that was overcome was the mismatch error of DAC cells. In this research, this error was simulated and compensated using two methods: DWA and SDEM. Simulation results in ISE showed that the signal-to-noise and distortion ratio (SNDR) values for LP, BP, and HP modes were 106.10 dB, 105.65 dB, and 104.95 dB, respectively.

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Appendix

Table 1: Final specifications of the selected system.

Parameter	Value	Parameter	Value
Sampling frequency (Fs)	4 GHz	LP filter order	2
Bandwidth (BW)	20 MHz	BP filter order	4
Oversampling rate (OSR)	100	HP filter order	2
Number of input bits	16	Internal quantizer bits	4
Interleaving channel number	4	SFDR (Fs)	> 100 dB
SNDR (Fs)	> 100 dB		

Table 2: SNDR values in dB for DCEs at 1% and 2% before and after compensation.

Modulator mode	Ideal TI-DSM	Compensation methods		DCE percentage	
				1%	2%
Low-pass	106.10	No compensation		62.25	56.23
		First-order FIR filter		100.60	96.12
		Second-order FIR filter		106.12	106.13
Band-pass	105.65	No compensation		36.07	30.05
		First-order FIR filter		36.07	30.05
		Second-order FIR filter		36.07	30.05
		Proposed method	Upper band	95.09	---
			Lower band	94.30	---
High-pass	104.95	No compensation		96.78	91.30
		First-order FIR filter		105.35	105.34
		Second-order FIR filter		104.34	105.34

Table 3: Comparison of used second-order TI-DSM in ideal case and after compensation.

Logic utilization	No compensation (Ideal)	Compensation methods	
		First-order FIR filter	Second-order FIR filter
Number of Slice Registration	76	88	92
Number of Slice LUTs	333	385	196
Number of fully used LUT-FF pairs	72	79	82
Number of bonded IOBs	24	25	25
Number of BUFG/BUFGCTRLs	2	2	2
Number of TIDSM output bits	4	5	6

Table(4): Simulation results of SNDR for different DAC error percentages with and without DWA compensation.

Modulator mode	Ideal TI-DSM	Compensation methods	DAC Cells Mismatch		
			1%	2%	3%
Low-pass	106.10	No compensation	53.53	39.99	36.36
		DWA compensation	99.85	89.23	85.76
Band-pass	105.65	No compensation	76.65	47.11	43.49
		DWA compensation	98.31	88.33	84.94
High-pass	104.95	No compensation	54.15	49.57	45.96
		DWA compensation	99.06	88.24	84.79

Table 5: SNDR values for 1%, 2%, and 3% DAC cell mismatch errors and compensation by first and second-order SDEM.

Modulator mode	Ideal TI-DSM	Compensation methods	DAC Cells Mismatch		
			1%	2%	3%
Low-pass	106.10	No compensation	53.52	39.99	36.36
		First-order SDEM	99.85	90.32	86.89
		Second-order SDEM	104.07	103.50	102.21
Band-pass	105.65	No compensation	76.65	47.11	43.49
		First-order SDEM	94.03	79.35	75.38
		Second-order SDEM	95.63	103.25	100.98
High-pass	104.95	No compensation	54.15	49.57	45.96
		First-order SDEM	85.23	74.61	71.08
		Second-order SDEM	89.60	101.68	99.75

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