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Research Article

Design of Low-Area, Low-Power and High-Speed Comparator in 65 nm FinFET Technology

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Abstract

In the present study, a new low-power and high-speed comparator circuit is designed in 65 nm fin field-effect transistor (FinFET) technology. Moreover, by properly using the capabilities of FinFET technology, the number of transistors is reduced, and subsequently, a smaller area is occupied. Replacing MOSFET transistors with FinFETs reduces the delay and power consumption of the circuit, so the overall performance is improved. The first innovation of the proposed design is that to reduce the size and power consumption, two transistors were removed and the back gates of two transistors were cross-coupled. The second innovation is the connection of back gates to other suitable points of the circuit that increase the speed of comparison. In this study, a supply voltage of 0.8 V is applied to the circuit to show that the proposed modifications with FinFET reduce the delay to 272 ps and power consumption to 6.7 µW.

Keywords: Comparator, FinFET, High-speed, Low-area, Low-power

Highlights

- New low-power and high-speed comparator circuit designed in 65 nm fin field-effect transistor (FinFET).
- Reduction of the number of transistors and subsequently, smaller area.
- Reduction of the delay and power consumption of the circuit by replacing MOSFETs with FinFETs.

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1- INTRODUCTION

The increasing need for low-power, high-speed and minimum area circuits such as analog-to-digital (A/D) in today's technology makes it easier to move towards dynamic comparator designs with maximum speed and low power consumption [1,2]. One of the most important blocks in ADCs is the comparator whose speed and power consumption are very influential in these circuits [3,4,5].
A fin field-effect transistor (FinFET) is a multi-gate device, a MOSFET built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double or even multi gate structure [6,7]. The FinFET devices have significantly faster switching times and higher current density than planar CMOS technology [8,9].
So far, fin field-effect transistor (FinFET) technology has been used in various researchhes [10,11].
A p-type Inverted-T FinFET has been optimally structured in [12], in which, FinFET has a higher layout efficiency and can thus provide larger drain current under the same dimension as that of a SOI FinFET by securing the extended channels of ultrathin body on the field region.
A FinFET transistor-based domino technique DNDFTDL is designed for low-power, high-speed and improved noise performance in [13], which the concept of current division is explored below the evaluation network for enhancement of performance parameters and simulations are carried out for 32-nm complementary CMOS and FinFET node using HSPICE for 2-, 4-, 8- and 16-input OR gates with a DC supply voltage of 0.9V.
Therefore, in this paper, after studying a few conventional circuits, a new high-speed and low-power comparator is designed and simulated in 65 nm FinFET technology. A comparison between the proposed comparator and previous works indicates the acceptability of the design.
In the second section, conventional comparators are mentioned. The third section, describes the fin field-effect transistor technology. In the fourth section, the results and their discussion are stated and in the last section, the conclusion is given.

2- CONVENTIONAL COMPARATORS

The output of an ideal comparator is shown in Figure 1. The output is “0” if the input signal is less than the reference voltage and is “1” if the input is greater than the reference voltage.

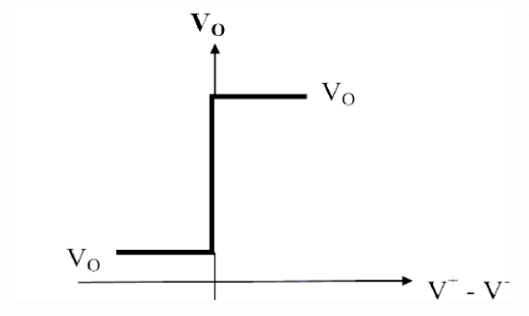

Figure 1. Output of an ideal comparator

Figure 2 shows a conventional comparator circuit that was proposed in [14]. In this figure, M1 and M2 are the input transistors and their source can be connected to GND through Mtail whenever CLK is ON, so the dynamic circuit performs the comparison. If INN<INP, then M2 turns on and M1 turns off. In this case, the current flow through M2, M4, and M6 increases and vice versa.
The circuit shown in Figure 3, is the next generation of the circuit shown in Figure 2. If INN<INP, then the drain current of M2 is more than that of M1, and the voltage of fn drops to zero. Moreover, since MR2 goes to zero, while MR1 is turned on and goes to one; the voltage of OUTN and OUTP go to zero and one. Consequently, M8 is turned on and connects OUTP to VDD, while OUTN is connected to GND through the M9.
As shown in Figure 4, MC1 and MC2 are respectively, in parallel with M3 and M4, and cross-coupled. This can help the voltage of fp to reach VDD faster, and similarly, the voltage of fn to GND. Since M1 is connected to fp, it prevents fp from going to VDD; the source of M1 is connected to GND through Mtail, which leads to a delay. Therefore, MSW1 is added to the circuit to disconnect M1 from GND while fp increases. Similarly, MSW2 is added to disconnect M2 from GND while fn increases to VDD [10]. In table 1, the results of conventional comparator circuits are shown.

TABLE 1. Result of the conventional comparators

Structure	Conventional Dynamic Comparator 1	Double-tail Dynamic Comparator 2	Double-tail Dynamic Comparator 3
Technology CMOS	180 nm	180 nm	180 nm
Supply voltage (V)	0.8	0.8	0.8
Delay/Log v_{in} (pS/dec.)	940	358	294
Energy per conversion (pJ)	0.3	0.27	0.24 (Without M_{sw1} & M_{sw2}: 0.256)
Estimated area (μm^2)	16*16	28*12	28*14

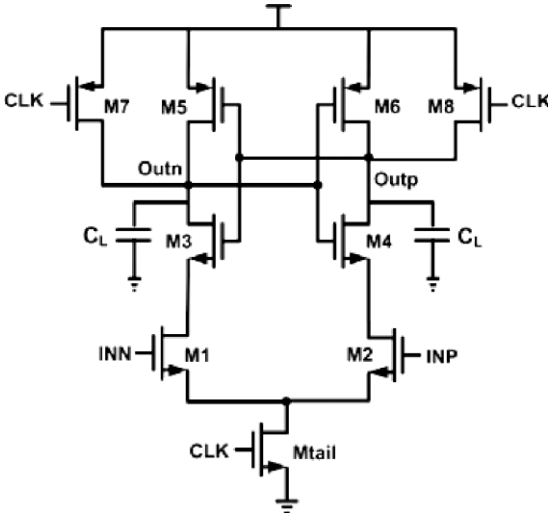

Figure 2. First conventional comparator [10]

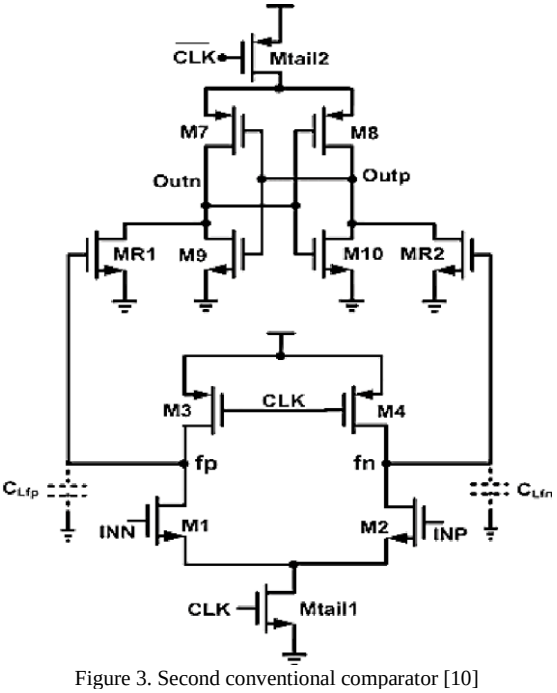

Figure 3. Second conventional comparator [10]

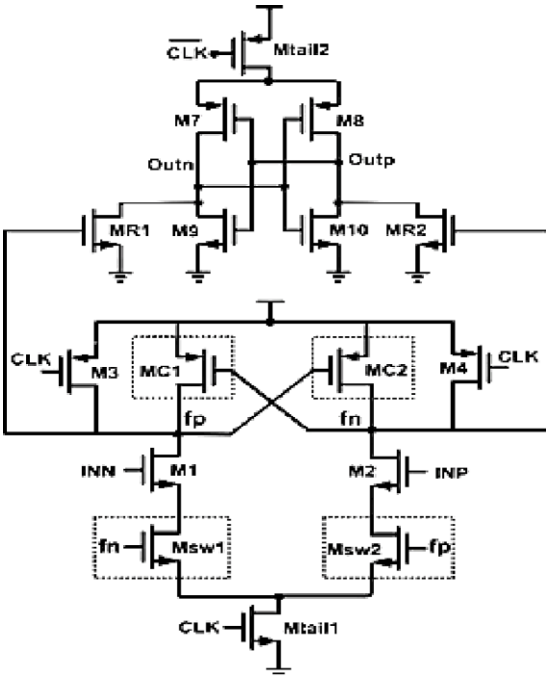

Figure 4. Third conventional comparator [10]

3- FIN FIELD-EFFECT TRANSISTOR

FinFETs are a very promising alternative to bulk MOS transistors in the nanoscale [15]. A FinFET has two gates that make it more efficient. This can reduce leakage current and short channel effect [16,17]. The main goal in very large-scale integration (VLSI) designs is to achieve the best possible efficiency with low power consumption [18,19]. This goal can easily be achieved by substituting FinFET circuits for CMOS blocks such as 6T-SRAM [20,21], 8T-SRAM [22,23] and 9-T SRAM [24,25]. Analysis of performance metric, process variation, and temperature effect Nanoscale FinFET based SRAM cell design is described in [26] and [27].

Despite the raw material limitations in the fabrication of transistors, the speed of progress in designing and CMOS technology scaling is very slow and the size reduction is very limited. One of our challenges is to reduce the leakage current which includes sub-threshold leakage and gate leakage [28,29].

Besides utilizing area more efficiently, FinFETs are also very efficient in controlling leakage currents, compared to CMOS transistors [30,31]. Better control on the channel is achieved since the channel is surrounded by the gate and there is an improvement in the channel effects. Moreover, the higher mobility of carriers reduces the sub-threshold leakage current [32].

4- PROPOSED CIRCUIT

Most of the circuits designed in FinFET technology are digital and a small percentage of them are analog. In this study, an analog comparator circuit is designed and presented. To compare the proposed circuit in FinFET technology with the conventional CMOS circuits, a FinFET circuit was required. However, there was no available FinFET analog circuit. Indeed, very little work has been done on using FinFET in the ana-log domain as it is an innovative and still developing area. Therefore, for a better comparison of the proposed comparator circuit in 65 nm FinFET technology with conventional designs, a prior art design is required. It was decided to redesign an existing 180 nm CMOS circuit in 65 nm CMOS technology, and then, use it in 65 nm FinFET technology for a comparison with previous designs.

In the proposed circuit (Figure 5) several transistors are eliminated, so the delay, power consumption, and the occupied area are reduced. To reduce the size and power consumption, transistors MSW1 and MSW2 are replaced by the M1 and M2as back gates.

Mc1 and Mc2 are used to cross-coupled connected to fn and fp points. The two transistors MR1 and MR2 are connected to the points fn and fp, so they work with the rapid changes of fn and fp, and with rapid shutdown, help reduce power consumption. Therefore, the back gates of these two transistors are also connected to GND to be in their weakest state and turn off faster when fn or fp goes to zero.

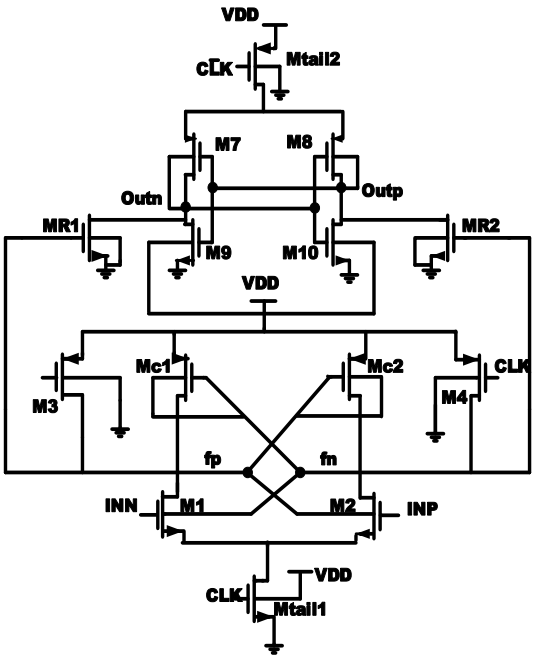

Figure 5. Proposed Comparator

As the voltage of fn drops, M1 would go off. Moreover, the back gate of M2 is connected to fp, and the decrease in the voltage of fp results in disconnection from GND. Therefore, by using proper back gates, two fewer transistors are needed, meanwhile, power consumption and chip area are reduced. Additionally, the overall switching speed increases because parasitic elements are reduced.

In conventional comparator circuits, speed increases with the proper use of positive feedback. Thus, in the proposed circuit, back gates and cross-coupled positive feedback are properly combined to reduce the overall delay significantly. Higher speed and lower power dissipation are achieved by connecting the gate of MC1 to fn, the gate of MC2 to fp, the gate of M7 to the drain of M8, and the gate of M8 to the drain of M7. The back gates of MR1 and MR2 are connected to GND to put them in their weakest state to increase the switching speed. It is worth mentioning that the back gate of N-channel transistors should be connected to VDD and P channel transistors' back gate should be connected to GND to increase their fanout and remain in the weakest state. Therefore, the back gates of M10 and M9 are connected to VDD to turn off the MR1 and MR2 later and are located in the upper cross-couple.

The two transistors MR1 and MR2 are connected to the points fn and fp, so they work with the rapid changes of fn and fp, and with a rapid shutdown, help reduce power consumption. Therefore, the back gates of these two transistors are also connected to GND to be in their weakest state and turn off faster when fn or fp goes to zero.

M3 and M4 are P-type and their back gates are connected to GND. Mtail1 is located at the bottom of the circuit and its back gate is connected to VDD. This transistor has a profound impact on the speed of the proposed circuit. Similarly, Mtail2 is a P-type transistor located at the top of the circuit with its back gate connected to GND. Since N-channel transistors are stronger, they can pass more current and are faster than the P-channel transistors.

In other words, the innovation of the proposed design is that to reduce the size and power consumption, two transistors MSW1 and MSW2 were removed and the back gate of two transistors M1 and M2 were cross-coupled and both were connected to the points fn and fp. In previous designs, the MSW1 transistor was cut off as the fn voltage decreased, but now, as it decreases, the M1 goes off because its back gate is connected to the fn. Also, transistor M2, whose back gate is connected to fp, goes off and prevents connection to GND. With proper use of back gates, two transistors are removed, speed is increased and power consumption is reduced. It should be noted that the connection of back gates to two points fn and fp is an innovation and the output power of the transistor is regulated by the current of these two points to optimize power consumption and increase speed. The back gate is not only for connecting to the vdd and ground to increase or decrease the power of the transistor, and by connecting the back gate to other suitable points of the circuit, this can also be done, and according to the type of design and proper use of the back gate can be Increased speed and reduced power consumption.

5- RESULT AND DISCUSSION

As explained above, the new comparator circuit using the 65 nm FinFET technology, simulated in H-SPICE circuit simulator and the results are shown in Table 2, Figure 6 and Figure 7 respectively.

Table 2. Results of the proposed circuit

Technology	W (μm)	L (μm)	Power consumption (μW)	Delay (ps)
FINFET 65 nm	4.54	0.91	6.7	272

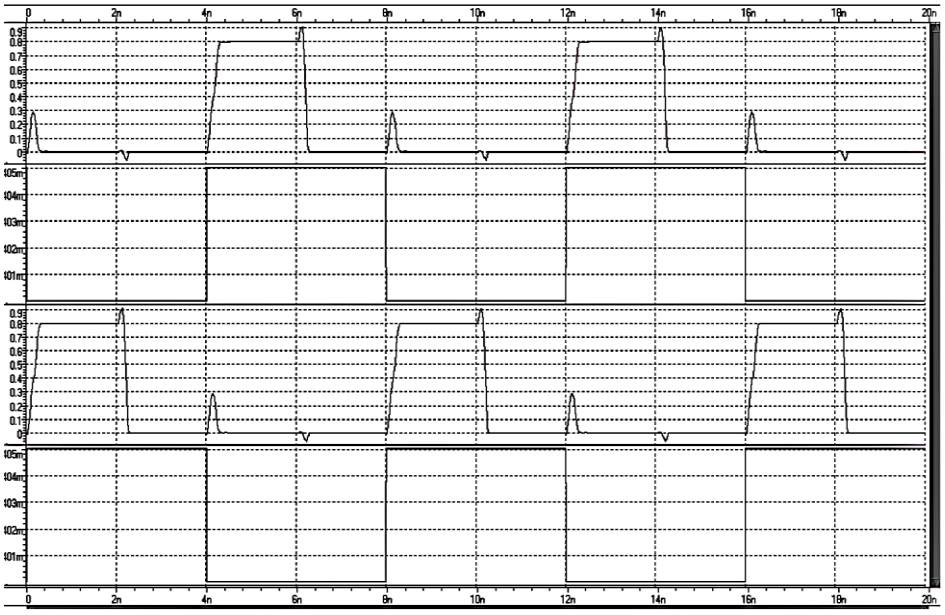

Figure 6. Waveforms of proposed comparator

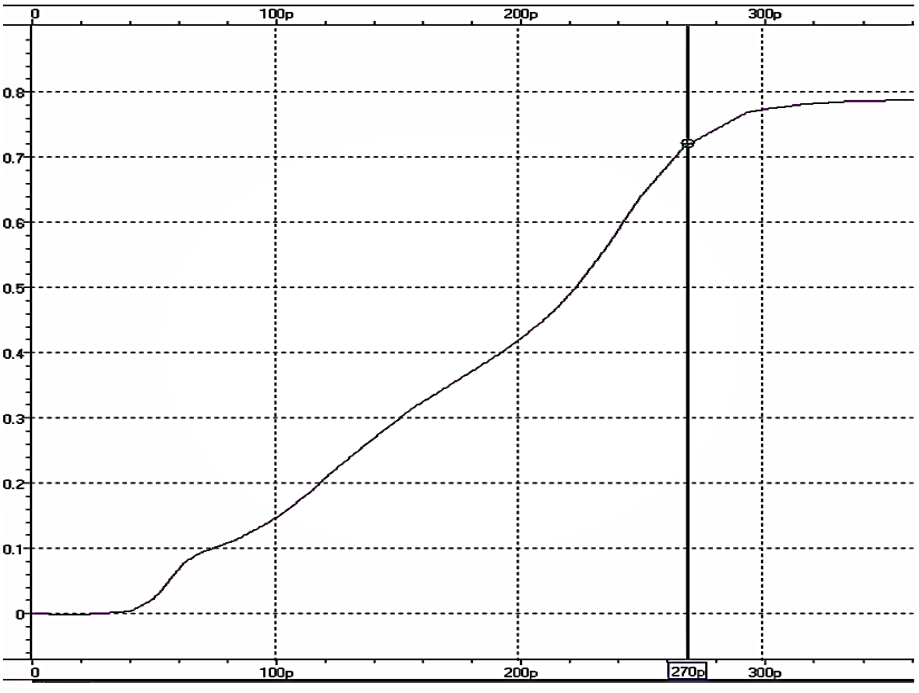

Figure 7. Time response of proposed comparator

Proper swing of the outputs indicates the optimal performance of the proposed circuit. The amount of time delay in 90% of the final output level is 272 ps.

Accordingly, the replacement of MOS transistors with FinFETs are more suited to their operating conditions and the overall performance of the circuit is increased significantly.
To better compare the results of the proposed circuit with the conventional designs, graphical representations are plotted in Figures 8 to 10.
The difference in the power consumption of the designs with FinFET and CMOS technology is shown in Figure 8. The amount of power consumed in 180 nm CMOS technology is 329 µw, while the corresponding value in 65 nm FinFET technology is 6.7 µw.

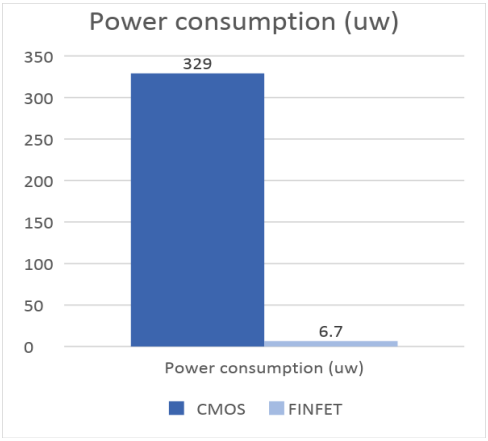

Figure 8. Power consumption of the two designs in FinFET and CMOS technologies

Figure 9 and Figure 10 compare the values of delay and area of the two comparator circuits in different technologies. The delay and occupied area in CMOS technology are 550 pS and 392 um^2, respectively. These values are reduced to 272 pS and 4.13 um^2 in 65 nm FinFET technology. These results show the superiority of the proposed circuit in FinFET technology.

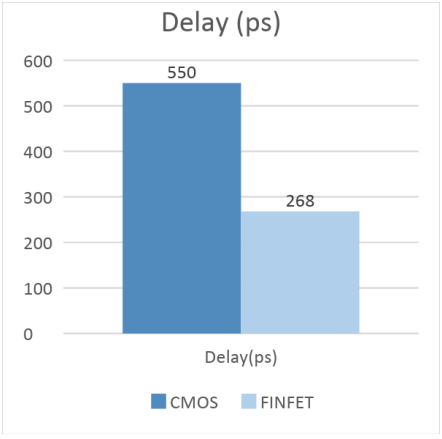

Figure 9. Delays of two comparator circuits in different technologies

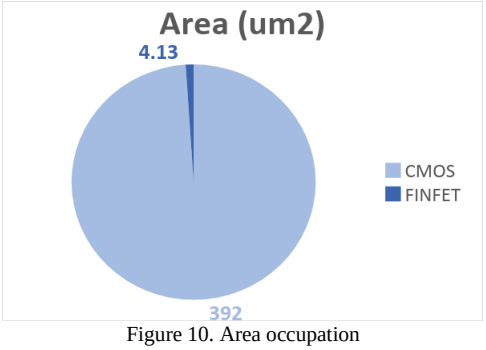

Figure 10. Area occupation

6- CONCLUSION

The power consumption of the proposed comparator circuit is 6.7 μW, which is 97.96% less than the previous circuit, i.e., the power consumption is reduced about 49 times. The measured delay of the circuit is 272 pS, which decreased by 51.27% compared to the previous circuit. The occupied area of the proposed circuit was 4.13 um^2, compared to 392 um^2 in the previous circuit, which means a 98.94% decrease. Consequently, all important parameters of the proposed comparator circuit are significantly improved. Using new tools such as CNTFETs and designing in the subthreshold area are from future works.

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