A Smart Four-Input Minority Gate Based on QCA Technology

Samaneh-Sadat Hashemipour[1], Keivan Navi [2]*

[1]Department of Electrical Engineering, Central Tehran Branch, Islamic Azad University, Tehran, Iran
[2] Faculty of Computer Science and Engineering, Shahid Beheshti University, Tehran, Iran, navi@sbu.ac.ir

Abstract

Quantum-dot cellular automata (QCA) is a new and very attractive technology for implementing logic gates and digital circuits at the nanoscale. This technology has very attractive and amazing features such as: low area, high processing speed and low power consumption. Over time, with the advancement of science and technology, there is hope that QCA technology will replace today's VLSI technology. Minority gates are one of the most important elements in digital circuit design. In this paper, a smart four-input minority gate is presented and it is the first time that a priority four-input minority gate is proposed. The proposed minority gate architecture is evaluated and simulated using the QCADesigner tool version 2.0.3. The results show 100% accuracy. By using this type of gates, the hardware required to design QCA circuits can be significantly reduced.

Keywords: Quantum-dot cellular automata technology, smart minority gate, Nano scale technologies, logical circuit design.
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1. Introduction

CMOS technology has many drawbacks such as high leakage current, high power consumption, high cost of lithography, low compression problem and speed limit in the GHz range. In contrast, the Quantum-dot cellular Automata is one of the significant alternatives. In QCA technology, binary information is determined by the position and arrangement of electrons instead of the current used in CMOS. Some of the special features of this technology are smaller size, higher speed, higher switching frequency, lower power consumption and higher scale integration. [1]

The basic logic element of the Quantum Cell Automated Circuit (QCA) is the majority gate(MV) and the minority gate (mV) which are one of the important components in the design of digital circuits. [2-3] In this paper, we propose a four-input minority gate, which can be used as a base gate in the design of other digital circuits such as priority decoders.

The remainder of this paper is organized as follows. In Section 2 a review of the QCA is presented; subsequently, related previous works are discussed in Section 3. Section 4 introduces our method for designing the four-input minority gate and simulation results has proposed. Finally, conclusions drawn from this study are provided in Section 5.

2. Overview of QCA

A standard QCA cell (Fig. 1) is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites that electrons can occupy by tunneling to them. Two free electrons can tunnel to any of these quantum-dots within the cell. These electrons will try to occupy the furthest possible site with respect to each other due to mutual electrostatic repulsion; so for minimum energy states of a quantum-dot cell, the electrons always occupy diagonally opposite positions in the square. Depending on the position of these electrons in the cell, its polarization can be determined to be one of the two stable cell-polarization states, as illustrated in Fig. 1. These two configurations are denoted as cell polarization P=+1 (binary ‘1’ state) and P=−1 (binary ‘0’ state) [4-6].

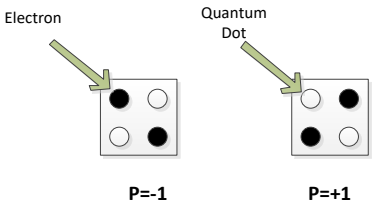


Fig. 1. Basic QCA cell and binary encoding.

All QCA circuit proposals require a clock not only to synchronize and control information flow but the clock actually provides the power to run the circuit. Each QCA circuit requires a clock to synchronize and control information flow. Also the clock actually provides the power to run the circuit. The clocking of QCA can be accomplished by controlling the potential barriers between adjacent quantum-dots. Accordingly, each QCA cell must be associated with one of the four successive clock zones depicted in Fig. 2. The lag between phases is considered to be $\pi/2$. Each clock zone has four phases labeled as: switch, hold, release, and relax. During the Switch phase, the inter-dot barrier is slowly raised and a cell attains a definitive polarity under the influence of its neighbors. In the hold phase, the barriers are held high so the cell maintains the current polarization and the outputs thus obtained can be used as inputs for the next stage.

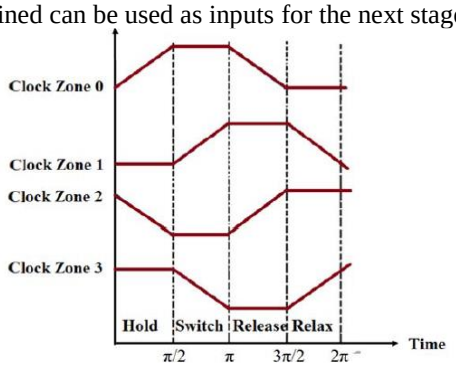


Fig. 2. Four phase QCA clocking

On the other hand, in the release phase, the QCA cells start to lose their stored value, i.e., becomes unpolarized. The last phase is the relax phase. In this phase, the QCA cells lose their value and become unpolarized [2, 6].

An array of QCA cells can be arranged to perform as a QCA wire. In a QCA wire, the binary signal propagates from input to output because of the Columbic interactions between cells (Fig. 3). In addition, in Fig. 4 some common inverters have been illustrated.

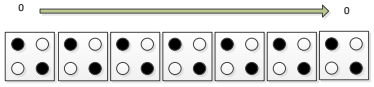


Fig. 3. QCA wire.

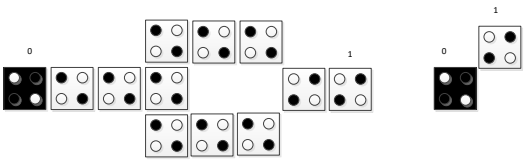


Fig. 4. QCA inverter.

The QCA majority gate performs a three-input logic function. A layout of a QCA majority gate is depicted in Fig. 5. Assuming the inputs are A, B, and C, the logic function of this majority gate is

$$M(A, B, C) = AB+BC+AC \quad (1)$$

By forcing one of the three inputs of the majority gate to a constant logic "0" or a "1" the majority gate can be used to perform AND/OR operations as shown in the following equations:

$$M(A, B, 0) = F = A.B \quad (2)$$

$$M(A, B, 1) = F = A.B + B.1 + 1.A = A.B + B + A = A(1 + B) + B = A + B \quad (3)$$

Any QCA circuit can be built using only majority gates and inverters [7, 8].

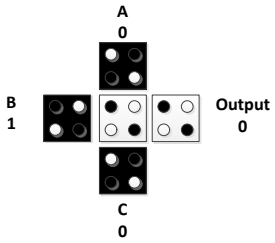


Fig. 5. A three-input majority gate MAJ3

The minority gate with three inputs is defined as follows:

$$m(A, B, C) = A'.B' + B'.C' + A'.C' \quad (4)$$

The implementation of NAND and NOR gates with minority gates is shown in Equations (5) and (6), respectively. The schematic of a minority gate is also shown in Fig. 6.

$$m(A, B, 0) = A'.B' + B'.(1) + A'.(1) = (A' + B') = (A.B)' \quad (5)$$

$$m(A, B, 1) = A'.B' + B'.(0) + A'.(0) = A'.B' = (A+B)' \quad (6)$$

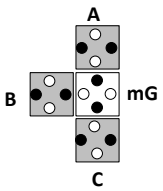


Fig. 6. A three-input minority gate [7]

3. An overview of minority gates with more than three inputs

Since the simple QCA majority and minority gate structure can implement relatively complex operations with minimal hardware (compared to transistor-based models), the researchers decided to extend the majority and minority 3-input gates to larger, more complex circuits. Fig. 7 shows four types of layout of a five-input minority gate. All layouts also have a majority output [8-9]. In the case of the seven-input minority gate, the seven-input majority gate introduced in [10] can be used and only its output should pass through the inverter gate to become a minority gate. In [11], the five-input majority gates introduced so far are given, which can be turned into a minority gate with only one inverting gate.

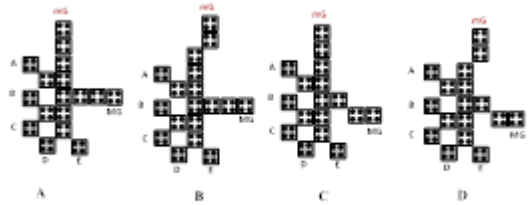


Fig. 7. Minority gates with five inputs [9]

4. Proposed Minority gate four inputs

The four-input minority gate proposed is shown in Fig. 8. All surrounding cells are considered as input cells. Due to the structure of the inverter gate, at first all inputs in Fig. 8 are inverted. The fourth input cell has less effect on the output cell because it is farther away from other voting cells, so the output value of this minority gate using the effect of the coefficient (1) is determined from other input cells and the coefficient of 0.5 is determined from the fourth input cell (D). In other words, this is a priority minority gate. The truth table of the gate of the four-input minority based on the sum of the inputs is shown in Table 1. In the left column of this table, the sum of the inputs is written with a coefficient of 0.5 for the fourth input. The maximum value is 3.5. Obviously for the following values lower than 2, the minority value is equal to 1 and for the values greater than or equal to 2, the minority value is equal to 0.

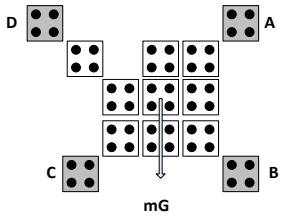


Fig. 8. Proposed four-input minority gate

Table.1.
The truth table of the four-input minority gate based on the sum of the inputs.

∑(A, B ,C, 1/2 D)	m(A, B, C, D)
0	1
.5	1
1	1
1.5	1
2	0
2.5	0
3.	0
3.5	0

For physical proof, we assume that all cells are similar, the length of each is (a = 18nm), there is a space (x = 2nm) between the two neighboring cells and only the neighboring cells affect each other. It should be noted that to achieve greater stability, the electrons of the QCA cell are arranged in such a way that their potential energy is minimized. The potential energy between two cells is calculated using Equation (7). In this equation, U is the potential energy, k is Coulomb's constant, q1 and q2 are the electric charges and r is the distance between the two electric charges. UT is the sum of potential energies between two cells.

$$U = \frac{kq1q2}{r} \tag{7}$$

$$Kq_1q_2 = 9*10^9*(1.6)^2*10^{(-38)} = 23.04*10^{-29} = A = cte \tag{8}$$

For example, the potential energy of neighboring cells (Fig. 9) as well as other states can be calculated. Table 2 shows the potential energy calculation of adjacent cells in different states [12-13].

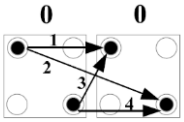
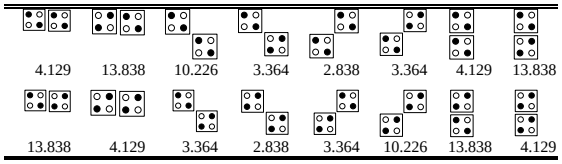


Fig. 9. Example of calculating the potential energy between two cells

$$U_1 = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} = 1.152 * 10^{-20}(J) \tag{9}$$
$$U_2 = \frac{23.04 * 10^{-29}}{41.59 * 10^{-9}} = 0.553 * 10^{-20}(J)$$
$$U_3 = \frac{23.04 * 10^{-29}}{18.11 * 10^{-9}} = 1.272 * 10^{-20}(J)$$
$$U_4 = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} = 1.152 * 10^{-20}(J)$$
$$U_T = 4.129 * 10^{-20}(J)$$

Table.2.
Calculation of potential energy of adjacent cells (10-20 J)



According to the proposed gate design and the distance between the inverse of the fourth input and the output cell, in addition to the items in Table 2, are shown in Fig. 10 and the horizontal distance of the fourth input and the output cell is 22 nm.

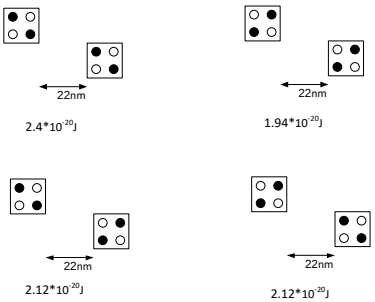


Fig. 10. The calculation of potential energy between two cells (fourth input and output)

With four inputs, we have 16 states. We have given the physical proof of one state for example. In this state, the inputs are considered (A = 0, B = 1, C = 0, D = 1) respectively. In case A in Fig. 11, the output is assumed to be one, and similarly in case B, the output is assumed to be zero, and in both cases the total energy is calculated. In case A, the total energy value is 42.452 * 10-20 J and in case B is equal to 74.706*10-20 J, so the minimum energy is obtained in case A.

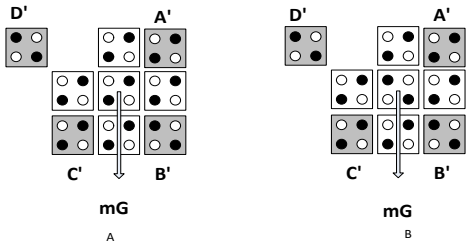


Fig. 11. Example of potential energy calculation for inputs (A = 0, B = 1, C = 0, D = 1) and outputs A-1 and B-0

In this study, the proposed layout is simulated using the QCADesigner software. The neighboring cells have a center-to-center distance of 20 nm. All of the simulation measurements and conditions are set as their default values in the QCADesigner tool. The proposed structure was simulated using the parameters listed in Table 3. The corresponding clocked QCA layout is presented in Fig. 12 [14].

Table.3.
Parameters used in the gate simulation of the proposed four-input majority gate.

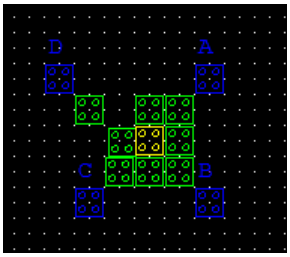


Fig. 12. QCA layout of proposed four-input minority gate

The area of consumption areas of the circuit is 0.05 µm2. The simulation results of the new circuit and the results of comparison between minority gates are shown in Table 4. It should be mentioned that the results are based on our simulations. Part of the simulated output is shown in Fig. 13 which shows the correct operation of the circuit.

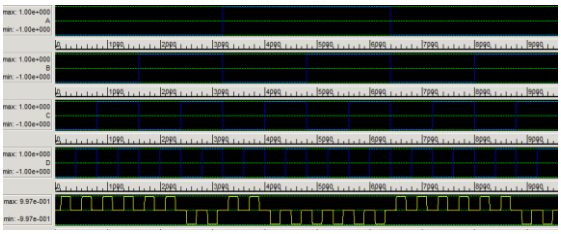


Fig. 13. Proposed four-input minority gate simulation output

Table.4.
Simulation results of the proposed four-input minority gate structure and Comparison of QCA minority designs

Parameter	*Value*
Cell size	18 nm* 18 nm
Cell separation	2 nm
Radius of effect	65 nm
Number of samples	12800
Convergence Tolerance	0.001000
Relative Permittivity	12.900000
Clock High	9.800000e-022
Clock Low	3.800000e-023
Clock Shift	0.000000
Clock Amplitude Factor	2.000000
Layer Separation	11.500000
Maximum iterations per sample	100

5. Conclusion

QCA with its unique specifications reduces the physical limitations of CMOS implementation and is an attractive and emerging technology to replace it. This technology has attracted a lot of attention because it has very small dimensions; about the dimensions of molecules and even atoms and also consumes very little power. These benefits have encouraged researchers to use this technology in the design of digital circuits. In this paper, a four-input minority gate is presented. In fact, with the unequal

voting rights of the inputs of this gate, the inputs of the minority gate have a priority. The four-input minority gate can be an important basic block in QCA circuits. The gate is implemented in one layer and uses thirteen QCA cells. The Performance of this proposed minority gate has been proven and evaluated by computer simulation. Our results have 100% accuracy. Since the new minority gate has an extraordinary structure, it can lead to further advances in QCA circuits.

References:

[1]. P. D. Tougaw and C. S. Lent. Logical devices implemented using quantum cellular automata. J. Appl. Phys., Vol. 75, No. 3, pp. 1818–1825, February 1994.

[2]. M. Kianpour, R. Sabbaghi-Nadooshan, K. Navi, A novel design of 8-bit adder/subtractor by quantum-dot cellular automata, Journal of Computer and System Sciences Vol. 80, No. 7, pp. 1404-1414, 2014.

[3]. C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein, Quantum cellular automata, Nanotechnology Vol. 4, p. 49, 1993.

[4]. R. Sabbaghi-Nadooshan, Evolutionary QCA Universal and Testable Gate, International Journal of Smart Electrical Engineering, Vol. 9, No. 2, 83–88, 2020.

[5]. M. Kianpour, R. Sabbaghi-Nadooshan, A Novel Quantum-Dot Cellular Automata X-bit x 32-bit SRAM, IEEE transactions on very large scale integration (VLSI) Systems, Vol. 24, No. 3, pp. 827-836, 2016.

[6]. P.D. Tougaw, C.S. Lent, Dynamic behavior of quantum cellular automata, Journal of Applied Physics vol. 80, No. 8, , pp. 4722–4736, 1996.

[7]. S. Roy, B. Saha, “Minority Gate Oriented Logic Design with Quantum-Dot Cellular Automata,” In: S. El Yacoubi, B. Chopard, S. Bandini (eds) “Cellular Automata,” ACRI 2006. Lecture Notes in Computer Science, vol. 4173. Springer, Berlin, Heidelberg, 2006.

[8]. K. Navi, S. Sayedsalehi, R. Farazkish, and M. Rahimi Azghadi, “Five-input majority gate, a new device for quantum-dot cellular automata,” J. Comput. Theor. Nanosci., Vol. 7, pp. 1546–53, 2010.

[9]. P. A. R. L. Silva, J. R. S. B. Alves, R. S. Ferreira, O. P. V. Neto and J. A. M. Nacif, "A Novel Five-input Multiple-function QCA Threshold Gate," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, pp. 1-5, 2018.

[10]. H. Mohammadi, K. Navi and M. Hosseinzadeh, An Efficient Quantum-Dot Cellular Automata Full Adder Based on a New Convertible 7-Input Majority-Not Gate, IETE Journal of Research, 2020.

[11]. H. Mohammadi, and K. Navi, “Energy-efficient single layer QCA logical circuits based on a novel XOR gate,”J. Circuits Syst. Comput., Vol. 27, no. 14, pp. 6–7,2018.

[12]. S. S. Ahmadpour, M. Mosleh, and S. Rasouli Heikalabad, “The design and implementation of a robust single-layer QCA ALU using a novel fault-tolerant three-input majority gate,” J Supercomput 76, 10155–10185 (2020).

[13]. N. Moosavi, K. Navi, V. Aghazarian, “Ultra-Low Cost Full Adder Cell Using the nonlinear effect in Four-Input Quantum Dot Cellular Automata Majority Gate,” International Journal of Nonlinear Analysis and Applications 11 (2), 1-16(2020).

[14]. S. Hashemipour, K. Navi, R. Sabbaghi-Nadooshan, “A Robust Encrypted Nanocommunication in QCA Circuit,” Microprocessors and Microsystems, 104240, 2021.

[15]. QCADesigner Home Page /www.atips.ca/projects/qcadesigner