Improving Adaptive Resolution of Analog to Digital Converters Using Least Squares Mean Method

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Abstract

This paper presents an adaptive digital resolution improvement method for extrapolating and recursive analog-to-digital converters (ADCs). The presented adaptively enhanced ADC (AE-ADC) digitally estimates the digital equivalent of the input signal by utilizing an adaptive digital filter (ADF). The least mean squares (LMS) algorithm also determines the coefficients of the ADF block. In this scheme, the input bandwidth is limited to the Nyquist-rate. This scheme has the ability of enhancing its resolution by one bit through doubling the gain of a low-quality amplifier circuit. Behavioral simulation results are also provided for a 10-bit AE-ADC to verify the usefulness of the approach. Simulation results indicate that the spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion-ratio (SNDR) are 68.8 dB and 55.5 dB, respectively.

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INTRODUCTION

DIGITAL signal processing (DSP) techniques are swiftly developing as nanometer CMOS technologies allow the implementation of high-speed, low-power digital blocks with high integration density. Furthermore, the design of circuits using op-amp with the required precision are critically hard in advanced CMOS processes. Digital-to-analog converters (DACs) often construct the main block of most ADCs (e.g., pipelined, successive approximation register (SAR), and delta-sigma ADCs). DAC imperfections arising from mismatch among DAC elements directly manifest itself through the performance degradation of ADCs. Furthermore, adaptive digital algorithms have the ability to track and correct imperfections of ADCs in the digital domain. Thus, utilization of adaptive digital methods in ADCs has been increasingly growing so as to enhance the resolution, to alleviate circuit non-idealities, and to increase the operating frequency (Shahoo & Razavi, 2012; Zeinali et al., 2014; Mafi & Shamsi,2015; Kim et al., 2010; Fredenburg & Flynn, 2012; Volkov et al., 2011)

Pipelined ADC is an appropriate candidate for high-speed digitization with moderate-resolution. However, a pipelined ADC often needs high-precision, power-hungry amplifiers and it also imposes latency between the sampled input signal and its digital output (i.e., half delay per a pipelined stage). Furthermore, SAR ADCs are the most energy-efficient type of ADCs. Therefore, they are popular in low-power applications with moderate sampling-rate and resolution. Nevertheless, an S-bit SAR ADC often samples its input signal at 1/S of its clock frequency. Although delta-sigma ADC is an attractive converter for high-resolution applications, this ADC usually restricts the input frequency to a small portion of its operating frequency Shahoo & Razavi, 2012; Zeinali et al., 2014; Mafi & Shamsi,2015; Kim et al., 2010; Fredenburg & Flynn, 2012)

This paper presents an adaptive digital resolution improvement scheme for extrapolating and recursive ADCs (Yang & Spiegel, 2005; Lewyn, 2000). The proposed adaptively enhanced ADC (AE-ADC) continuously esti-mates the input signal in the digital domain through an adaptive digital filter (ADF). The digital estimate of the ADF is extracted based on the previous samples of the input signal. It is worth mentioning that the AE-ADC also has the ability to achieve the required resolution through low performance analog circuits. The AE-ADC improves its resolution according to the gain of a low-quality amplifier circuit. For each doubling the amplifier gain, the AE-ADC resolution increases by one bit (Yang & Spiegel, 2005; Lewyn, 2000). The AE-ADC operates at full sampling-rate as opposed to the SAR and delta-sigma ADCs. The AE-ADCs does not exhibit any extra delay unlike pipelined ADCs as well. The AE-ADC consists a coarse ADC (referred to as sub-ADC) with a lower accuracy than the resolution of the AE-ADC unlike pipelined and SAR ADCs (Yang & Spiegel, 2005; Lewyn, 2000).

The remainder of the paper is structured as follows. Section II presents the fundamentals and architecture of the AE-ADC. Simulation results and discussions are provided in Section III. Finally, Section IV concludes the paper.

AE-ADC FUNDAMENTALS AND ARCHITECTURE

In this section, the fundamental concept of the AE-ADC is first described. For presentation clarity, all signal is normalized to the reference voltage; the signals are therefore distributed within the interval $[-1, 1]$. Depicted in Fig. 1 is the structure of the AE-ADC based on extrapolating and recursive ADCs (Yang & Spiegel, 2005; Lewyn, 2000). At each discrete-time, n, the task of the ADF is to digitally evaluate the input signal of the AE-ADC and continuously generate the digital estimate, $D_{est}(n)$. Afterwards, this digital signal needs to be evaluated so as to find the quality of the ADF estimation process. For this reason, the digital estimate, $D_{est}(n)$, is then converted to its analog version, Vest(n), by a coarse DAC (referred to as sub-DAC) and subtracted from the input signal by the input differencing node in order to extract the error signal, $V_e(n)$. Since the ADF block operates in the digital domain, the required error signal must be converted to

its digital equivalent, $D_e(n)$ using the sub-ADC. It is notable that the addition of $D_{est}(n)$ and $D_e(n)$ also constructs the digital format of the input voltage, $D_{out}(n)$ (i.e., the AE-ADC digital output).

Next, the ADF utilizes the previous samples of the digital output, $D_{out}(n)$, to extract the present sample of the digital estimate, $D_{est}(n)$, and to evaluate the estimation process using $D_e(n)$.
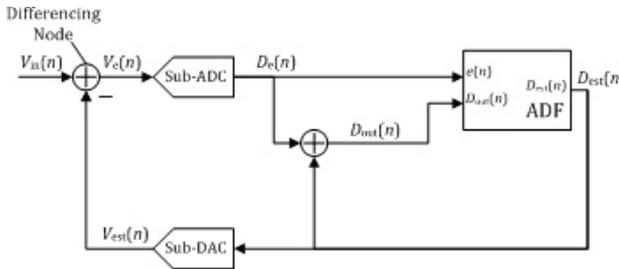
Fig. 1. Basic architecture of AE-ADC.
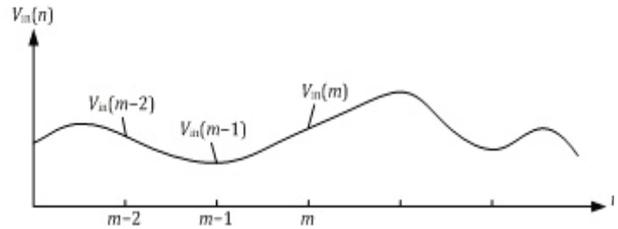
Fig. 2. Concept behind AE-ADC.
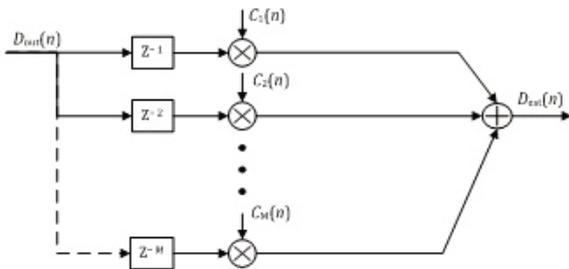
Fig. 3. FIR filter of ADF block.
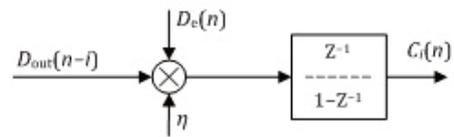
Fig. 4. LMS machine of ADF block.

Adaptive digital filter operation

Fig. 2 depicts the concept behind the AE-ADC. As long as the input signal is band-limited and bounded to the Nyquist-rate, it may be estimated using its previous samples through a finite impulse response (FIR) filter (Zeinali et al., 2014; Volkov et al., 2011; Widrow & Stearns,1985). For this reason, the ADF is comprised of a FIR filter as well. The digital version of the input signal, $D_{out}(n)$, is exploited in order to generate the digital estimate as following:

$$D_{est}(n) = \sum_{i=1}^{M} C_i \cdot D_{out}(m-i) \qquad (1)$$

where C_i and M denote the coefficients and the length of the FIR filter, respectively (Zeinali et al., 2014; Volkov et al., 2011; Widrow & Stearns,1985). Shown in Fig. 3 is the FIR filter section of the ADF block. Actu-

ally, the coefficients C_i, i = 1,…, M, depend on the length of the filter and also the frequency and bandwidth of the input signal. As a consequence, the coefficient Ci must be adaptively determined during the normal operation of the AE-ADC. It is obvious that as the distribution of the error signal reduces, more accurate estimates of the input signal are extracted by the ADF block. Besides, the error signal needs to be zero for the optimal estimation process. In turn, a mechanism must be exploited to adjust the ADF coefficients such that the error signal is confined close to zero as possible.

A least mean squares (LMS) algorithm has the capability of determining the ADF coefficients such that the mean the squared error, $E(V_e(n)^2)$, is derived to its minimum (Widrow & Stearns, 1985).The ADF is consequently comprised of the LMS algorithm to adjust the coefficients of the FIR filter as well [Appendix-A]. However, the digital signal is utilized

rather than the signal $V_e(n)$ because of the fact that the LMS performs on digital signals. The LMS update equations can be expressed as:

$$C_i(n+1) = C_i(n) + \eta D_{out}(n-i) D_e(n) \quad i = 1, ..., M) \tag{2}$$

Fig. 5. Complete structure of AE-ADC.

where η denotes the step-size of the LMS algorithm (Zeinali et al., 2014; Volkov et al., 2011; Widrow & Stearns,1985). Fig. 4 illustrates the block diagram of the LMS engine. The step-size, η, determines the convergence-rate of the LMS algorithm (Widrow & Stearns,1985). For each coefficient, a replicated block of the LMS machine is employed. All the replicas operate simultaneously.

Coarse data converters

As the delay between the analog input and digital output of the sub-ADC must be identical to one, the sub-ADC can be practically realized using a flash or SAR ADCs. This limitation is imposed by the ADF block. Furthermore, after the convergence of the LMS machine, the error signal is distributed around zero. Accordingly, an amplifier with a gain of G_a is utilized to normalize the error signal to one such that the entire range of the sub-ADC is exploited by the error signal. The digital output of the sub-ADC is then scaled down by a factor of $1/G_a$ through an additional digital block, G_d.

It is worth mentioning that the number of nominally identical elements in a sub-DAC increases exponentially with the sub-DAC resolution. Hence a binary weighted element array is suitable for the implementation of the sub-DAC with a resolution of more than 4 bits (Sahoo & Razavi, 2012; Fredenburg & Flynn, 2012). The AE-ADC thus utilizes a binary weighted DAC. In addition, for each of the sub-DAC input bits, a weighted element is dedicated. Nonetheless, because the weight error in a sub-DAC element is actually proportional to the corresponding weight, the design of a binary weighted sub-DAC also becomes harder as the weight ratio of the greatest element to smallest element grows exponentially through each additional number of the sub-DAC input bit (Sahoo & Razavi, 2012; Fredenburg & Flynn, 2012). Therefore, the input bits of the sub-DAC are truncated to K bits by ignoring the remaining least significant bits (LSBs) though truncation operation, *Trun*(.).

Final structure of AE-ADC

All the input differencing node, sub-DAC, and amplifier block are actually realized by a switched-capacitor circuit (i.e., the same as the multiplying-DAC (MDAC) in pipelined ADCs). In this architecture, the binary weighted elements are employed for the sub-DAC implementation [Appendix-B].

Fig. 5 shows the complete structure of the AE-ADC. In this design, since the sub-ADC inserts a unit delay in the digital error, the digital signal $D_{est}(n)$ must also be delayed by one unit for the compatibility of the discrete-time. Therefore, the LMS equations are finally given

by

$$C_i(n)= C_i(n-1)+ \eta D_{out}(n-i-1)D_e(n-1) \quad i=1,...,M. \tag{3}$$

It is worth mentioning that the maximum achievable effective number of bits (ENOB) of the AE-ADC is determined by

$$ENOB_{max} = B_{sub-ADC} + \log_2(G_a). \tag{4}$$

Consequently, the resolution of the AE-ADC is enhanced by one bit through doubling the gain G_a. In summary, the AE-ADC provides an approach to improve the sub-ADC resolution according to the gain Ga. The most interesting advantage of the proposed AE-ADC is its immunity to the mismatch between the gains G_a and G_d and to the sub-ADC offsets [see Section III-B].

SIMULATION RESULTS AND DISCUSSIONS

To verify the effectiveness of the proposed technique, a 10-bit AE-ADC is designed and simulated. In the simulations, the AE-ADC is comprised of a 4-bit sub-ADC, a 6-bit binary weighted sub-DAC, and an FIR filter with 5 tabs (M = 5). In addition, thermal noise is considered. A sinusoidal is applied to the AE-ADC with different frequencies as the test signal. The sampling frequency is set to 1; as a result, the frequency of all signals is normalized one. The nominal value of the gains G_a and G_d are 64 and 1/64, respectively. In these simulations, the following mismatch and imperfections are also considered as

1) The amplifier circuit is supposed to be a third-order nonlinear block with the coefficients as following: $a_0=0.005G_{a,nom}$, $a_1=1.125G_{a,nom}$, $a_2=0.005G_{a,nom}$, and $a_3= -G_{a,nom}/2$, where is $G_{a,nom}$ is the nominal gain of the amplifier circuit.

2) The errors of the binary weighted sub-DAC are considered as independent Gaussian random variables with normal deviations as following: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, and 6.4%, according to the weights of the sub-DAC from the most significant bit (MSB) to LSB, respectively.

3) The sub-ADC offset errors are also considered as independent Gaussian distributed random variables with a normal deviation of 50% of the sub-ADC LSB.

The power spectral density of the AE-ADC output is shown in Fig. 6. Depicted in Fig. 7 are the convergence of the ADF coefficients during the AE-ADC conversion operation. Similar results are obtained for different input frequencies as well. The spurious-free dynamic range (SFDR) and signal-to-noise-distortion-ratio (SNDR) are 68.8 dB and 55.5 dB, respectively. Fig. 8 demonstrates the output spectrum of the AE-ADC and an ideal 9-bit ADC with a band-limited Gaussian distributed random input and a nominal amplifier gain of 32 (i.e., in this case, the expected resolution is therefore 9 bits). Moreover, Fig. 9 depicts the coefficients of the ADF block during the AE-ADC conversion operation with the band-limited Gaussian distributed random input. Shown in Fig. 10 are the output spectrum for three gain values with M = 5. As seen from the figure, the resolution of the ADC increases by one bit for each doubling the value of Ga. Fig. 11 illustrates the AE-ADC output spectrum for two values of M with a nominal amplifier gain of 64. The SNDR is enhanced from 51.9 dB to 55.5 dB as M increases from 3 to 5.

LMS algorithm considerations

In this paper, the LMS machine update expression are obtained based on the assumption that the error signal is distributed inside the interval $[-1/G_a, 1/G_a]$ and the digital error is equivalent to its analog format with infinite resolution. However, the error signal actually exceeds the desired range before the convergence of the LMS algorithm. Moreover, the digital error is the quantized version of the error signal, and it consequently contains considerable quantization-error. For this reason, the operation of the LMS machine can be divided into:

1) Initial operation: the error signal distribution is most often greater than $[-1/G_a, 1/G_a]$; hence the amplifier enters its saturation region, and the digital LMS algorithm acts as a sign-LMS.
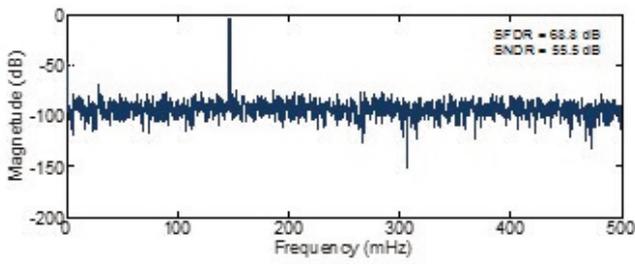
Fig. 6. Digital output spectrum of AE-ADC.
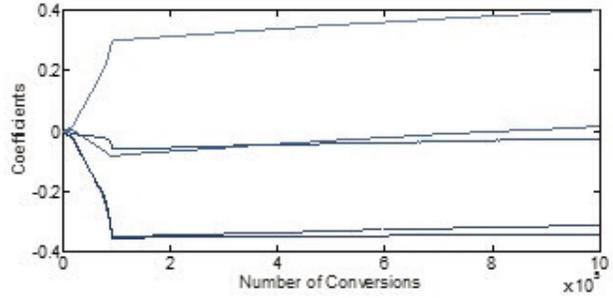
Fig. 7. ADF coefficients during AE-ADC conversion operation.
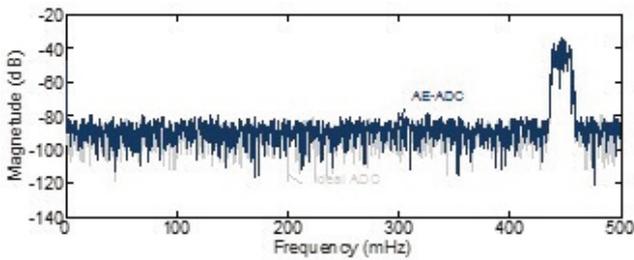
Fig. 8. Digital output spectrum of AE-ADC with a band-limited random input.
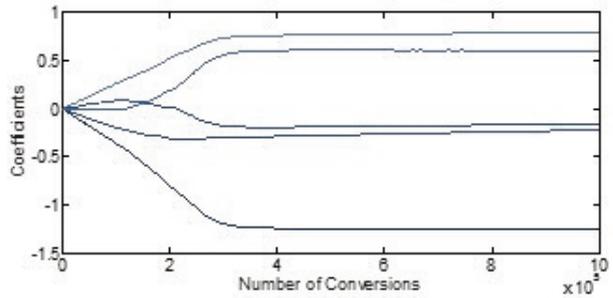
Fig. 9. ADF coefficients during AE-ADC operation with a band-limited random input.

2) Primary convergence: in this stage, the AE-ADC achieves its expected resolution as the error signal is bounded to the interval $[−1/G_a, 1/G_a]$. However, the LMS algorithm continues its operation to find the optimal values of the ADF coefficients. This procedure is normally slow due to the substantial amount of the quantization-error generated by the sub-ADC.

3) Final convergence: the LMS machine have adjusted the coefficients of the ADF to their optimal values.

Finally, the ADF block actually is placed in an external closed-loop. For this reason, the AE-ADC operates well with a small value of M (=5). Simulation results indicate that M must be greater than 2 for AE-ADC proper operation as well. Besides, the variations of the ADF coefficients can lead to the resolution degradation of the AE-ADC. It must be noted that the step-size, η, needs to be chosen such that the fluctuations of the ADF coefficients is confined blow a specific level (Zeinali et al., 2014; Mafi & Shamsi, 2015) and the stability of the ADF block is guaranteed as well.
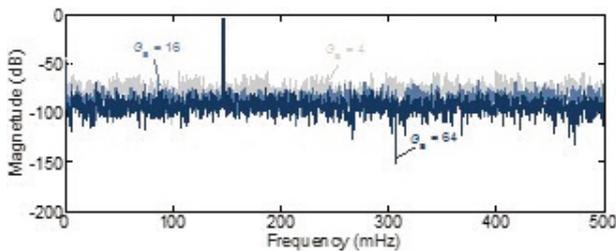
Fig. 10. Digital output spectrum of AE-ADC for three nominal values of G_a.
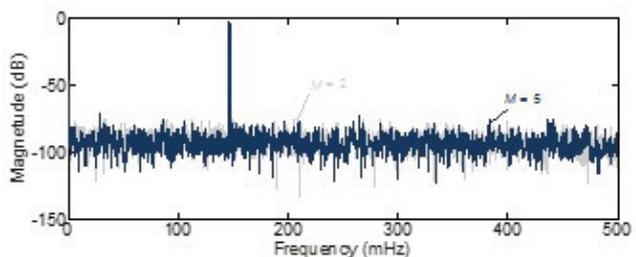
Fig. 11. Digital output spectrum of AE-ADC for two values of M.

MDAC and Sub-ADC considerations

The presented approach mostly decouples the AE-ADC resolution from the imperfections of the amplifier, sub-ADC, and sub-DAC because the MSBs of the digital output are produced by the ADF block. Therefore, the imperfections of these circuits are suppressed in the LSBs of the digital output. The AE-ADC can thus exploit a sub-ADC and sub-DAC with a resolution lower than the needed resolution for the AE-ADC. Furthermore, the MDAC can be realized with a low-gain, low-power op-amp (or even an open-loop amplifier). In summary, the power consumption of MDAC and sub-ADC is not a major issue.

In high resolutions (ENOB>10 bits), the offset and second-order errors in the amplifier may affect the AE-ADC resolution. Nonetheless, the MDAC and sub-ADC are often implemented by differential circuits in practice. Therefore, the offset and second-order errors are negligible.

Additionally, it is imperative to note that as the number of truncated bits in the digital output increases, the error signal distribution range exponentially grows (i.e., it is doubled for each additional truncated bit). Consequently, Ga must be selected according to the distribution range of the error signal. Afterwards, the error signal may exceed its desired interval even after primary convergence providing that a band-limited random is applied to the AE-ADC. In this case, the gain Ga needs to be further decreased in order to constrain the error signal. As seen in the simulation results, the gain G_a is reduced from 64 to 32 when a band-limited signal is applied to the AE-ADC.
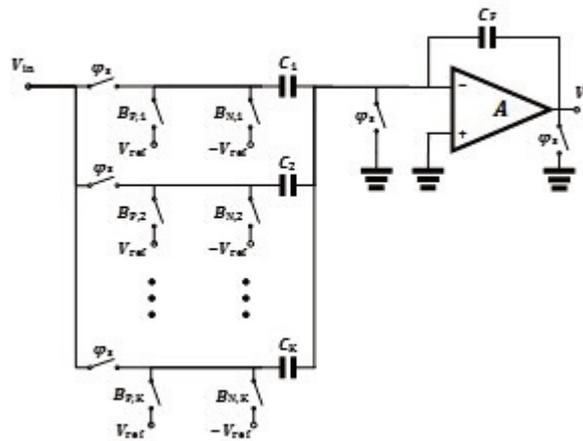
Fig. A1. MDAC practical analog circuit.

Comparison to other ADCs

The AE-ADC operates at full sampling-rate in contrast to the SAR and delta-sigma ADCs. The AE-ADCs does not impose any extra delays between its input signal and digital output and also doesn't need any multiple stages unlike pipelined ADCs. The AE-ADC achieves the required resolution using the low-quality MDAC and sub-ADC as opposed to other ADCs (Volkov et al., 2011; Yang & Spiegel, 2005; Lewyn, 2000).

In the AE-ADC, the digital output generation is similar to the mechanism in pipelined ADCs. The digital output of the first stage and the digitized version of the residue signal are summed so as to produce the digital output of the pipelined ADC. Nevertheless, the sub-ADC of the AE-ADC digitizes the digital output of ADF block.

CONCLUSION

In this paper, an adaptive resolution improvement mechanism for extrapolating and recursive ADCs has been described. The presented AE-ADC has the ability to significantly enhance its sub-ADC resolution. This method continuously

estimates the input signal in the digital domain. The AE-ADC require the sub-ADC with a resolution lower than the AE-ADC resolution since the AE-ADC provides an approach to improve the sub-ADC resolution according to the gain of the low-accuracy amplifier circuit. The AE-ADCs does not insert any extra delays unlike pipelined ADCs.

APPENDIX A

In this Appendix, the LMS update expressions in (2) are derived. The LMS machine optimally minimizes the mean of the cost function (Zeinali et al., 2014; Volkov et al., 2011; Widrow and Stearns, 1985), defined as

$$J(n) = (D_e(n)^2)/2. \qquad (A.1)$$

It can be shown that the LMS machine update equations are expressed as

$$C_i(n+1) = C_i(n) + \eta US_i(n) \quad i=1,...,M \qquad (A.2)$$

where η denotes the step-size of the LMS engine, and the update-sizes of the LMS algorithm are also given by

$$US_i(n) = \partial J(n)/(\partial C) \qquad i=1,...,M. \qquad (A.3)$$

As stated earlier, the digital error is equal to its analog counterpart, and the error signal is also the dereference of the input signal and analog version of the digital estimate, $D_{est}(n)$. Therefore, using (1) and (A.3), the LMS update expressions are represented by

$$C_i(n+1) = C_i(n) + \eta D_{out}(n-i) D_e(n) \quad i=1,...,M). \qquad (A.4)$$

After the convergence, the cost function has its possible minimum value function (Zeinali et al., 2014; Volkov et al., 2011; Widrow & Stearns, 1985). However, the ADF coefficients may have variations mainly owing to the variance of the digital error.

APPENDIX B

In this Appendix, the practical analog circuit of the input differencing node, sub-DAC and amplifier based on the switched-capacitor MDAC is presented. The simplified analog circuit of a MDAC is depicted in Fig. A1. For presentation clarity, a single-ended configuration is shown; nonetheless, a differential circuit is often employed in reality. The analog input signal, $V_{in}(n)$, is sampled during the sampling phase onto the sampling capacitors C_i (i = 1,…, K) while φ_s is high. In the following amplifying period, when φ_a is high, the control signals, BP,i and BN,i are 1 and 0, respectively, in case the sub-DAC input bit, D_{est},i is equal to 1, and otherwise, BP,i and BN,i are identical to 0 and 1, respectively. During the phase φ_a, the capacitor C_i is thus connected to V_{ref} or $-$Vref depending on the sub-DAC input bit, D_{est},i (i = 1,…, K), where Vref and $-V_{ref}$ represent the reference voltages scaled to 1 and -1, respectively. At the end of the phase φ_s, the analog error signal is expressed as

$$V_e(n) = G_a(V_{in}(n) - V_{est}(n)) \qquad (B.1)$$

where G_a and V_{est} are given by

$$G_a = \frac{\sum_{i=1}^{K} C_i}{C_F + \left(C_F + \sum_{i=1}^{K} C_i\right)A^{-1}}, \qquad (B.2)$$

and

$$V_{est}(n) = \sum_{i=1}^{K} \frac{C_i}{\sum_{i=1}^{L} C_i} D_{est,i}. \qquad (B.3)$$

In (B.2), A represents the op-amp DC gain (Sahoo & Razavi, 2012; Kim et al., 2010).

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