

CMOS Design and Realization of Gaussian Membership Function for Application in Fuzzy Controllers

Ali Naderi Saatlo

Microwave and Antenna Research Center, Urmia Branch, Islamic Azad University, Urmia, Iran

Email: ali.naderi@iau.ac.ir

Receive Date: 20 November 2023

Revise Date: 04 February 2024 Accept Date: 13 March 2024

Abstract

In this paper a novel method for realization of Gaussian function is presented. The current-mode circuits are employed for the implementation of main circuits owing to the simple circuitry and intuitive configuration. Unlike the previous works which were based on the transistors worked in weak inversion region, the proposed configuration operates in the saturation region, therefore high-accuracy as well as the high-speed performance are obtained. The proposed circuit is fully programmable in terms of mean value, standard deviation and peak gain of the Gaussian function. Simulation results of the circuit is obtained by HSPICE with TSMC level 49 (BSIM3v3) parameters in 0.35 μ m standard CMOS process.

Keywords: Gaussian Circuit, Membership Function, Signal Processing, Current Mode.

1. Introduction

Signal processing circuits find various applications in many domains such as telecommunications, medical equipment, hearing devices, and disk drives [1]–[4], the preference for an analog approach of signal processing systems being mainly motivated by their high performance operation that allows a real-time signal processing. Current-mode approach of analog signal processing attracted significant interest and has been extensively investigated in recent years [5]–[7], thanks to the potential advantages of high speed operation due to low parasitic capacitor nodes, low power consumption and simple circuitry. This approach has been employed for implementing of functional circuits such as squarer [8] or square rooter [9] circuits,

multiplier/divider [10], [11] or exponential circuits [12].

Besides these circuit functions, the Gaussian function [13], [14] is widely used in many domains such as fuzzy set and systems, neural networks, neural algorithms, neuro-fuzzy and classification applications. In fuzzy set and systems, Gaussian membership function is utilized to construct fuzzifier block which has a dominant effect on the reasoning process of a Fuzzy Logic Controller (FLC). The requirements for analog realization of FLCs are mainly related to the necessity of reducing the power consumption and to the increasing of the circuits' speed for a real-time operation. Therefore, various methods as well as types of GMF have been proposed in order to improve the performance of this membership function.

There are a large number of Gaussian

circuits in the literature which their realizations are based on the different techniques. In [15] it was implemented a mixed-signal CMOS integrated of a Gaussian function for neural/fuzzy hardware, the programmability of the generator being obtained via varying the reference voltages and also the size of transistors in differential pairs. Another method has been presented in [16] which combines the exponential characteristics of MOS transistors in weak inversion with the squaring characteristics in saturation.

The proposed circuit in [17] implements the Gaussian function replacing the classical MOS active devices with FGMOS (Floating Gate MOS) transistors and use these devices as tunable resistors for enhancing the bandwidth of the conventional circuit. A programmable Gaussian function circuit has been presented in [18], this function being designed using simple and intuitive current sources.

It was presented in [19] a compact analog synapse cell, which is not biased in the sub-threshold region for fully-parallel operation, the cell being able to approximate with reasonable accuracy the Gaussian function only in the ideal case.

In [20], a fully-programmable analog circuit for Gaussian function generator using switched-current (SI) technology was developed, the programmability being implemented and controlled by the clock frequency and by the transconductance ratios of SI filters. All of these efforts were made to fulfill aforesaid demand to realize Gaussian membership function.

A common disadvantage of the reported works is that most of the designed circuits operate in sub-threshold region. Although this technique leads to circuits offering low

power consumption, the dynamic range and the operation speed of the circuits turn out to be limited. Another disadvantage of the reported works is dependency of the circuit performances to the temperature variations, which in turn reduces the overall accuracy of the function.

In this paper, design of a high-precision CMOS circuit which realizes GF is fully described. Unlike the previous works, proposed circuits work on the saturation region, therefore high-accuracy as well as the high-speed performance are obtained. The current-mode circuits will be employed for the realization of main circuits owing to the simple circuitry and intuitive configuration.

The performance of the proposed circuit is characterized using HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35 μ m CMOS technology.

The paper is organized in 5 sections: The proposed method is discussed in section 2, followed by the transistor level design of the circuits in section 3. In section 4, HSPICE simulation results of proposed circuits are presented to prove the efficiency of the design. Finally, conclusions are outlined in section 5.

2. Gaussian Function and Design Consideration

The Gaussian Function (GF) is a non-linear bell-like transfer function which can be defined as:

$$f(x) = A \exp \left[-\frac{(x-\mu)^2}{2\sigma^2} \right] \quad (1)$$

where “ A ” represents the peak of the Gaussian curve, “ μ ” is the position of the

peak and the standard deviation of “ σ ” controls the full width at half maximum of the Gaussian curve. In order to implement this function two main functional circuits should be provided: Exponential Function Generator (EXPFG) circuit and Squaring (SQ) circuit. Both of these functions will be separately realized using CMOS circuits. In all of the designed circuits the bias current of I_B is defined and normalized to one. Design and compact integration of the circuits in a power efficient way will be thoroughly discussed in the following section.

3. Realization of Gaussian Function

According to eq. (1), EXPFG and SQ functions are the main building blocks of Gaussian function. A block diagram representation of this equation is depicted in Fig. 1. In the first step of design each functional circuit will be implemented, then by replacing in the proposed block diagram the desired output will be provided.

3.1 Current Squaring Circuit

Fig. 2 shows the current mode squarer circuit which is based on the dual trans-linear loop consists of transistors M5, M8, M10 and M12 [7]. Considering this loop we have:

$$\sqrt{I_{DS5}} + \sqrt{I_{DS8}} = \sqrt{I_{DS10}} + \sqrt{I_{DS12}} \quad (2)$$

Since the drain currents I_{DS5} and I_{DS8} are equal to a constant bias current, i.e., I_B , one can easily express the drain currents of M10 and M12 in terms of input and output currents as follows:

$$I_{DS10} = I_{out} + I_{in} + I_B \quad (3)$$

$$I_{DS12} = I_{out} - I_{in} + I_B \quad (4)$$

Substituting Eqs. (3) and (4) into (2) and taking the square of both sides, we have:

$$2\sqrt{I_B} = \sqrt{I_B + I_{out} - I_{in}} + \sqrt{I_B + I_{out} + I_{in}} \quad (5)$$

$$4I_B = 2I_B + 2I_{out} + 2\sqrt{I_B^2 + I_{out}^2 + 2I_B I_{out} - I_{in}^2} \quad (6)$$

By squaring both sides again, output current of the circuit can be written as:

$$I_{out} = \frac{I_{in}^2}{4I_B} \quad (7)$$

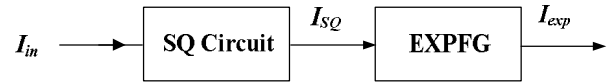


Fig. 1. Conceptual schematic of the Gaussian function circuit.

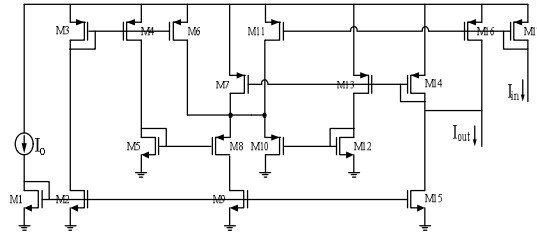


Fig. 2. Current-mode squaring circuit.

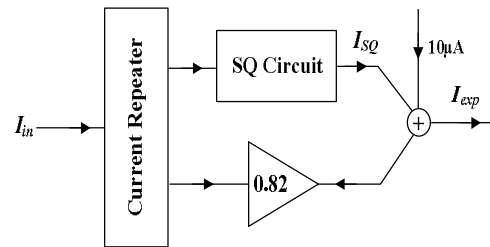


Fig. 3. Block diagram of the EXPFG circuit.

3.2 Exponential Function Generator Circuit

Two main approaches are basically introduced for the implementation of EXPFG circuit in saturation region.

The first method relies on realizing the exponential characteristic using the Taylor series expansion of the exponential function [21], [22] while the second one is based on a “pseudo-exponential” generator [23]. However, both of these approaches suffer from low-accuracy as well as the low-range operation.

In Ref. [25] another method has been presented based on the new approximation formula for the exponential function obtained by MATLAB using *linear least squares* method and *curve fitting* toolbox:

$$\exp(-x) \approx 0.19x^2 - 0.82x + 1 \quad 0 < x < 2 \quad (8)$$

Circuit realization of this equation is shown in Fig. 3. In this block diagram, first I_{in} is injected in a current repeater to produce two current signals with different scales which flow to the corresponding branches. The upper branch provides “ $0.19x^2$ ” while the bottom branch gives “ $0.82x$ ”.

Designing of circuits in the current-mode allow simple summation or subtraction of signals by applying in a low impedance node. Advantage of this approximation is that it is simple to implement because of using only “ x ” and “ x^2 ” terms which can be readily implemented by a current mirror and SQ circuit respectively.

3.3 Gaussian Function Generator Circuit

The complete schematic of proposed Gaussian function generator circuit based on SQ and EXPFG circuits is shown in Fig. 4.

It should be pointed out that this structure is designed in such a way that it has the ability of programming in terms of three parameters:

programmability of mean value using current source I_{μ} which is subtracted by I_{in} and then applied to the SQ circuit, the second parameter is the standard deviation programmability using different bias current which was considered in the SQ circuit, and finally the third programmable parameter is the peak gain of the function.

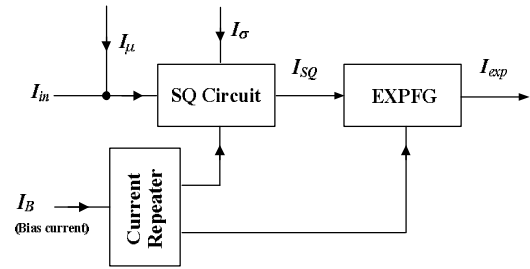


Fig. 4. Proposed structure for the programmable Gaussian function.

Considering the outputs of designed circuits, I_{SQ} and $I_{f(x)}$ can be expressed as:

$$I_{SQ} = \frac{(I_{in} - I_{\mu})^2}{I_{\sigma}} \quad (9)$$

$$I_{f(x)} = e^{-\frac{(I_{in} - I_{\mu})^2}{I_{\sigma}}} \quad (10)$$

4. Simulation Results

In this section, simulation results of the proposed circuit as well as the performance analysis are presented using HSPICE with TSMC level 49 (BSIM3v3) parameters for $0.35 \mu\text{m}$ CMOS technology so as to verify the performance of the circuit. For all of the simulations the bias current of I_B is equal to $10 \mu\text{A}$ and the supply voltage is 3.3 V .

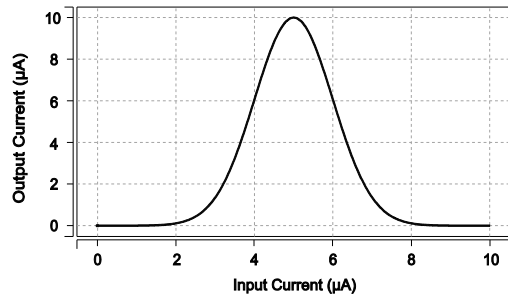


Fig. 5. Simulation result of the Gaussian function for typical value of programming parameters.

Fig. 5 shows the simulation result of the Gaussian function for a typical value for the parameters. Since the proposed circuit is programmable in terms of mean value, standard deviation and peak gain, therefore we will illustrate the programmability of the circuit for each of these parameter separately.

Fig. 6 shows the simulation result of the function for different mean values by changing I_{μ} . The simulation results in Figs. 7 and 8 demonstrate the programmability of the Gaussian function circuit in terms of standard deviation and peak gain respectively, in which standard deviation is programmed by I_{σ} , and peak gain can be programmed by I_B . Consequently, the proposed circuit can be easily programmed by the expert of the system via changing the corresponding current signals to create different shapes of Gaussian function.

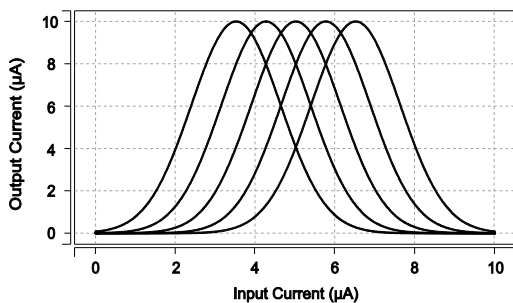


Fig. 6. Mean value programmability of the Gaussian circuit.

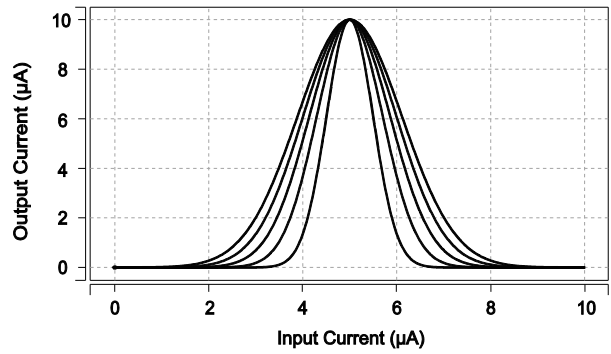


Fig. 7. Standard deviation programmability of the Gaussian circuit.

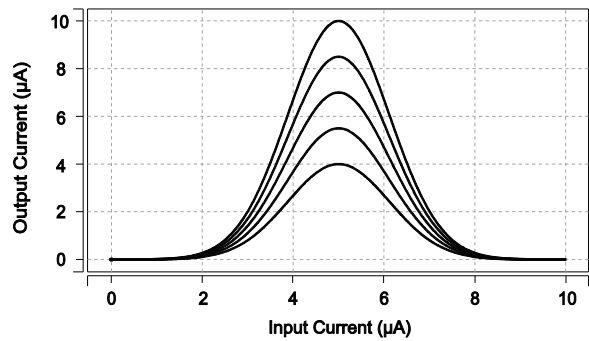


Fig. 8. Peak gain programmability of the Gaussian circuit.

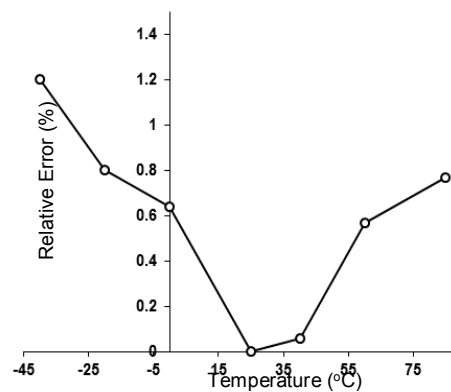


Fig. 9. Relative error of the Gaussian circuit versus different temperatures.

Table 1: Transistor Aspect Ratios

Transistor name	W/L ($\mu\text{m}/\mu\text{m}$)
M1, M2, M9, M15, M23, M30, M35	3.2/0.6
M7, M13, M14, M22, M24, M28	5.6/0.35
M3, M4, M6, M31, M32, M34	1/2
M16, M17, M19, M20	4/0.35
M5, M12, M25, M33	2/2.8
M8, M10, M26, M29	5.6/2.8
M11, M27	8/0.35
M18, M21, M36, M37	2/0.6
M38, M39, M40	3/0.5
M41, M42, M43, M44, M45	2/0.5

Fig. 9 is illustrated to prove the circuit performance regarding temperature variations. In this simulation, relative error versus different temperatures are computed. If we consider the temperature of 25 °C as a reference, other simulations in six temperatures are carried out and then compared with the reference temperature. In the worst case, relative error of 1.2% is occurred at -40 °C which exhibits an acceptable performance of the Gaussian function circuit with respect to temperature variations. Also the aspect ratios of the transistors in circuit of Fig. 2 is given in Table I.

5. Conclusion

The implementation of a current-mode Gaussian function circuit via CMOS transistors working in saturation region was presented. The proposed circuit was fully programmable in terms of mean value, standard deviation and peak gain of the

Gaussian function and could be readily programmed by the system expert. Simulation results of the circuits was obtained by HSPICE in 0.35 μm standard CMOS process which verified the feasibility of the circuit. The simulation results was shown that the circuit could be worked independent of the temperature variations.

References

- [1] R. Harjani, "A low-power CMOS VGA for 50 Mb/s disk drive read channels," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 6, pp. 370–376, Jun. 2019.
- [2] A. Motamed, C. Hwang, and M. Ismail, "A low-voltage low-power widerange CMOS variable gain amplifier," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 7, pp. 800–811, Jul. 2018.
- [3] C. Popa, *Synthesis of Computational Structures for Analog Signal Processing*, New York, USA: Springer-Verlag, 2020.
- [4] C. Popa, *Superior-Order Curvature-Correction Techniques for Voltage References*, New York, USA: Springer-Verlag, 2019.
- [5] A. Naderi, H. Mojarrad, H. Ghasemzadeh, A. Khoei and Kh. Hadidi : "Circuit Implementation of Programmable High-Resolution Rational-Powered Membership Functions in Standard CMOS Technology", *Eurocon 2009*, vol., no., pp.1236,1241, 18-23 May 2009.
- [6] A. Naderi, H. Mojarrad, H. Ghasemzadeh, A. Khoei and Kh. Hadidi : "Four-quadrant CMOS analog multiplier based on new current squarer circuit with high-speed," *EUROCON 2009, EUROCON '09. IEEE*, vol., no., pp.282, 287, 18-23 May 2009.
- [7] A. Naderi and S. Ozoguz, Design of high-linear, high-precision analog multiplier free from body effect, *Turkish Journal of Electrical Engineering and Computer Sciences*, in press 2013.
- [8] A. Naderi, Khoei A, Hadidi Kh, Ghasemzadeh H. A new high speed and low power four-quadrant CMOS analog multiplier in current mode. *AEU-Int J Electron*; 63: 769–775, 2009.

- [9] A. Kircay, M.S. Keserlioglu, U. Cam, A new current-mode square-root-domain notch filter, in: *Proceedings of the European Conference on Circuit Theory and Design*, pp. 229–232, 2022.
- [10] A. Naderi, A. Khoei, and Kh. Hadidi: “High Speed, Low Power Four-Quadrant CMOS Current-Mode Multiplier”, *Electronics, Circuits and Systems, ICECS. 14th IEEE International Conference on*, vol., no., pp.1308,1311, 11-14 Dec. 2007.
- [11] A. Naderi, and S. Ozoguz, “CMOS Design of a Multi-input Analog Multiplier”, *Ph.D. Research in Microelectronics and Electronics (PRIME), 2012 8th Conference on*, vol., no., pp.1,4, 12-15 June 2012.
- [12] A.N. Saatlo; S. Ozoguz, "A new CMOS exponential circuit with extended linear output range," *Circuit Theory and Design (ECCTD), 20th European Conference on*, pp.893,896, 2011.
- [13] G. Evans, J. Goes, A. Steiger, M.D. Ortigueira, N. Paulino, J.S. Lopes, Low-voltage low-power CMOS analogue circuits for Gaussian and uniform noise generation, *Int. Symp. Circuits Syst. 1*, I-145–I-148, 2023.
- [14] K. Basterretxea, J.M Tarela, I. del Campo, Digital Gaussian membership function circuit for neuro-fuzzy hardware, *Electron. Lett.* 42, 2021.
- [15] M.E. Pour, B. Mashoufi, A low power consumption and compact mixed-signal Gaussian membership function circuit for neural/fuzzy hardware, in: *Proceedings of the International Conference on Electronic Devices, Systems and Applications*, pp. 87–91, 2011.
- [16] J. Madrenas, M. Verleysen, P. Thissen, J.L. Voz, A CMOS analog circuit for Gaussian functions, *IEEE Trans. Circuits Syst.: Express Briefs*, 43, 70–74, 2016.
- [17] R. Srivastava, U. Singh, M. Gupta, Analog circuits for Gaussian function with improved performance, in: *Proceedings of the World Congress on Information and Communication Technologies*, pp. 934–938, 2017.
- [18] M Melendez-Rodriguez, J. Silva-Martinez, A fully-programmable temperature-compensated analogue circuit for Gaussian functions, *IEEE Int. Symp. Circuits Syst.* 5, 481–484, 2018.
- [19] C. Joongho, B.J. Sheu, J.C.F. Chang, A Gaussian synapse circuit for analog VLSI neural networks, *IEEE Trans. Very Large Scale Integr. VLSI Syst.* 2, 129–133, 2018.
- [20] C. Popa, “Improved Accuracy Pseudo-Exponential Function Generator with Applications in Analog Signal Processing”, *IEEE transactions on VLSI systems*, vol. 16, no. 3, 2022.
- [21] A. Carlos, De La Cruz Blas and Antonio López-Martín, “Novel Low-Power High-dB Range CMOS Pseudo-Exponential Cells”, *ETRI Journal*, vol. 28, no. 6, 2021.
- [22] B. Maundy and S. Gift, “Novel Pseudo-Exponential Circuits”, *IEEE transactions on circuits and systems*, vol. 52, no. 10, 2022.
- [23] A. Naderi, A. Khoei and Kh. Hadidi : “Circuit Implementation of High-Resolution Rational-Powered Membership Functions in Standard CMOS Technology”, *International Journal of Analog Integrated Circuits and Signal Processing*, vol. 65, no. 2, 217-223, 2010.