A novel Asymmetric Cascade Multilevel Inverter with Reduced Components and the Ability of Using Intelligent Control Methods

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Abstract

One of the most famous algorithms in the field of focused exploration of data mining correlation rules is the Apriori algorithm and its many developed versions. But what can be raised as a major challenge in this field is the proper application of this algorithm in the distributed environments of today's world. In this research, a parallelization-based approach is proposed to improve the performance of the Apriori algorithm in the process of exploring recurring patterns on network topologies. The proposed approach includes two major features: (1) combining the node centrality criterion and the Apriori algorithm to identify frequent patterns, (2) using the mapping/reduction method in order to create parallel processing and achieve optimal values in the shortest time. Also, this approach pursues three main goals: reducing the temporal and spatial complexity of the Apriori algorithm, improving the process of extracting dependency rules and identifying recurring patterns, comparing the performance of the proposed approach on different network topologies in order to determine the advantages and disadvantages of each topology. To prove the superiority of the proposed method, a comparison has been made between our approach and the basic Apriori algorithm. The evaluation results of the methods prove that the proposed approach provides an acceptable performance in terms of execution time criteria compared to other methods.

Keywords: :Asymmetric cascaded multilevel inverter, Cascaded multilevel inverter, Symmetric cascaded multilevel inverter.

1. Introduction

Over the last five decades, the attractive features of multilevel inverters have led to their widespread use in ac motor drives, high voltage direct current (HVDC) systems, reactive power compensators, electric vehicles (Evs), renewable energy conversion systems and other medium-high applications. Among these features, we can mention the increase of power quality, high voltage gain, improvement of waveform quality, reduction of filter size and power loss [1, 2]. The most common multilevel are: neutral-point-clamped (NPC) [3], flying capacitor (FC) [4] and CHB multilevel inverters [5]. Meanwhile, NPC multilevel use a large number of clamping diodes, the voltage balance of the capacitors in the FC multilevel is difficult and CHB multilevel need a large number of components. Nevertheless, due to the simplicity of the structure and control methods, CHB multilevel has attracted the attention of researchers to improve this structure and to reduce the number of components used [6-8]. As mentioned, one of the disadvantages of cascaded multilevel inverters is the use of a large number of power electronic components to produce voltage levels at the output. Researchers have focused their efforts on improving this defect [9-25]. The structures described in [10-14] alone produce positive voltage levels at the output and have used an H-bridge to produce

negative levels. The voltage drop on H-Bridge switches is very high, and this leads to an increase in the voltage drop of all switches, and as a result, the value and price of inverters increases. The dc voltage sources used in symmetrical topologies in [14,15] have the advantage of having the same value, and their cost and sizes are low and improve reliability, but they do not have the possibility of implementing asymmetrical topologies and the total blocking voltage on their switches is high. In the structures presented in [12,13,16,17,20,23], both symmetric and asymmetric topologies have been implemented and the switches used in [10,12] are unidirectional and bidirectional. In the structures [12,13,18-20,23,25], first the basic structure is introduced and then to produce more voltage levels in the output, several basic structures are connected together and multilevel inverters have been created. This method makes it possible to expand the number of output voltage levels without increasing the complexity of the circuits and reduce the design cost of the controller. Algorithms presented in them are a method to produce odd and even levels and reduce the blocking voltage in the switches. The number of components used in the structures [21,23-25] is high and causes the high cost and complexity of their control. However, the structure presented in [22], despite using a lowest number of dc voltage sources, also uses capacitors, which causes the difficulty of their voltage balance.

First, in this paper, the basic unit is introduced and then to produce more voltage levels several basic units are connected together and cascade inverter topology with ability of using different kinds of intelligent control methods is created. In the next section, the necessary algorithm to determine the value of the dc voltage sources is discussed and then compared with other structures to evaluate the benefits of the proposed inverter. Finally, the detailed performance of the proposed 15-level inverter is discussed using with PSCAD/EMTDC software program.

2. Proposed Basic Multilevel Structure

Fig.1, shows the proposed basic structure for the 15-level multilevel, which consists of seven unidirectional switches (each switch comprises of an antiparallel diode and an IGBT), six bidirectional switches (each switch comprises of two antiparallel diode and two IGBTs) and three independent dc voltage sources V_1, V_2 and V_3. For the correct operation of the structure and to prevent the output from being short circuited, the switches i.e. S_1 and S_2 cannot be turned on simultaneously. Table 1, shows the switching states for this structure, where 0 and 1 represent the off and on states of the switches, respectively.

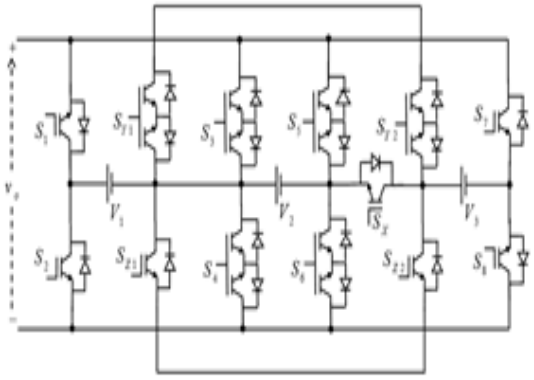


Fig. 1. Proposed basic 15-level multilevel

According to this table, the maximum magnitude output voltage produced is equal to . In order to prevent the production of repeated output voltage levels and to have the largest number of levels, the magnitude of the dc voltage sources are considered as follows:

$$V_1 = V_{dc} \quad (1)$$

$$V_2 = 2V_{dc} \quad (2)$$

$$V_3 = 4V_{dc} \quad (3)$$

3. Proposed Cascaded Multilevel Inverter Structure

In order to obtain the maximum number of voltage levels at the output, the proposed basic structure is expanded and a proposed cascaded multilevel inverter is formed with n independent dc voltage sources (Fig. 2). To control the proposed multilevel inverter, it is possible to use different control methods. Considering the number of used switches and switching table and noticing the application, to control the on and off states of switches for generating the desired of output voltage it is possible to use not only the different kinds of pulse width modulation (PWM) methods but also we can use different kinds of intelligent control methods. Although, in this paper the fundamental frequency control method is used to control of the proposed multilevel inverter. $N_{variety}$ shows the number of variety of dc voltage sources used for proposed asymmetric multilevel inverter, which is calculated from the following equation:

$$N_{Variety} = n \quad (4)$$

4. Determination of the Magnitude of dc Voltage Sources

Quantification and proper determination of dc voltage sources is another important and effective way to obtain the maximum number of output voltage levels and prevent the production of duplicate levels in multilevel. Therefore, the following algorithm is considered to have the highest output voltage levels of the proposed asymmetric multilevel inverter, so that the number of dc voltage sources is n

$$V_1 = V_{dc} \quad (5)$$

$$V_2 = 2V_{dc} \quad (6)$$

$$V_3 = 2^2 V_{dc} \quad (7)$$

$$V_n = 2^{(n-1)} V_{dc} \quad (8)$$

Considering the mentioned algorithm, the following relationships for proposed cascaded multilevel inverter structure is obtained:

$$N_{IGBT} = 8n - 5 \quad (9)$$

$$N_{source} = n \quad (10)$$

$$N_{driver} = 5n - 2 \quad (11)$$

$$N_{step} = 2^{n+1} - 1 \quad (12$$

$$V_{o,\max} = (2^n - 1)V_{dc} \quad (13)$$

So that N_{IGBT} , N_{source} , N_{driver} and N_{step} specifies the number of IGBTs, dc voltage sources, gate driver circuits, output voltage levels and $V_{o,\max}$ is the largest output voltage value produced by the cascaded multilevel.

5. Comparison Results

To confirm the performance of the proposed asymmetric multi-level inverter, a comparison has been made between it and other structures. Fig.3, compares the number of IGBTs, gate driver circuits and dc voltage sources against the number of output voltage levels. The result of

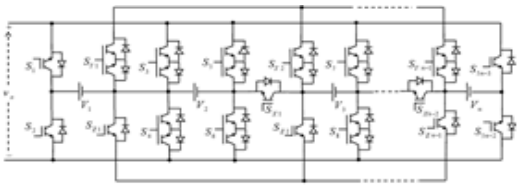


Fig. 2. Proposed cascaded multilevel inverter

this comparison shows that, the proposed asymmetric multilevel inverter structure has the lowest number of IGBTs and dc voltage sources compared to other structures for output voltage levels over 40. According to Fig.3(c), to produce equal voltage levels, the proposed asymmetric multilevel inverter uses more dc voltage sources than structure in [22], but less dc voltage sources than other structures. Table 2. shows the number of power electronic components of different structures to produce 61 output voltage levels. The results of this table confirm the previous results.

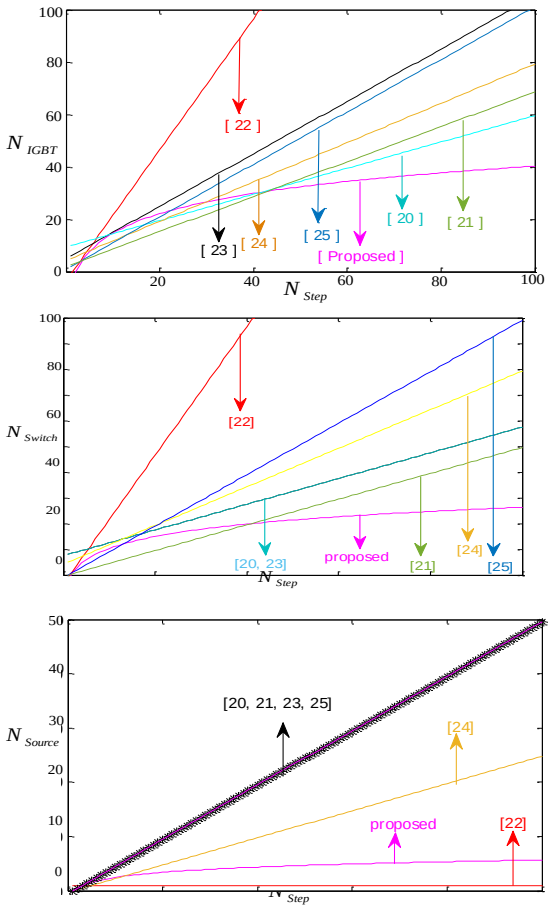


Fig. 3. Comparison results (a) N_{IGBT} (b) N_{source} (c) N_{driver} versus N_{step}

6. Simulation Results of Proposed 15-level Inverter

In confirmation of the performed calculations, the 15-level multilevel inverter is simulated with the help of the PSCAD / EMTDC software. This structure consists of seven unidirectional and six bidirectional switches, 19 IGBTs, 13 gate driver circuits and three dc voltage sources with values of 10V, 20V and 40V for V_1, V_2 and V_3, respectively, for $n=3$. R-L load is considered with values of 50Ω and 55mH for resistance and inductor, respectively. The proposed inverter is controlled by the basic fundamental frequency switching method with 50Hz. It is important to note that it is possible to use different kinds of the intelligent control methods. The output voltage and current waveform is shown in Fig. 4. The presence of the R-L load causes the sinusoidal nature of the load current of the multilevel inverter and acts as a low-pass filter for the current. Fig. 5 shows the voltage on the switches of $S_1, S_2, \ldots, S_8, S_X, S_{Y1}, S_{Y_2}, S_{Z1}, S_{Z2}$. The positive and zero voltage amplitude of the switches indicate that they are unidirectional, and the positive and negative voltage amplitude of the them indicate that they are bidirectional. THD of output current and voltage according to simulation is equal to 0.64% and 3.29% respectively. According to the waveform of the output current (Fig. 4 -b) and the THD value of the current, it is clear that the load current is almost sinusoidal and without high-order harmonics, and the reason for this is the presence of the R-L load, which acts as a low-pass filter for the current.

Table 1. Switching states of proposed basic unit

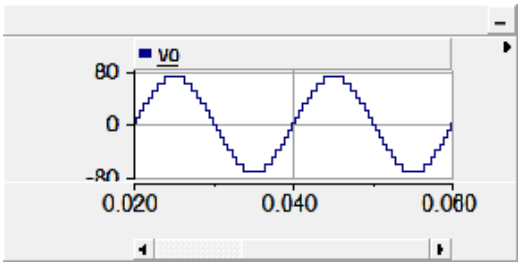
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_X	S_{Y1}	S_{Y2}	S_{Z1}	S_{Z2}	v_o
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	V_1
0	0	1	0	0	1	0	0	0	0	0	0	0	V_2
1	0	0	0	0	1	0	0	0	0	0	0	0	V_1+V_2
0	0	0	0	1	0	0	1	1	0	0	0	0	V_3
1	0	0	0	0	0	0	1	0	1	1	0	0	V_1+V_3
0	0	1	0	0	0	0	1	1	0	0	0	0	V_2+V_3
1	0	0	0	0	0	0	1	1	0	0	0	0	$V_1+V_2+V_3$
0	1	1	0	0	0	0	0	0	0	0	0	0	$-V_1$
0	0	0	1	1	0	0	0	0	0	0	0	0	$-V_2$
0	1	0	0	1	0	0	0	0	0	0	0	0	$-(V_1+V_2)$
0	0	0	0	0	1	1	0	1	0	0	0	0	$-V_3$
0	1	0	0	0	0	1	0	0	0	0	1	1	$-(V_1+V_3)$
0	0	0	1	0	0	1	0	1	0	0	0	0	$-(V_2+V_3)$
0	1	0	0	0	0	1	0	1	0	0	0	0	$-(V_1+V_2+V_3)$

Table 2. Comparison of the proposed structure inverter with other reference structures for producing 61-level

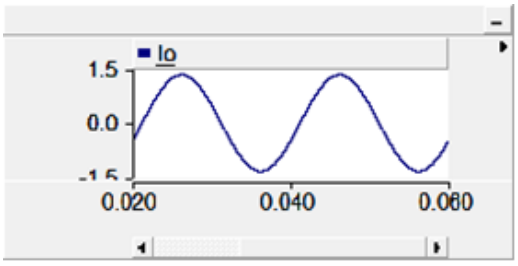
parameters	[20]	[21]	[22]	[23]	[24]	[25]	**proposed structure**
N_{level}	61	61	61	61	61	61	**61**
N_{IGBT}	40	43	149	66	50	62	**35**
N_{source}	30	30	1	30	15	30	**5**
N_{driver}	38	28	149	38	50	60	**23**
$N_{capacitor}$	0	0	29	0	15	0	**0**
N_{diode}	0	0	0	0	0	0	**0**

Conclusion

In this paper, a new basic unit for cascaded multilevel inverter is proposed, which is asymmetrically configured and capable of producing negative and positive voltage levels at the output. To produce a greater number of output voltage levels, the basic unit is expanded. The proposed topology can be controlled by different control methods such as PWM methods and intelligent control methods. Comparing the proposed structure with other structures shows that the proposed structure uses fewer switches and dc voltage sources.

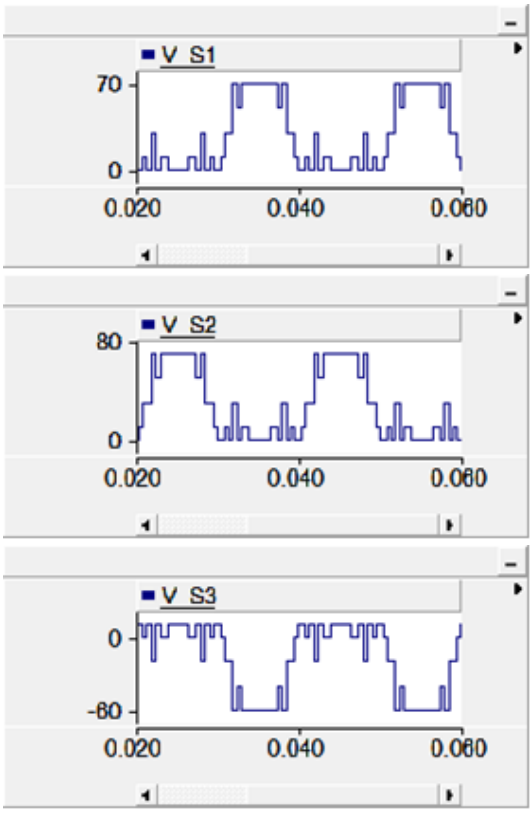


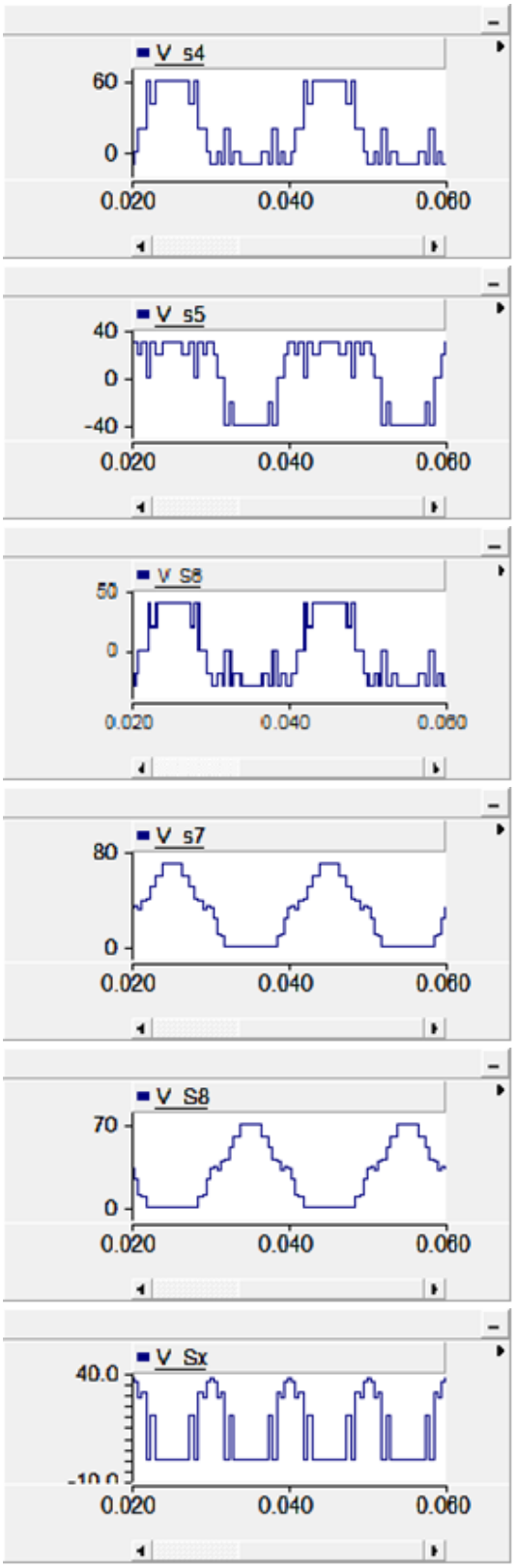
(a)



(b)

Fig. 4. output (a) voltage (b) current waveforms for 15-level cascaded





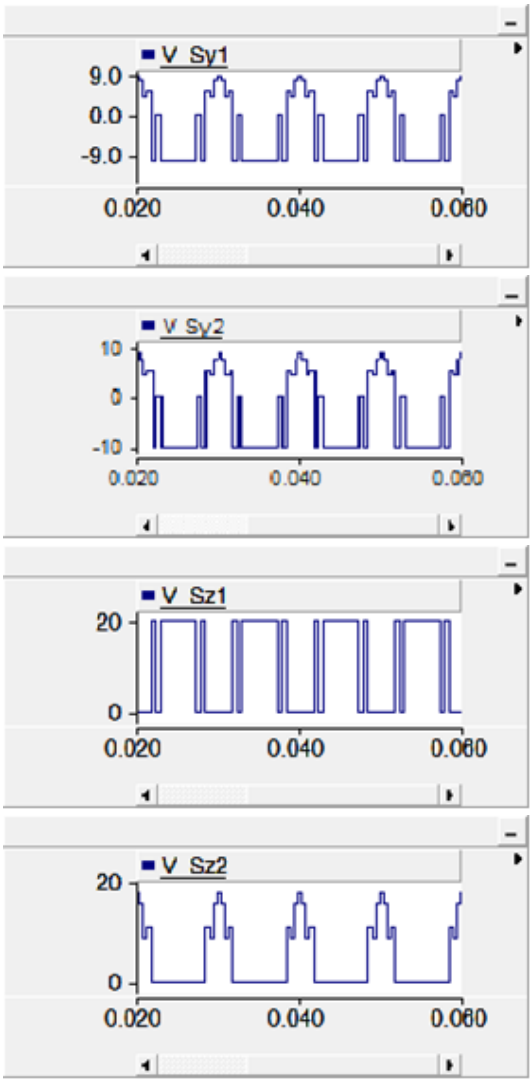


Fig. 5. Voltage waveforms for different switches in the simulation

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