A New Coplanar Full Adder/Subtractor in Quantum-Dot Cellular Automata Technology

Mohsen Vahabi [1*], Amir Sabbagh Molahosseini [2]
1- Department of Electrical Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran.
Email: mohsen.vahabi@iauk.ac.ir (Corresponding author)
2- Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran.
Email: Sabbagh@iauk.ac.ir

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ABSTRACT:
The conventional CMOS technology faces different challenges such as fabrication in nanoscale which motivates researchers to find new alternatives to it for future high-performance systems. The quantum-dot cellular automata (QCA) is one of efficient nano-electronics technologies which can provide simple and efficient implementation of digital circuits in nanoscale. Due to the importance of addition in digital processors and embedded systems, there many QCA designs of adders and subtractors during the previous years. However, recently the unified design of adder and subtractor circuits has been considered to achieve overall area and delay reduction for digital computational circuits. In this paper, we present new coplanar design of a unified adder/subtractor unit with the QCA technology. Besides, the proposed single-layer design approach has been used to design separate half adder, half subtractor, half adder and full adder circuits. The comparison of circuit's parameters of the proposed designs than previous works show the significant improvement in term of area, delay and cell number.

KEYWORDS: Quantum-dot Cellular Automata, Full Adder/Subtractor, Coplanar (single layer).

1. INTRODUCTION

QCA technology, with its unique features such as small dimensions, high speed, low latency, and low power consumption, as a new method of communication and computing, is one of important technologies that is considered as an alternative to the conventional complementary metal oxide semiconductor (CMOS) technology and is used to sustain the economy of scale by the continuity of this device miniaturization trend in Digital Signal Processing applications [1]. On the other hand, adders which are one of the most fundamental computational circuits of many VLSI systems, such as microprocessors and processors, have been attracted considerable research attention. Designing full adder (FA) with a simple structure and limited power consumption can play a vital role in achieving high-performance digital circuits. Also, the design of full Adder/full Subtractor as a composite circuit has particular importance. Among the problems involved in the design of circuits and compound cells, efficient design of wiring intersection is the best to improve circuit parameters.

The multi-layer design of QCA circuits, due to imposing high cost and increasing the area of the circuit, is not desirable for nowadays high-performance applications [2], [3]. Besides, in order to achieve the intersection of the parallel wires, a 45-degree QCA cell rotation has been used, due to the coexistence of two types of QCA cells with problems such as low strength and high implementation cost. Therefore, design with the use of this type of cells is also not efficient [2], [4]. However, recently, a single cell type, using only non-porous clock phases (4 phase phases), is used to design the intersection of single-layer passing wires [2], [5]. We have to design the proposed single-layer full adder/subtractor circuit with the reduced number of consumed cells and small used area together with low latency in compare with the previous works.

The rest of the paper is organized as follows. In Section 2 (background), an overview of QCA and previous work is presented. In Section 3 (proposed work), the architecture of the proposed circuit is presented. In Section 4 (simulation output and comparison of results), we compared the proposed design with previous architectures. In Section 5 (Conclusion), we conclude the paper.

2. BACKGROUND

2.1. Quantum-dot Cellular Automata (QCA)

This technology is based on quantum cells where each cell can display a logical bit, i.e. "0" and "1", with

the electrons position. A QCA cell consists of two electrons, which are based on the columbic repulsion created between them. QCA cells are represented in the square design, and each cell consists of four holes. There are two electrons inside each cell which are enclosed and can move freely between the holes. By placing two electrons in four cavities, six different states are created, which is not possible due to the presence of a coulomb force between electrons, and these two electrons are always in the position that they have the greatest distance from each other. Consequently, in order to consistent with this rule, the electrons are placed in the holes in the diagonal, which are the most spaced apart due to rule of thumb for Columbia. By placing electrons in a diameter, two structures are created. We can associate these two polar structures +1 and -1 with the logical values of "1" and "0", respectively as shown in Fig.1.

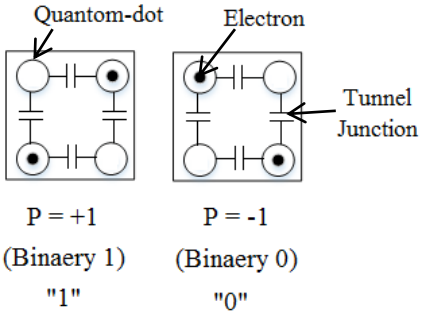

Fig. 1. QCA Cells Structure [2].

When electrons move inside the cell, they tunnel through the holes, which is the movement of the electrons into the cell as a nonlinear motion. The columbic repulsion force does not exist between the electrons within a cell, but as shown in the Fig. 2, each cell from the adjacent cell affects the next adjacent cell [6-8].

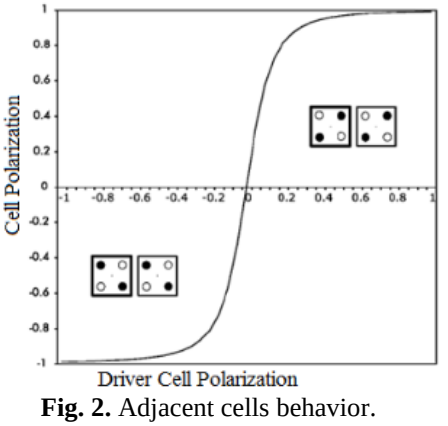

Fig. 2. Adjacent cells behavior.

2.2. Four-phase QCA

The four phases of the QCA clock are shown in Fig. 3. It can be seen that the potential barriers are rising during the first phase of the clock (Switch). At the beginning of this phase, the barriers are low, and the QCA cell is in an unpolarized state, and the cell is given from its surrounding cells under a columbic force. Then, with increasing barriers, the QCA cells are polarized according to their input drive states, and at the end of this clock phase, barriers are high enough to prevent electron tunneling; thus, the cell is locked, and real switching occurs. During the second phase of the clock (Hold), the barriers remain high. In this phase, the cell is completely stable and transmits its data to the surrounding cells. During the third phase of the clock (Release), obstacles go down and the cell becomes unstable. During the other phase, intracellular data is not needed, and the cell is allowed to polarize (unpolarized) to go to the Relax state. During the fourth relaxation phase (Relax), cell barriers remain at the lowest level, and cells remain in the unpolarized state. In fact, in this phase, the cell is not used. At the end of this phase, the cell re-enters the switch's phase [3, 9].

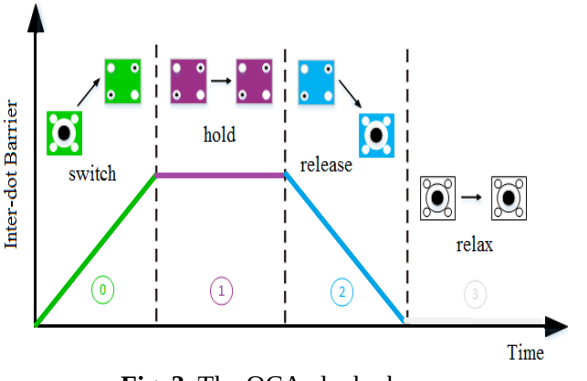

Fig. 3. The QCA clock phases .

2.3. Basic Gates with QCA

Not gate is one of the most commonly used gates, which is also needed in QCA technology. In order to invert the desired signal, one of the inversion gates shown in Fig. 4 can be used in different applications [10], [11].

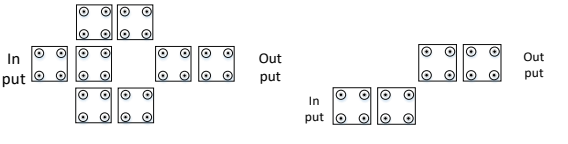

Fig. 4. Not Gate in QCA.

Another important gate in QCA technology is the majority gate. This gate has three inputs and the output, where the majority of inputs determine the output value. As a result, the polarization and the output is controlled by the majority of input values [8, 10]. Fig. 5 shows an example of this gate, and its relationship is as

follows

$$M(A, B, C) = A.B + A.C + B.C \quad (1)$$

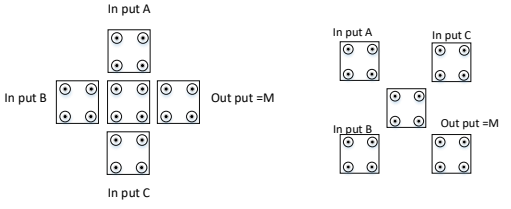

Fig. 5. The QCA majority Gate.

The majority gate can be used as AND gate, by fixing one of its entries to the "0" (polarization-1) [10], [12]. Fig. 6 shows the AND gate with two inputs. The relationship (2) represents the logical relationship of this gate.

$$A \cdot B = M(A,B,0) \quad (2)$$

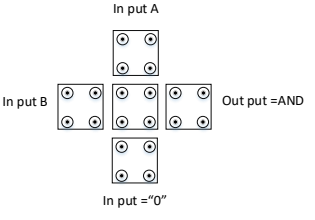

Fig. 6. AND Gate with two inputs.

Moreover, OR gate can be designed by fixing one of the majority gate's entries to the "1" value (polarization + 1) [10], [12]. This OR gate is shown in Fig. 7, and its relation is as follows

$$A + B = M(A,B,1) \quad (3)$$

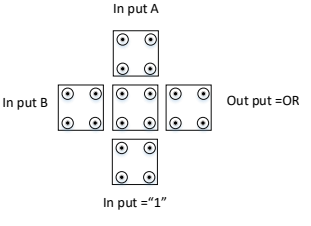

Fig. 7. OR gate with two inputs.

2.4. Literature Review

Different QCA based structures have been introduced for half and full adders. In this part, some of them are investigated. One of these structures is shown in Figs. 8 and 9 [13]. Besides, the architecture of a coplaner full adder (Fig. 10) is introduced in [14] with the use of an efficient intersection. In [15], the architecture of a full Subtractor (Fig. 11) has been presented. Moreover, the full Adder/full Subtractor circuit architecture is presented in [16], which is a multilayered design. In [17], the design of half adder, half- Subtractor, full adder and full Subtractor circuits (Figs. 12-15) is presented.

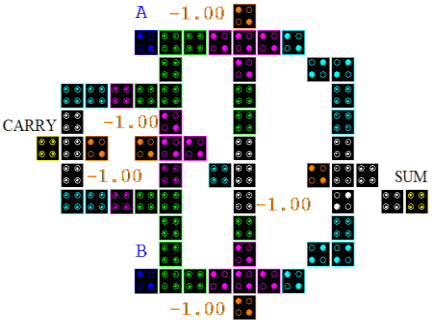

Fig. 8. Half-adder circuit [13].

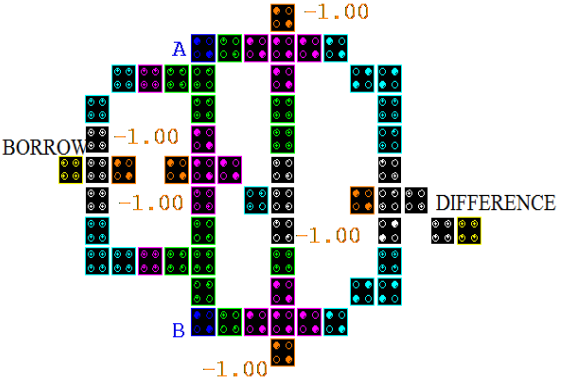

Fig. 9. Half-Subtractor circuit [13].

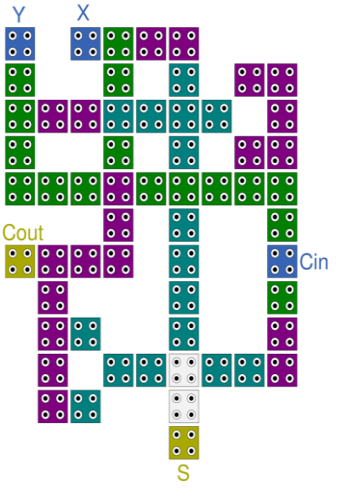

Fig. 10. Full-adder circuit [15].

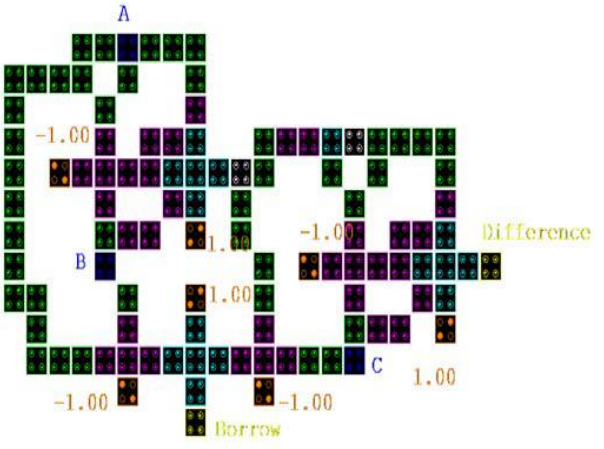

Fig. 11. Full-Subtractor collector circuit [14].

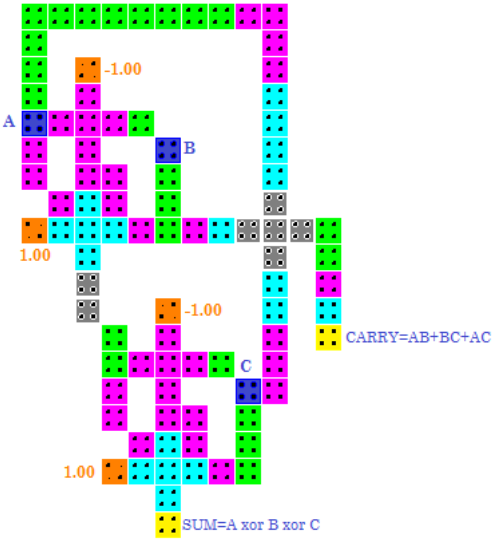

Fig. 12. Full-adder circuit [17].

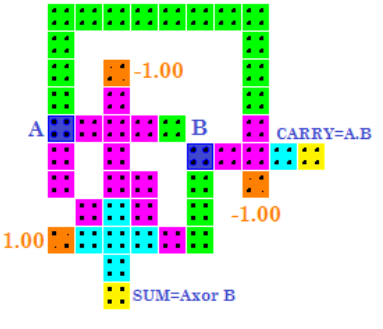

Fig. 13. Half-adder circuit [17].

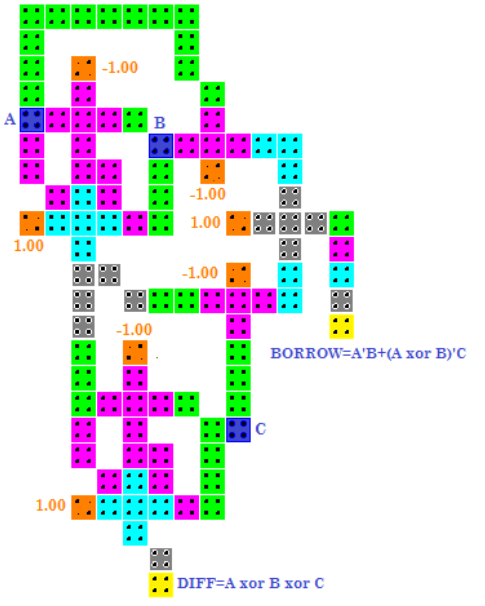

Fig. 14. Full- Subtractor Circuit [17].

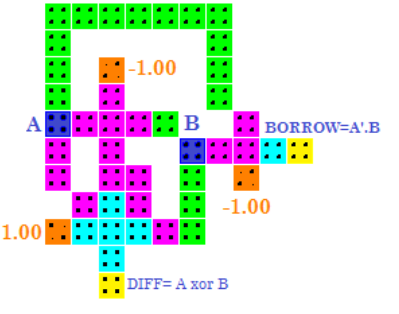

Fig. 15. Half- Subtractor Circuit [17].

3. PROPOSED CIRCUITS

In this paper, we propose new half-adder (HA), half Subtractor (HS), FA, full Subtractor (FS), and full adder/subtractor (FA/S) circuits based on the effiecient XOR gate introduced in [19]. In all designs, one-layer design has been considered.

3.1. Proposed Half Adder circuit

The proposed adder is depicted in Figs. 16 and 17, and just relies on one layer; results in an efficient design with significant area and delay reduction.

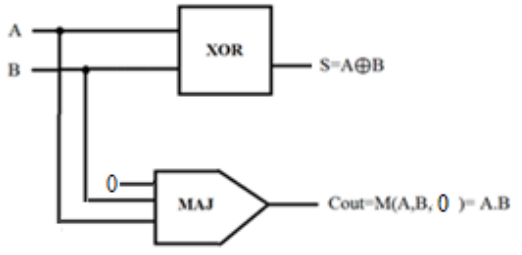

Fig. 16. Block diagram of the proposed Half-Adder circuit.

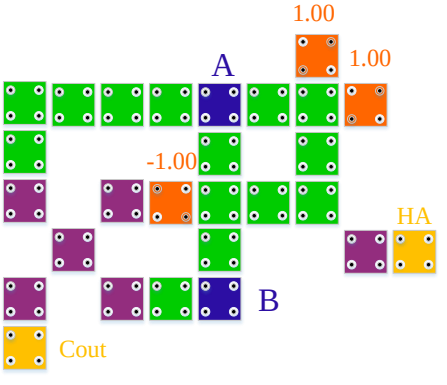

Fig. 17. The proposed Half-Adder circuit.

3.2. Proposed Half Subtractor circuit

Figs. 18 and 19 show the proposed half Subtractor circuit. It can be seen that it is just implemented in single layer.

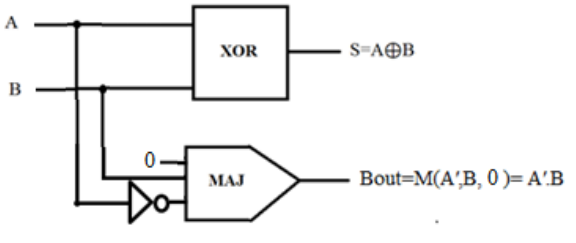

Fig. 18. Block diagram of the proposed Half-Subtractor circuit.

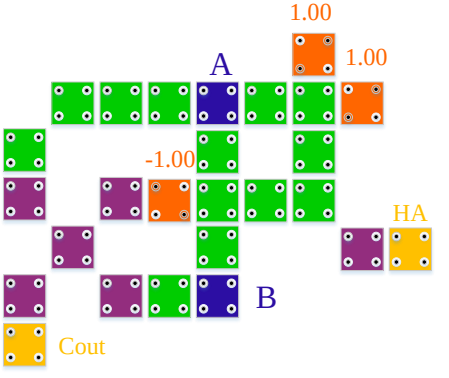

Fig. 19. Proposed Half Subtractor Circuit.

3.3. Proposed Full Adder circuit

Fig. 20 presents the block diagram of the proposed single-layer Full Adder while its QCA implementation is shown in Fig. 21.

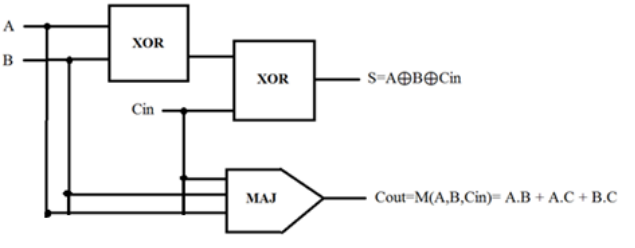

Fig. 20. Block diagram of the proposed Full Adder.

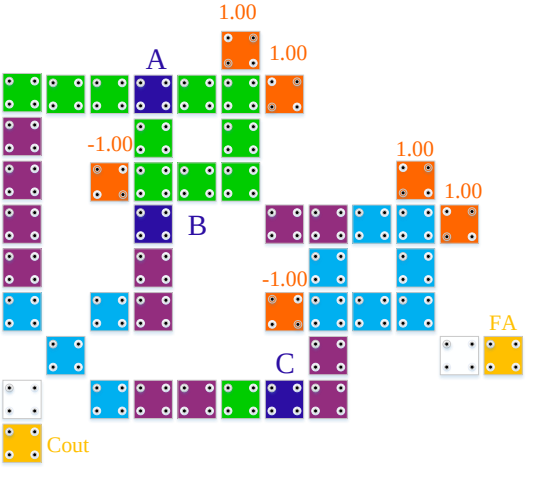

Fig. 21. The proposed QCA Full Adder.

3.4. Proposed Full-Subtractor circuit

The proposed Full Subtractor Circuit is shown in Figs. 22 and 23. one of the finest samples ever designed. It is only implemented in single layer.

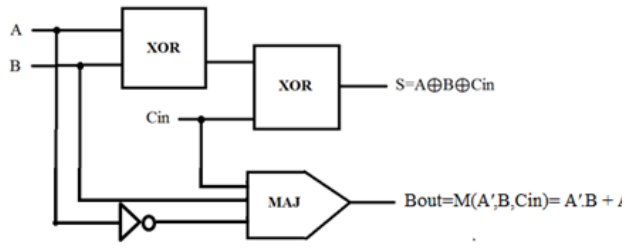

Fig. 22. Block diagram of the proposed Full Subtractor.

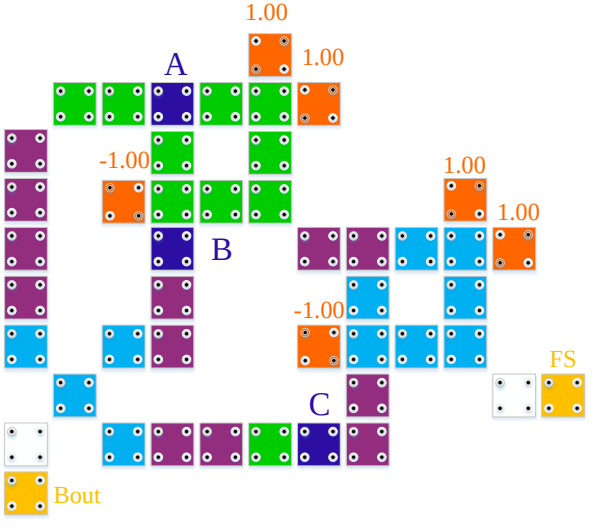

Fig. 23. The proposed QCA Full Subtractor .

3.5. Proposed Full Adder/Full Sabtractor circuit

An Full Adder/Full Sabtractor circuit is a combinatorial circuit that performs addition and subtraction operations. This circuit has three inputs (A, B, Cin) and three outputs (S\D, Cout, Bout) [20], [21]. relationships show the formulas related to the outputs of this circuit. The Fig. 24 shows the block diagram and Table 1 presents the correct table of this circuit.

$$S\backslash D = A \oplus B \oplus Cin \quad (4)$$

$$Cout = M(A,B,Cin) = A.B + A.C + B.C \quad (5)$$

$$Bout = M(A',B,Cin) = A'.B + A'.C + B.C \quad (6)$$

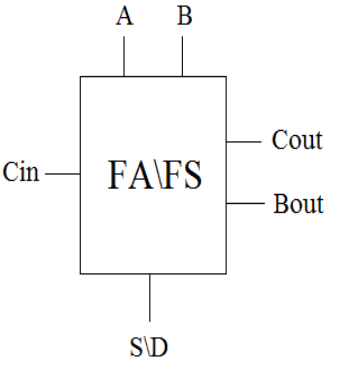

Fig. 24. Block diagram for FA/S circuit.

Table 1. Accuracy Table of Full Adder/ Subtractor circuit.

A	B	Cin	S\D	Cout	Bout
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

In this paper, we focus on designing a FA/S circuit with the lowest number of cells, less area and lower latency than the best of the previous designs. In the proposed design, the single layer has been considered. Fig. 25 shows the block diagram, and Figs. 26-a and 26-b present the QCA Implementation of the Full-Adder /Full-Subtactor circuit. Besides, Figs. 31 and 32 represent the output of the simulator for these circuits.

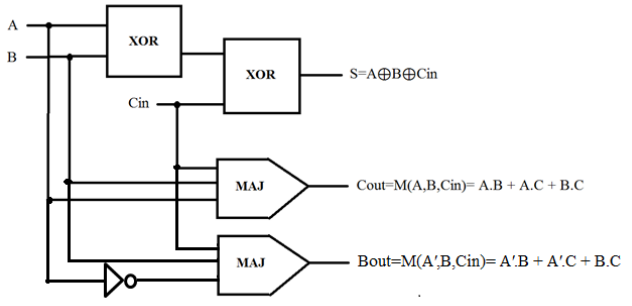

Fig. 25. Block diagram of the proposed Full Adder / Full Subtractor circuit (FA \ FS).

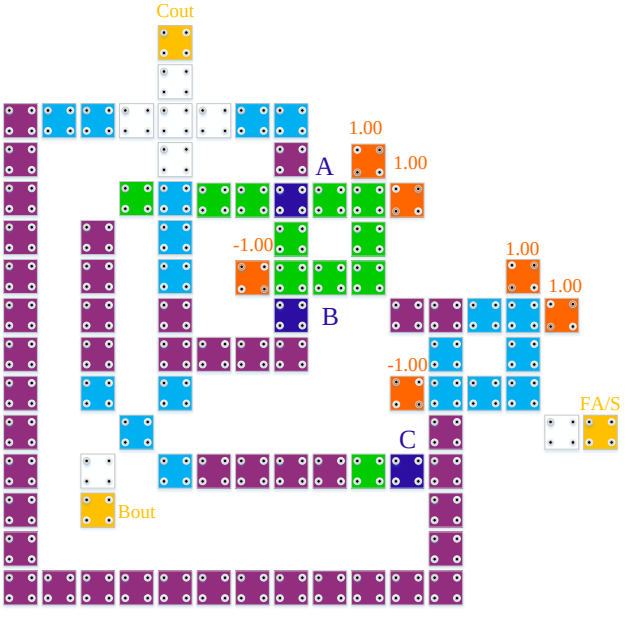

Fig. 26-a. The proposed Full Adder/Subtractor (FA /S) circuit.

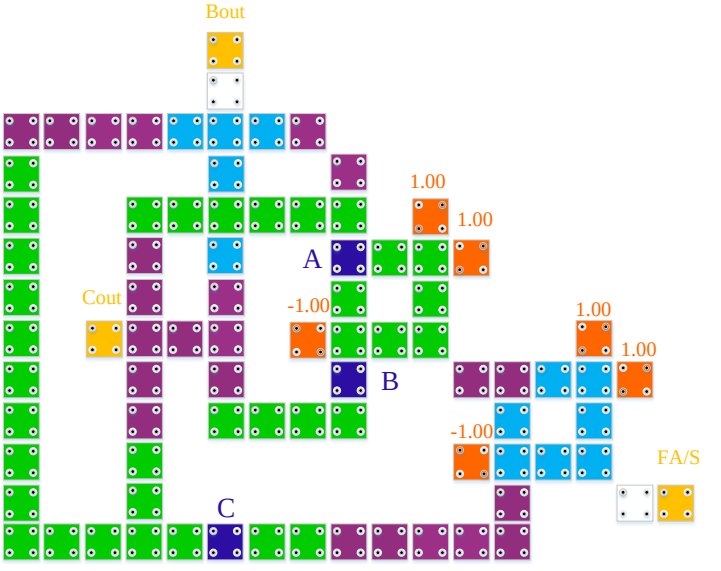

Fig. 26-b. The proposed Full Adder/Subtractor (FA /S) circuit.

4. SIMULATION RESULTS

In this section, the QCA Designer tool has been used to simulate all the proposed designs, and the result are depicted in the Figs. 27-32. Besides, Table 2 and Figs. 33-35 compare the proposed circuits than previous related designs.

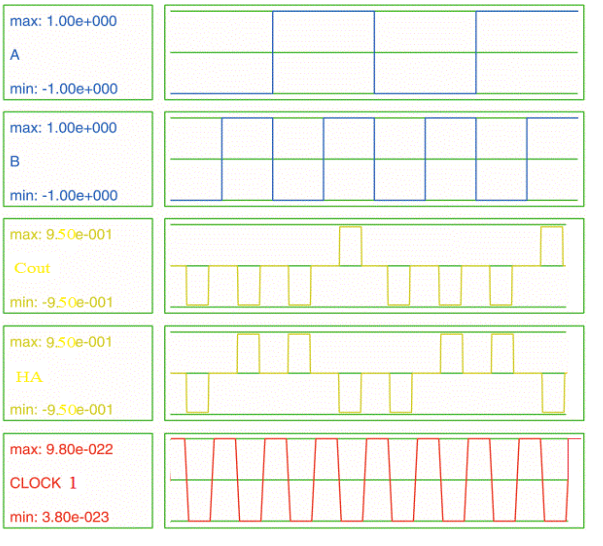

Fig. 27. Simulation result of the proposed Half Adder.

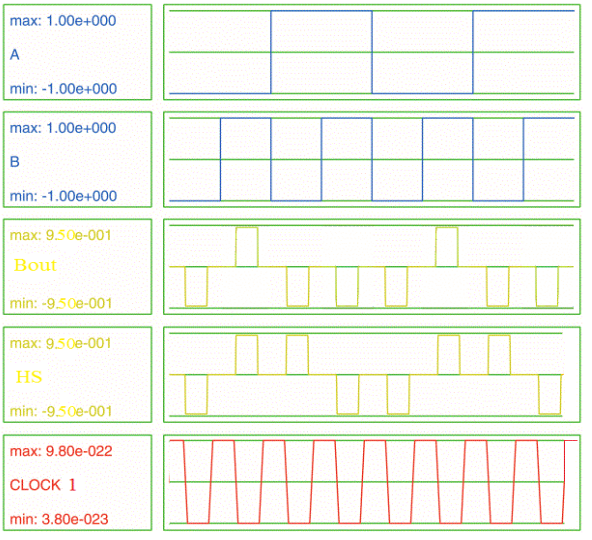

Fig. 28. Simulation result of the proposed Half – Subtractor.

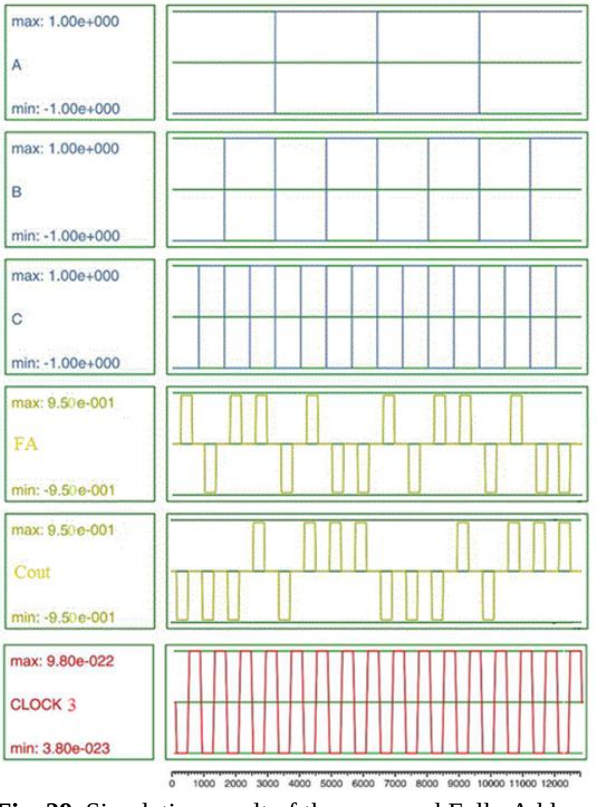

Fig. 29. Simulation result of the proposed Full –Adder.

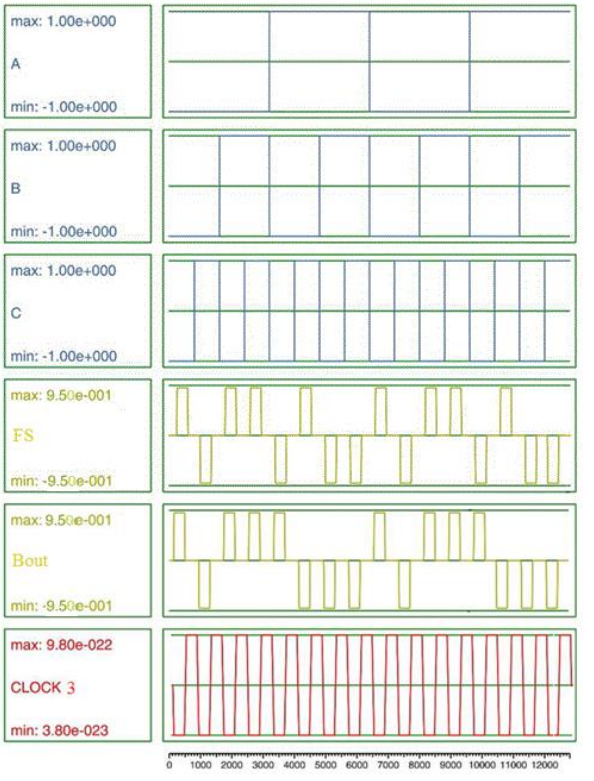

Fig. 30. Simulation result of the proposed Full – Subtractor.

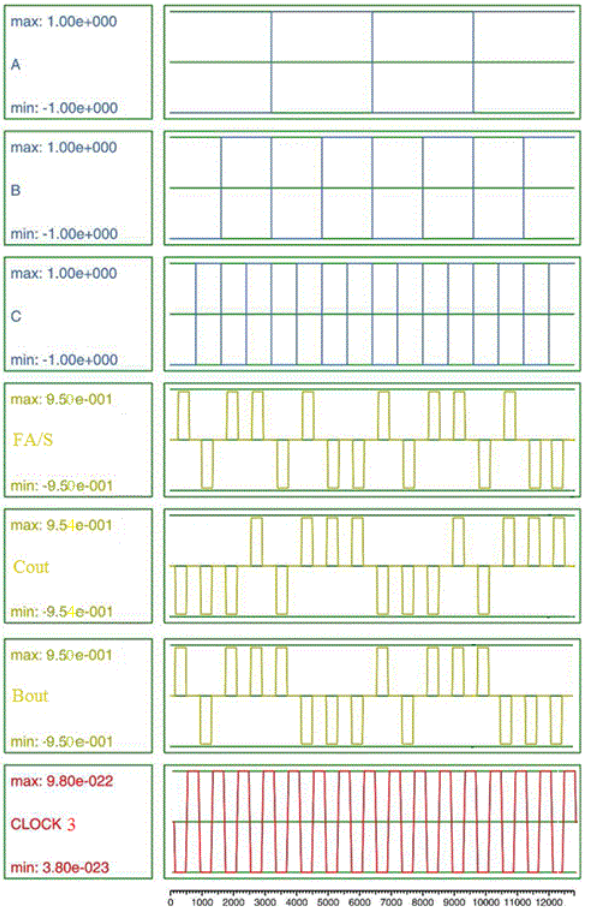

Fig. 31. Simulation result of the proposed Full Adder/Subtractor in Fig. 26-a.

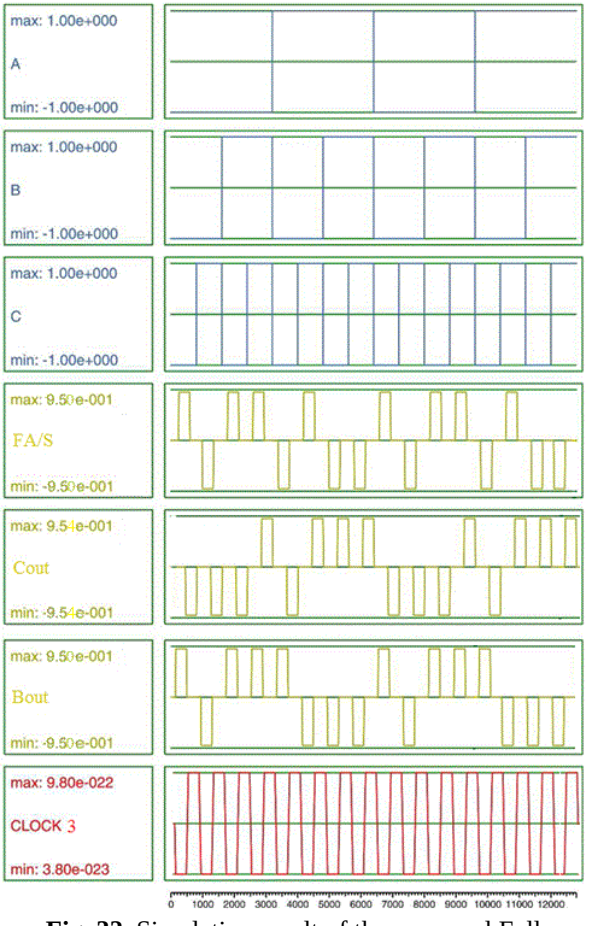

Fig. 32. Simulation result of the proposed Full Adder/Subtractor circuit in Fig. 26-b.

Table 2. Comparison of Circuit's Parameters for different Designs

Circuit	Area (um^2)	Cell count	Latency (Clock cycle)	Layer Type
Half Adder	0.03	27	0.5	Coplanar (clocking based)
[13]	0.08	62	2	Coplanar (clocking based)
[17]	0.035	46	0.75	Coplanar (clocking based)
Half Subtractor	0.03	26	0.5	Coplanar (clocking based)
[13]	0.08	62	2	Coplanar (clocking based)
[17]	0.035	45	0.75	Coplanar (clocking based)
Full Adder	0.05	47	1	Coplanar (clocking based)
[13]	0.043	59	1	Coplanar (clocking based)
[17]	0.073	90	2	Coplanar (clocking based)
Full Subtractor	0.05	46	1	Coplanar (clocking based)
[15]	0.12	108	2.5	Coplanar (clocking based)
[17]	0.10	104	1.75	Coplanar (clocking based)
FA / S Proposed (26-a)	0.09	92	1	Coplanar (clocking based)
FA / S Proposed (26-b)	0.09	84	1	Coplanar (clocking based)
[16]	0.19	180	1.75	Multilayer
[18]	0.6	90	3	Multilayer

The proposed Adder/Subtractor circuit is important because of the combination of two complementary and subtractive circuits results in having simultaneous operations.

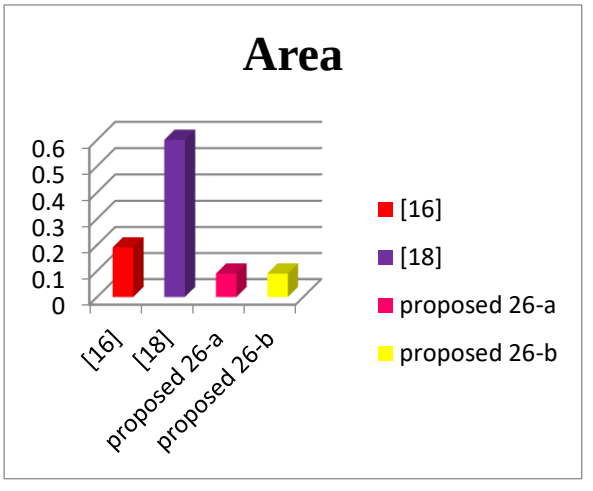

Fig. 33. Area comparison of Full Adder/Subtractor designs.

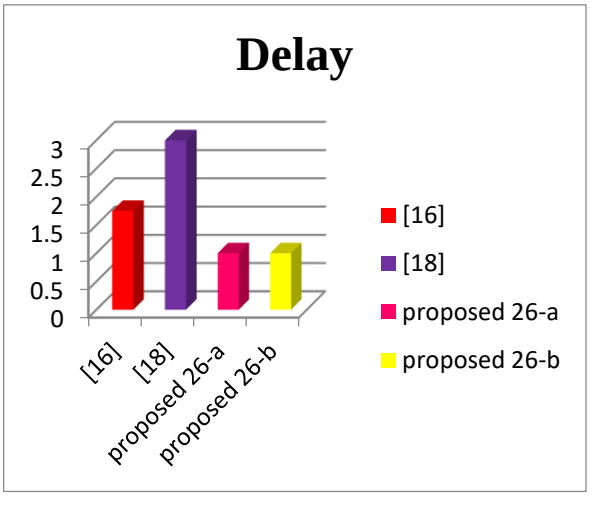

Fig. 34. Delay comparison of Full Adder/Subtractor designs.

According to Fig. 33, the area of the proposed circuit is compared with the previous work. It can be seen that the proposed scheme 26-a results in 85% and 52.63%, and the proposed scheme 26-b lead to 85% and 52.63%, area saving than [18] and [16], respectively. Besides, according to Fig. 35, the delay has been considerably improved. In other words, the proposed lead to about 67.66% and 42.86%, and the proposed scheme 26-b lead to 66.67% 42% improvement than [18] and [16], respectively.

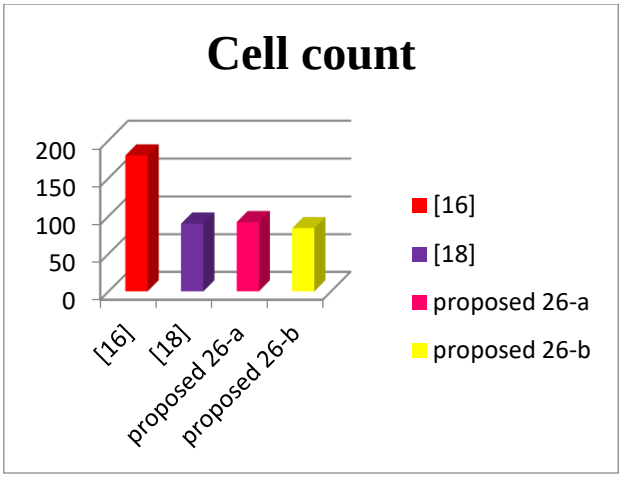

Fig. 35. Cell count comparison of Full Adder/Subtractor Designs.

Fig. 35 also shows the comparison of the proposed circuit cell number with the previous designs. It can be seen that the proposed circuit has fewer cells than the other designs. The proposed scheme 26-a results in about 48.9% and the proposed scheme 26-b results in 67.6% and 53.33% cell reeducation than [18] and [16], respectively.

5. CONCLUSION

In many designs, HA, FA, HS, FS, and FA / S, QCA technology uses at least two layers for intersection, while there are a number of designs that have been used in the design of the 45 ° cells. The design of the intersection with the phases of the clock is much stronger and better. That's why we used this design in our designs. While the proposed design of the research is in terms of the number of cells consumed, the consumption level, the delay, and the cost function, or better than the previous design, or the best of them in some parameters.

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