# An Ultra-Low Power RF Interface for Biomedical Implantable Devices

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**ABSTRACT**
This paper presents an efficient radio frequency (RF) front-end for power and data telemetry in biomedical implantable devices. The fully integrated system includes an amplitude shift keying (ASK) demodulator, a low drop out (LDO) voltage regulator and a charge pump voltage rectifier. This paper presents a rectifier structure based on Dickson charge pump. Simulation results show that this rectifier can provide 1.4 Voltage supply at a PCE of 33.4%. The rectifier consumes 80µW. The demodulator utilizes an ultra- low power envelope amplifier that removes the need for any voltage comparator or Schmitt trigger circuit, With a carrier frequency of 13.56 MHz and 40 Kbps data rate. The proposed ASK demodulator achieves a modulation index range from 38% consuming less than 32µW. The low drop out regulator can provide a maximum current of 2.8 mA and output voltage of 1.2 V and drop out voltage is 200mV. LDO temperature variation is 2.4µV/˚C. The LDO consumes only about 76µW. Designed in a 0.18 µm CMOS process, the system totally consumes 200µW.

**KEYWORDS:** Low Power, Power Supply Design, Wireless, Implant, Biomedical.

## 1. INTRODUCTION

Our purpose in this research is to design a power supply for implants devices. A typical implantable micro-system consists of two distinct units: an external controller and an internal unit (implant). A major concern in these micro systems is providing a durable power for implanted chip noting that batteries are not suitable due to their limited lifetime and large size.
Furthermore, communication between the implantable unit and external controller should be provided without wires to reduce the risk of infection.
In order to deal with these problems, power and data telemetry system using magnetically coupled coils are commonly used in the most of the biomedical microelectronic systems. The external part of the biomedical system sends the RF signal through induction to the internal part which is located inside the human body and uses modulated signals like ASK,FSK,PSK to send data as well. Signal transmission must be done with a high efficiency and low power consumption. Among various types of modulation techniques available, amplitude-shift keying (ASK) is the most common approach due to its simplicity yielding relatively low power consumption.

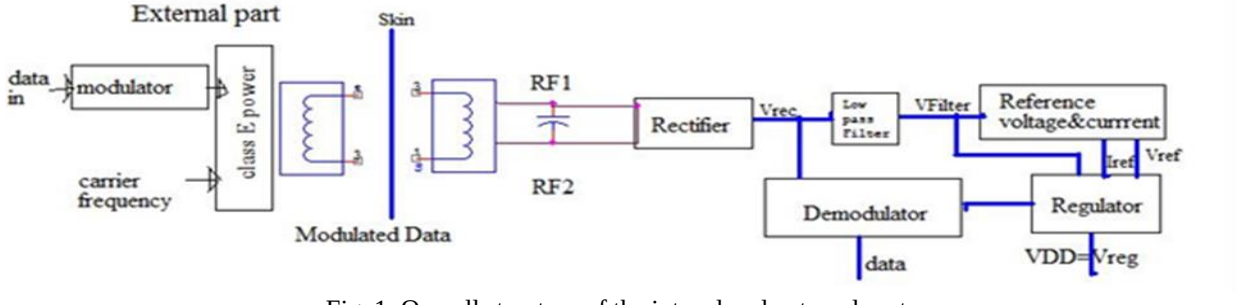


Fig. 1. Overall structure of the intenal and external parts

The external part includes a battery, a modulator and a power amplifier which has an inductive coil. The internal part should be designed with low power consumption and includes receiver coil, rectifier which turns the RF signal to DC voltage (which is the steady voltage we are trying to achieve), a voltage regulator, a low pass filter and a demodulator. Fig.1 shows the overall structure of internal and external parts. The research objective in the field of medical implant devices includes, designing components with low power consumption, energy transfer efficiency, high data rate, high efficiency amplifiers, small size and acceptable price. Therefore some parameters must be considered such as carrier frequency and size of elements. An important issue in designing wireless links is choosing an appropriate carrier frequency. The Standard frequency range that human body can be exposed is 3KHz to 30 GHz [1]. In this paper, the standard ISM frequency band of 13.56 MHz is used.

On the other hand the size of implanted device should be small as it is possible to be less aggressive to human body. To reduce size of implanted device we must reduce the complexity of electronic circuit blocks and the number of passive elements such as capacitors and resistors. The paper is organized into following sections: In Section II, system architecture is presented. Circuit details of the building blocks will be discussed in Section III. Simulation results are given in Section IV while in Section V, the conclusion is presented.

## 2. SYSTEM ARCHITECTURE

Fig.2 shows the overall block diagram of the designed RF interface. For realizing the wireless link, two inductively coupled coils are used: the primary coil is placed outside the body and the secondary coil is located in the human body connected to the implanted micro system. As mentioned previously, the carrier frequency must be selected by considering the safety level of human body and the required data rate. To be able to obtain a moderate data rate a carrier frequency of 13.56 MHz is chosen in this work and the modulation index is selected to be about 38% that can allow us to design a fully integrated system. As depicted, the internal fully integrated section includes voltage rectifier/multiplier, ASK demodulator, Ripple suppressor filter, voltage and current reference unit and voltage regulator.

The first block connected to the internal coil is the multiplier that rectifies the received RF signal and charges up storage capacitors to an unregulated voltage, $V_{rec}$ which is required for the stimulation unit. However, $V_{rec}$ , includes a high frequency ripple from the carrier frequency and a low frequency one coming from envelope data which makes hard the design of the regulator with fully on chip elements. So, a ripple suppressor filter is used to reduce these ripples for the reference circuit and the voltage regulator. In the following section, detailed circuit implementation of the building blocks will be provided.

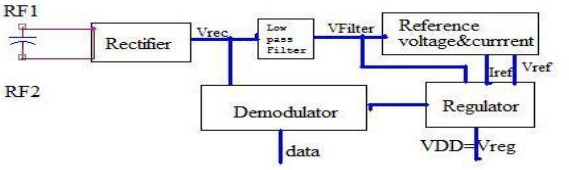


**Fig.2**. Overall block diagram of the RF interface.

## 3. CIRCUIT DETAILS

### 3.1. Rectifier

Voltage rectifier converts the induced ASK modulated signal into an unregulated supply voltage. Rectifiers are the most important blocks in implanted devices so it has to be good power efficiency.

In this paper we proposed a structure to improve the power efficiency of rectifier structure based on Dickson charge pump. This structure can overcome the drawback of conventional rectifiers and also use bulk driven technique. The charge pump rectifier works for low input RF signals and output Voltage of rectifier is also partly amplification. In addition step to step charging capacitor plays an important role in producing the output voltage and partly eliminates the ripple, therefore the overall implanted system needs a simpler regulator and filter blocks. When the Dickson charge pump structure is used, voltage drop of diode-connected MOS transistors decreased the PCE. We propose a novel rectifier structure that is compatible with the standard CMOS process and can realize a high PCE s well as the desired output voltage. PCE is an index of power dissipated by the load compared to total incident power and defined as the ratio of the output DC power to the incident power as follows:

$$\%PCE=P_{DC}/P_{RF} \quad (1)$$

To solve the threshold voltage drop problem, diode and diode-connected MOS transistor should be avoided also reverse current from the storage capacitor to the antenna should be suppressed as much as possible. Fig.3 shows the proposed rectifier in [2], sub circuit S1 and S2 consist of two PMOS transistor respectively. $M_a$ and $M_b$ are not diode-connected MOS transistor so the forward voltage drop arising from threshold voltage can be largely saved as much as in a gate cross-connected structure. To improve the potential reverse current drawback of the gate cross-connected circuit, $M_b$ is added. This MOS transistor will largely limit reverse

current from Node N3 to Node N1.In rectifier stage exists a voltage drop of $2I\times R_{on}$. It is necessary to reduce this voltage drop for the designed low voltage rectifier. One way is increase the devices size, another is to utilize the body bias technique. In this paper for proposed charge pump rectifier used body bias technique. This technique used for full wave rectifier in [16].It can be seen from the equation (2), $V_{TH}$ will decrease with the increasing of $V_{SB}$ and a smaller threshold voltage means a smaller on-resistance. Then an appropriate bias voltage can be applied to the substrate of $M_a$ and $M_b$. Fig.4.a shows the proposed rectifier in this article. In fig.4b shows a simple diode connected NMOS voltage divider circuit, which generates the bias voltage for PMOS transistors. In a standard CMOS process, the substrate of NMOS transistors is grounded directly.

$$V_{th}=V_{th0}+\gamma\left(\sqrt{2\varphi f-VBS}-\sqrt{2\varphi f}\right) \quad (2)$$

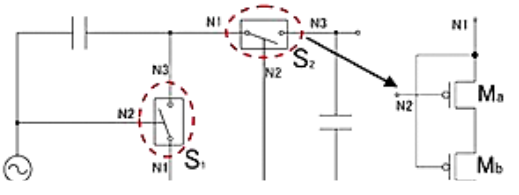


**Fig 3**. Recfier in [2]

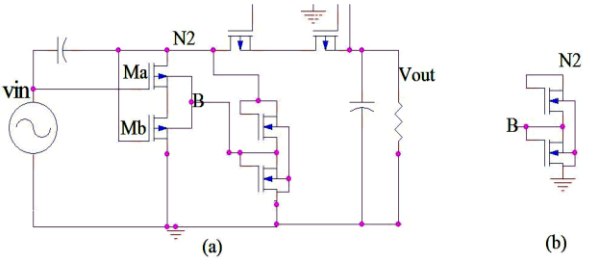


**Fig.4.a**. One stage rectifier structure, **b**. Substrate

### 3.2. Low drop out regulator

The low drop out (LDO) regulator is an essential block in implantable devices. The advantages of a low dropout voltage regulator include a lower minimum operating voltage, higher efficiency of operation and lower heat dissipation. The dropout voltage is defined as the minimum voltage drop required across the regulator to maintain output voltage regulation. Power supply rejection ratio (PSRR) is ripple rejection ability of the circuit to reject the ripple of power supply at various frequencies. The proposed low drop-out regulator is designed to improve power supply rejection ratio (PSRR) of the conventional LDO.

The proposed circuit is developed using error amplifier, sub-tractor circuit and PMOS as pass device. The purpose of this paper is to design an LDO with the following constraints. The output voltage will be 1.2 V using a 1.4 V unregulated supply voltage and a 400-mV reference voltage and 5uA reference current.

Fig.5 shows the general structure of proposed regulator. The pass transistor must be very wide so that it can source large load currents with a reasonable gate-source voltage. The length remains at the minimum value to keep the threshold voltage low. NMOS transistors are used at regulator output , instead of resistors voltage divider, to feed a fraction of the output voltage back to the input so that very little current flows through them, minimizing the power consumption of the feedback pat.

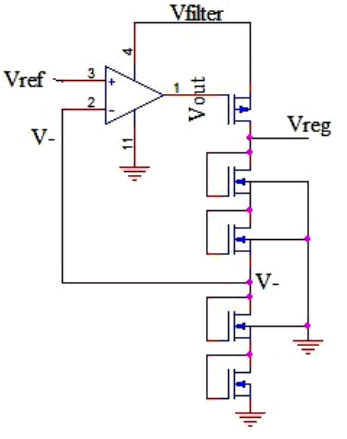


**Fig.5**.General structure of proposed LDO

Fig.6 shows the proposed op-amp circuit in this paper. The first stage is a folded cascade, which allows a lot of gain to be obtained in a single stage. PMOS transistors M1 and M2 are the inputs, with transistors M9 and M10 forming the cascaded tail current source, and NMOS transistors M3 and M4 are the “folded back” common gate transistors of the cascade . M5 and M6 provide the bias currents for M3 and M4, respectively. The folded cascade is loaded by an improved Wilson current mirror, formed by M7, M8, M11, and M12. This type of mirror eliminates the systematic gain error of the conventional Wilson mirror by adding another transistor to input side (M7 and M11) to equalize the drain-source voltages of the two transistors closer to the power supply (M7 and M8). Loading the first stage with an improved Wilson mirror instead of a simple two-transistor mirror increases the output resistance of the stage and thus further increases the gain. Finally, Last stage is a buffer that placed between the output of error amplifier and pass transistor to increase unit gain and stability of LDO stage.

For LDO Line regulation is the capability to maintain a constant output voltage level on the output channel of a power supply despite changes to the input voltage level also Load regulation is the capability to maintain a

constant voltage level on the output channel of a power supply despite changes in the supply's load.

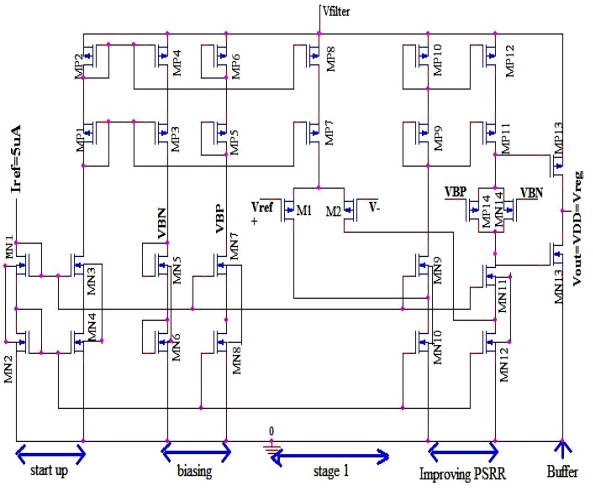


**Fig.6**. Proposed op-amp circuit

### 3.3. Demodulator

The typical ASK demodulators consist of two main building blocks; envelope detector and comparator. Presented ASK demodulator in [4] does not require comparator or Schmitt trigger circuit, thus mainly saving the power and area.

Fig.7 shows ASK demodulator in [4]. The design is divided into three main parts: voltage divider, envelope amplifier and buffer. In the first step, voltage divider receives the envelope of the ASK signal at the rectifier output, $V_{rec}$, providing three specific levels. These voltage levels are served as input to the subsequent envelope amplifier. In the envelope amplifier unit the amplitude of the envelope signal is maximized to a level that can be recognized by only a digital inverter-based buffer. Consequently, Schmitt trigger or comparator is no longer needed. Referring to Fig.7 voltage divider resistors, $R_1$ and $R_2$ and $R_3$ generate three voltage levels from incoming envelope signal named $V_{env\text{-}h}$, $V_{env\text{-}m}$ and $V_{env\text{-}l}$ where $V_{env\text{-}m}$ is set to the middle of the $V_{env\text{-}h}$ and $V_{env\text{-}l}$ . The low pass filter receives $V_{env\text{-}m}$ and eliminates its high frequency ripples so that a smooth voltage, $V_{avg}$ , is generated.

In this research, voltage divider and envelope amplifier blocks are improved. A voltage divider based on CMOS current mirror is used. NMOS and PMOS transistors are used as voltage divider instead using resistors. Also with replacing capacitor and resistor with MOS transistor connections the LPF is improved. Fig8 shows improved demodulator.

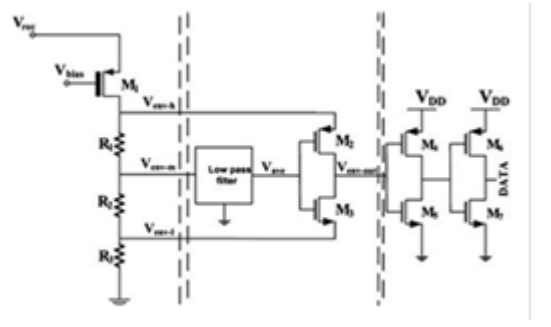


**Fig.7**. Demodulator in [4]

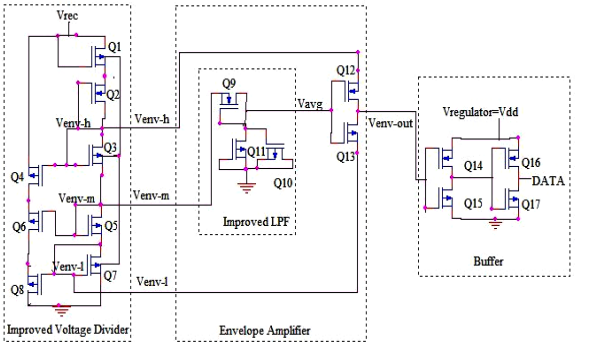


**Fig.8**. Improved demodulator

## 4. SIMULATION RESULTS

### 4.1. Improved rectifier

A single-stage rectifier circuit has been simulated in a 0.18um standard CMOS process.in order to achieve a 1.2 V regulated voltage at the regulator output in full load condition with a high current driving capability, about 1.4 V unregulated voltage should be provided by rectifier. Table1, provides the performance summary and comparison results for the Implement rectifier. This table proved that PCE of proposed rectifier have been improved. The rectifier consumes 80µW.

### 4.2. Improved LDO

The overall goal of this study was to design 1.2 V power supply for implanted devices. The proposed LDO was designed with TSMC standard 0.18µm CMOS process .In order to achieve a 1.2 V regulated voltage at the regulator output about 1.4 V unregulated voltage is needed therefor the output is only 200mV. Fig.9 and fig.10 shows The load and line regulation respectively, which are 0.0107 mV/mA and 0.28 mV/V, respectively. The LDO consumes only about 76 µW.

TABLE 1. RECTIFIER PERFORMANCE SUMMARY AND COMPARISON

| **Reference and year** | **[6] 2011** | **[3] 2012** | **[2] 2010** | **Proposed Rectifier** |
|---|---|---|---|---|
| **Technology** | 90 nm | 0.5 µm | 0.18 µm | 0.18 µm |
| **Number of stages** | 17 | 1 | 1 | 1 |
| **Input frequency (MHz)** | 915 | 13.56 | 900 | 13.56 |
| **Input voltage /power** | -18.83 dBm | 3V | 0.32 µW | 1.118V & 106µA |
| **Load resistance (KΩ)** | 1000 | No reported | 20 | 50 |
| **Output voltage (V)** | 1.2 | 0.25 | 1 | 1.4 |
| **PCE %** | 11 | 3.76 | 32 | **33.4** |

Also table 2, shows the critical points of the regulated output voltage versus temperature changes. Temperature changes from -40 ° C to 100 ° C and the LDO output voltage changes only 0.34 mV by changing the LDO input voltage from 1.4 V to 3.4 V, LDO temperature variation is 2.4µV/˚C**.** Table3 summarizes and compares the performance of the proposed LDO with other researches. This table proved that the proposed LDO have been improved.

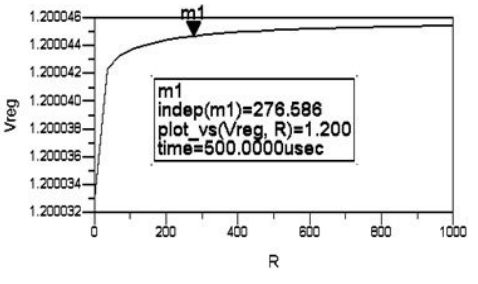


**Fig.9**.The measured load regulation for

**TABLE 2.** Critical points of the regulated output voltage versus temperature changes

| **Maximum voltage 3.6** | **Balance voltage 2.4** | **Minimum voltage 1.4** | **Output voltage (V) ←** | **Temperature ( ˚C ) ↓** |
|---|---|---|---|---|
| 1.2057314 FF | - | 1.2053904 FS | **Min temp:-40** | |
| - | 1.2056431 TT | - | **Balance temp: 30** | |
| 1.2057314 SF | - | 1.2053904 SS | **Max temp:100** | |

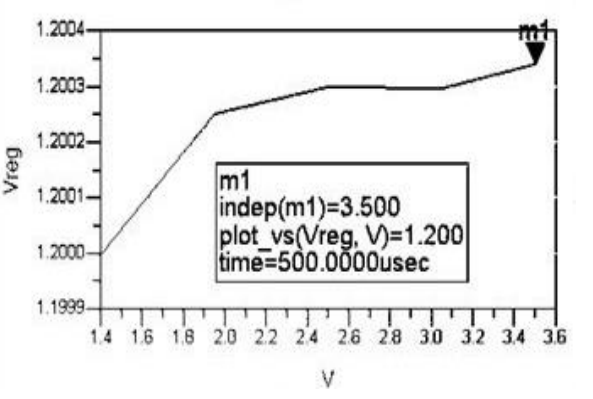


**Fig.10**. The measured line regulation For $1.4V<V_{in}<3.6V$

**TABLE 3**. The LDO charactristics and its comparison with others works.

| **Reference** | **[7]** | **[8]** | **[9]** | **Proposed LDO** |
|---|---|---|---|---|
| **Year** | 2009 | 2012 | 2013 | 2014 |
| **Technology (µm)** | 0.18 | 0.25 | 0.18 | 0.18 |
| **Input voltage range(V)** | 2-3.2 | 3-5 | 3.5-4.5 | 1.4-3.6 |
| **Output voltage range (V)** | 1.5 | 2.8 | 3.3 | 1.2 |
| **Output drop out(mV)** | 541 | 200 | 200 | 200 |
| **Max output current(mA)** | 150 | 50 | 200 | 2.8 |
| **load regulation (mV/mA)** | 0.101 | 0.056 | 0.09 | 0.0107 |
| **Line regulation (mV/V)** | - | 1.85 | 2 | 0.28 |

### 4.3. Improved demodulator

Fig.11 Shows voltage levels provided by the voltage divider previously called, $V_{env\text{-}h}$ and $V_{env\text{-}l}$ which represent the envelope of the signal, also the output of the low pass filter, $V_{avg}$ .Data rate is, the "one per length of each bit." which mean if the length of each bit be 2µs then the data rate is equal to 0.5 Mbps.

Modulation index is a measure based on the ratio of the modulation excursions of the RF signal to the level of the un-modulated carrier. 100% or over 100% modulation index, causes distortion in received signal. Usually it is better modulation index be less than 50%.For a data rate of 40 Kbps according RFID standard and modulation index of 38%, the ASK demodulator consumes only about 32 µW.

Table 4, summarizes the demodulator charactristics and compares it with some other researches.Fig.12 shows output data.

Table 5, shows overall characteristics of the proposed RF interface and compare it with prior works and indicates that the overall proposed RF interface has achieved a good rank among other prior works.

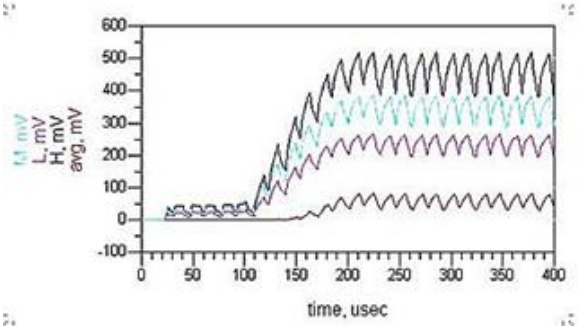


**Fig.11**. Shows voltage levels provided by the voltage dividerup to down : Venv-h و Venv-m و Venv-l و Vavg

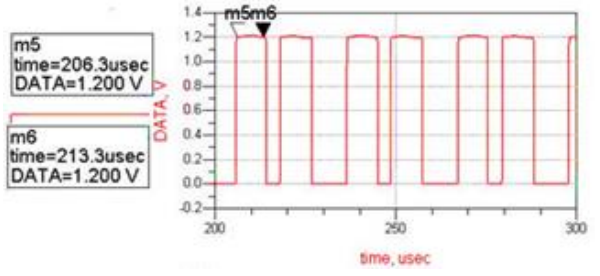


**Fig.12**. Output data

**TABLE 4**. The demodulator charactristics and its comparison with others works.

| Year Reference | Data rate (Kbps) | Loss Power (mW) | number of components | technology (um) | carrier frequency (MHz) |
|---|---|---|---|---|---|
| **2010[10]** | 45 | 0.031 | 43 | 0.25 | 1.5 |
| **2010[11]** | 500 | 0.0295 | - | 0.18 | 1.5 |
| **2009[12]** | 1000 | 0.396 | 17 | 0.18 | 2 |
| **2011[13]** | 1000 | 0.35 | - | 0.35 | 10 |
| **2013[14]** | 76 | 0.1 | - | 0.25 | 1 |
| **2012[4]** | 1000 | 0.035 | 16 | 0.18 | 12 |
| **Ours** | 40 | 0.032 | 19 MOS | 0.18 | 13.56 |

**TABLE 5**. Overall characteristics of the proposed

| Reference year | Loss power (mW) | Vdd (V) | LDO Pass transistor | Rectifier | Carrier frequency (MHz) | Technology (µm) |
|---|---|---|---|---|---|---|
| **[4] 2012** | 35 | 3.3 | PMOS | Full wave | 12 | 0.18 |
| **[15] 2013** | 85 | 1.8 | NMOS | Full wave | 13.56 | 0.35 |
| **This work** | 0.2 | 1.2 | PMOS | Improved Charge pump | 13.56 | 0.18 |

## 5. CONCLUSION

A fully integrated front-end circuitry for power and data telemetry system for biomedical implants was reported. An improved rectifier, a LDO, an ASK demodulator circuits are presented which are suitable for biomedical applications. Furthermore, by using a ripple suppressor filter the need for an off chip storage capacitor in voltage regulator circuit is removed. Designed in a 0.18 mm CMOS process, the system totally consumes 200µW.

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