Behavioral modeling for sampling receiver with baseband structure with noise pattern recognition and cancelation in MATLAB/SIMULINK

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ABSTRACT:
Software Defined-Radio (SDR) is a wireless communication system which consists of a transmitter and a receiver that are controlled by means of software. Its goal is to provide a single radio transceiver with multi-mode multi-standard wireless communications capability. This advantage will help the designers to have a more precise technological look at the performance and processing principles of this structure and have better designs for their structure. In this work, discrete-time signal processing of a direct-sampling discrete-time receiver which is used for radio Bluetooth applications, is modeled in Simulink environment. The results show that, when the BPSK signal is entered to the receiver with an additive white gaussian noise (AWGN), the system had the best performance. In this simulation the signal time domain and its spectrum is shown in each stage of receiver, in order to display the noise removal process and the original signal extraction from noisy signal.

KEYWORDS: BPSK Modulation, FIR/IIR Filtering, Noise Pattern Recognition, Signal Processing, Transmitter-Receiver.

1. INTRODUCTION

In the recent decades, the world is faced with huge increase in demand for wireless devices which are portable, so to fulfill this demand, the size and the power consumption of all components must be reduced, for this purpose the classic RF receivers have been under study. Using conventional techniques in design of wireless communications devices like cell phones with multi applications will lead to build a bigger receiver, and even that would not work properly in many cases. This concept is an important drawback of classical techniques. One of the best solutions to these problems for the RF receivers is to use the digital blocks in the receiver and eliminate analog components. Using analog blocks in design of the multi application receivers will be the main cause of the increase in the size of receiver, so we have to use the structures that bring the digitalization closer to the antenna. This will lead to design smaller receivers that improve their capabilities through software. This is the emersion of Software Defined-Radios.

In the next three Figures, the architecture of the most common conventional analog front-end is shown. It can be seen in all of these architectures, the analog components like filters, amplifiers and mixers; are used.

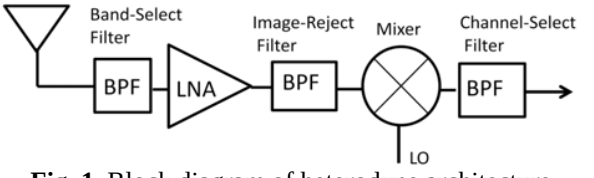

Fig. 1. Block diagram of heterodyne architecture

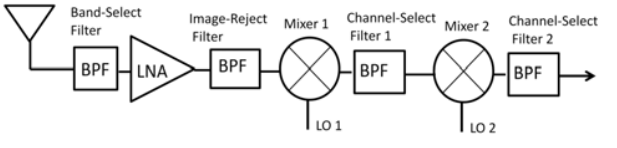

Fig. 2. Block diagram of superheterodyne architecture

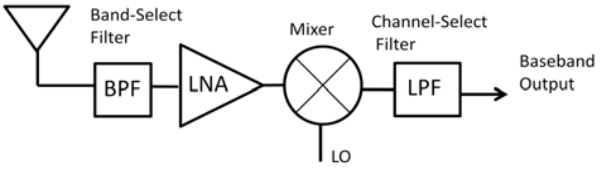

Fig. 3. Block diagram of homodyne architecture

The above receiver structures have some disadvantages [1] and can't be use as a proper receiver

in software defined-radios. So to solve this problem discrete time techniques can be used. The block diagram, of such systems is shown in fig. 4.

2. DISCRETE-TIME RECEIVER STRUCTURE

Fig. 4 shows the block diagram of a receiver employing discrete-time techniques. The band pass filter (BPF) and the low noise amplifier (LNA) are the only off-chip components used in this structure.

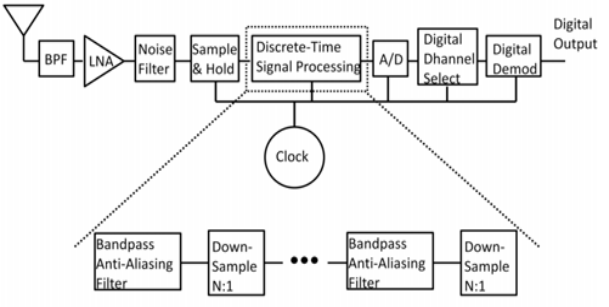

Fig. 4. Block diagram of a receiver with discrete-time technique

When the signal reaches the sample and hold stage, this block will start the sampling process with 1/T sampling frequency from the signal. After this stage, the signal is not continuous anymore and it is converted to discrete in time. So after this stage, digital blocks can be used, and desire signal processing operations can be done with digital blocks which means lower power consumption and smaller occupied space. In the discrete in time processing unit using the blocks such as bandpass anti-aliasing filter and a down-sampling block with decimation factor N are very formal.

In discrete in time processing unit, first of all, the input noise of the signal is filtered out and if needed, the sampling frequency will be down-converted to lower frequency, to reduce the next stage's computation process. The next stage in this system is like the classic structures [1]. The discrete-time signal is converted to digital signal by using an analog to digital converter (ADC) then the important information of the signal is extracted by using a digital modulator.

The most important blocks used in multi-rate digital signal processing are a Sampler (S&H) an Anti-aliasing Filter, a Down-converter and an Up-converter.

The use of an Anti-aliasing Filter with a Down-converter is called Decimation and if instead of Down-converter, an Up-converter is used it is called Interpolation. These two combinations of blocks are shown in fig. 5 and fig. 6.

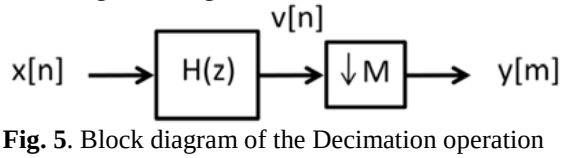

Fig. 5. Block diagram of the Decimation operation

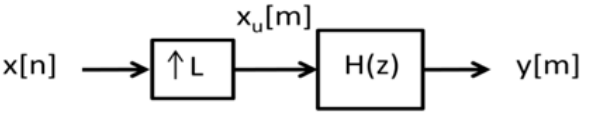

Fig. 6. Block diagram of the Interpolation operation

Like superheterodyne structure, in the software defined-radio's structure the multistage decimation or interpolation can be used instead of one stage for decreasing or increasing the sampling rate of the signal. This will help to avoid high decimation or interpolation factors in one stage, and will reduce the manufacturing difficulty and cost. In order to do this job there is one requirement which must be accomplished. The decimation or interpolation factor (N) cannot be a prime number because to be dividable into more than one stage, so the decimation or interpolation factor N can be written as $N=N_1\times N_2\times\ldots\times N_i$, which N_i is the decimation or interpolation factor related to each stage.

The proper sampling receiver can be designed, by using the basic blocks, for software defined-radio applications.

2.1. Direct-Sampling Receiver

The receiver proposed in this work, is a fully digital receiver for Bluetooth Radio applications. In this receiver, direct sampling technique is used [2]. The structure of this fully digital receiver is shown in fig. 7. As can be seen, there is three filtering and rate conversion stage between sampler and ADC, in this receiver. The carrier frequency of the input signal is 2.4 GHz and it is sampled with 2.4 GS/sec rate then in the next stage the sampling rate is down-converted directly, to reach the baseband frequency. In this structure, to achieve the best rate for the receiver, 64 is chosen for the final decimation factor. This number is not a prime number and it can be divided as 64=8×4×2. So the rate can be decimated by 8, then by 4 and then by 2. So the signal will reach the proper sampling value. Thus if the input frequency of the receiver's sampler is equal to 2.4 GS/sec and the final decimation factor is 64 then the input signal of the ADC will have a sampling rate, equal to $2.4\,\text{GS/sec}/64 = 37.5\,\text{MS/sec}$.

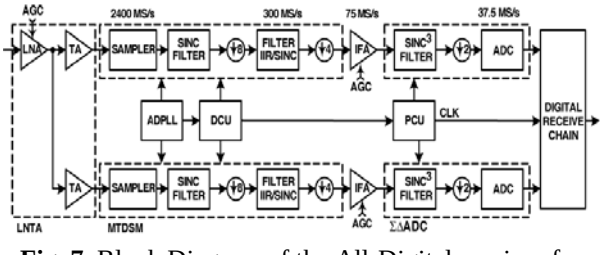

Fig. 7. Block Diagram of the All-Digital receiver for Bluetooth Radio [3]

2.2. Advantages of a Direct-Sampling Receiver

Designing and implementation of a receiver on single IC is the goal of this project and it will reduce the manufacturing cost, implementation complexity and occupied space of silicon [2], [4]. Implementation of the programmable digital signal processing unit of this receiver has the most complexity. With this feature, any special operation is achievable just by one time programming of this IC and this IC can be used for millions of different devices like cell phones and etc., just by one simple programming stage. Thus it will extremely reduce the manufacturing cost. There is no limitation in working frequency of this structure and it can be used in the whole working frequency range of silicon [2]. In this structure the filter of the receiver's input stage can be omitted. This structure is useable to implement swept receivers, such as those in spectrum and network analyzers. It has minimal spurious response caused by non-ideal effects and nonlinearities of circuits. The most important spurious effects in this structure are caused by harmonics of local oscillator, which their frequency is far enough from operating frequency of the receiver and are filtered out automatically. Additionally, the signal processing path is very short and thus this structure has a very high linearity.

2.3. Structure Modeling in Simulink Environment

The structure of this receiver can be modeled by using the ordinary blocks in Simulink environment like, discrete blocks and FIR/IIR Digital filters. For this purpose, first of all the transmitter of this structure must be modeled.

To model the transmitter, a random Bernoulli binary generator is used and it is modulated by a BPSK modulator. The BPSK binary modulator is a digital modulator and it will convert the random Bernoulli binary generated numbers to data with desire information. The digital output of the BPSK modulator, is modulated with a carrier signal in much higher frequency. The carrier frequency of this multiplier is provided by a sinusoidal carrier in Bluetooth frequency of 2.4 GHz. The point in this simulation is that Matlab works with discrete-time signals instead of time-continuous signals, so the carrier frequency of 2.4 GHz must be converted to discrete signal which can be used in discrete-time system of the receiver without any problem [4]. For this purpose the carrier signal frequency f_c=2.4 GHz must be sampled with a much higher frequency to be converted to discrete-time signal. Thus the sampling frequency of the carrier generator is about 24GS/sec to guaranty the stable working of the receiver [5]. It is obvious that this is done because the simulation is performed in Simulink environment and this software has some limitations. So first of all, the undesirable harmonics in 24 GHz frequency must be filtered in receiver stage and the signal frequency must be reduced by a factor of 10, to reach the desirable frequency for Bluetooth application which is 2.4 GS/s. After this stage, the full structure of the receiver which is composed of mixer, filters and sigma-delta can be designed [5]. The model of this receiver is shown in fig. 8. It is good to mention that in the real world, the shape and the frequency response of the modulated signals which are transmitted through antenna to the environment are undesirably distorted because of the adverse effect of the environment on the signal. The connection path between the transmitter antenna and the receiver antenna is called communication channel. This channel has some undesirable effects on the signal which are caused by the environmental parameters, such as environment noise, temperature, structural and non-structural barriers and etc. To simulate these undesirable effects on the modulated signal in Simulink environment, an AWGN generator block is used. The AWGN Channel block adds white Gaussian noise to input signal and will help us to simulate the undesirable effects of the communication channel on the signal. In fig. 9 the shape of the output signal of the BPSK is shown.

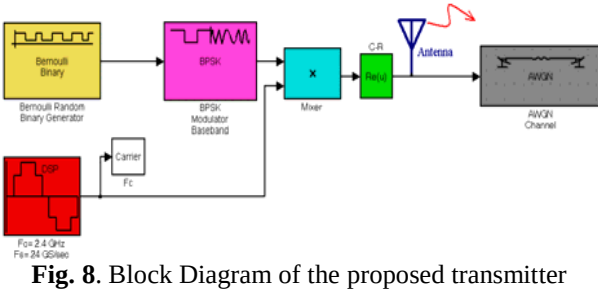

Fig. 8. Block Diagram of the proposed transmitter

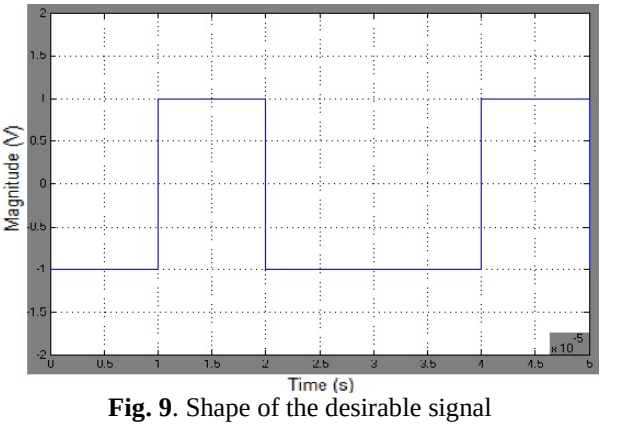

Fig. 9. Shape of the desirable signal (output of the BPSK)

2.4. Modeling of the Receiver

As it was discussed in previous sections, the overall decimation factor applied to the sampling frequency is N=64. This decimation factor is very large and its implementation is hard so this decimation factor is implemented in 3 stage with N=8, 4 and 2. The

modeling of this receiver in Simulink environment is shown in fig. 10.

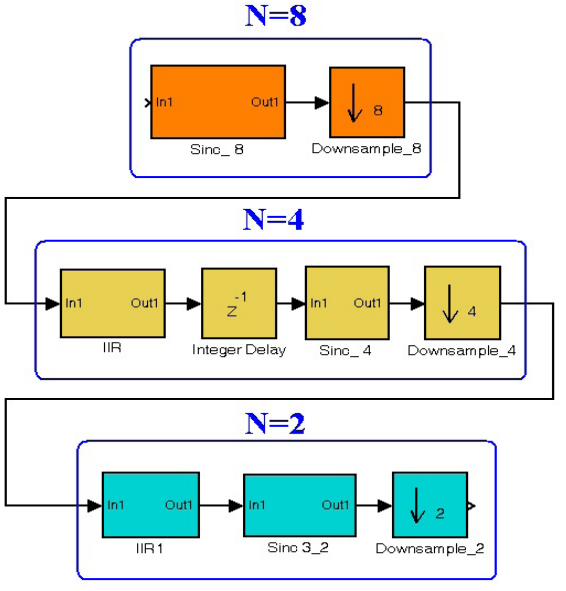

Fig. 10. Block diagram of the multistage direct-sampling receiver

Fig. 11 shows the structural overview of this transmitter-receiver and its spectrum.

Fig. 12 and fig. 13 show the simulation result of the transmitter-receiver model of fig. 11. The results obtained display the signal at each point in the frequency and time domain.

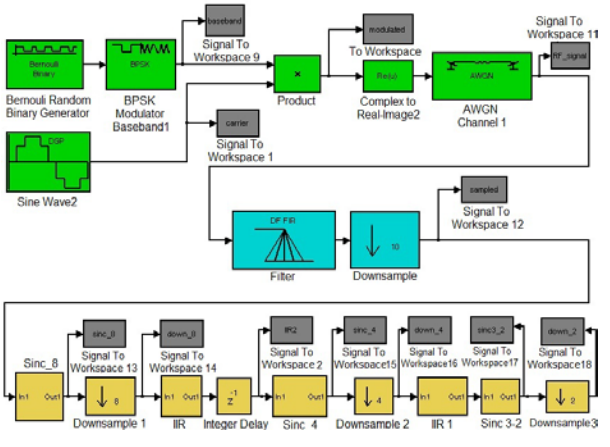

Fig. 11. Block diagram of the direct-sampling transmitter-receiver

At first the modulated signal and its spectrum is shown before considering the impact of noise. As it was expected, this signal has an absolute sinusoid shape. Then, the shape of the signal is shown after passing the AWGN block. In this stage the effect of the channel noise is added to the signal and as can be seen, the shape of the signal is not sinusoid anymore and it is destructed by the noise.

The main goal of this simulation is to reconstruct the signal that is destroyed by the channel noise and extract the original signal (output of the BPSK block – fig. 9) from the destructed signal. The results of the each receiver stage are shown step by step, to reach the desirable output from the receiver. By following the demonstrated results, the reconstruction process of the affected signal will be more comprehensible and we will understand how the noise is being eliminated as the signal is filtered. The proposed method can fully reconstruct the disturbed signal by using the sampling rate changing technique and filtering in each stage.

3. CONCLUSION

In this paper, we had an overview of the history and application of Software Defined-Radio (SDR). Then, a discrete-time structure of Software Defined-Radio (SDR) is proposed.

Then, a direct-sampling, transmitter-receiver structure is introduced for using in Bluetooth Radios and a model is proposed for its simulation in Matlab/Simulink environment. To simulate this model, a BPSK modulated signal and a channel with AWGN is used for modeling the transmitter block. The receiver model is composed of several sampling rate reducer and several digital filters such as FIR/IIR. The simulation result in Matlab environment shows that the proposed model has the ability to extract the desirable data from the disturbed noisy signal with very small errors.

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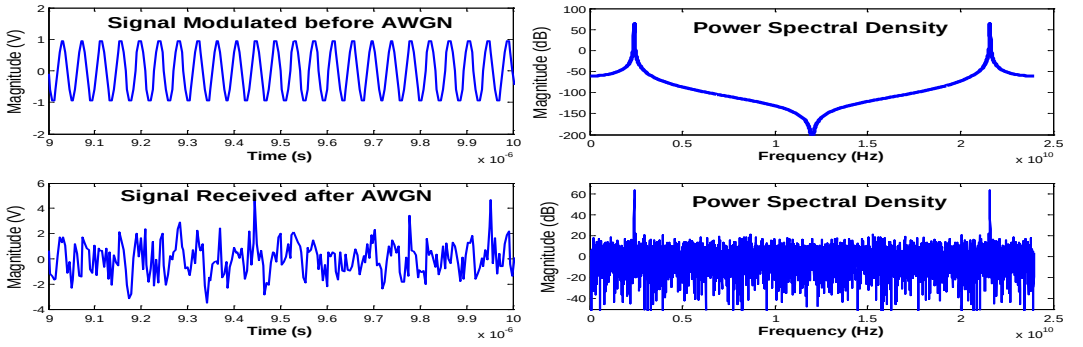

Fig. 12. Simulation results for transmitter stage, before and after noise destruction

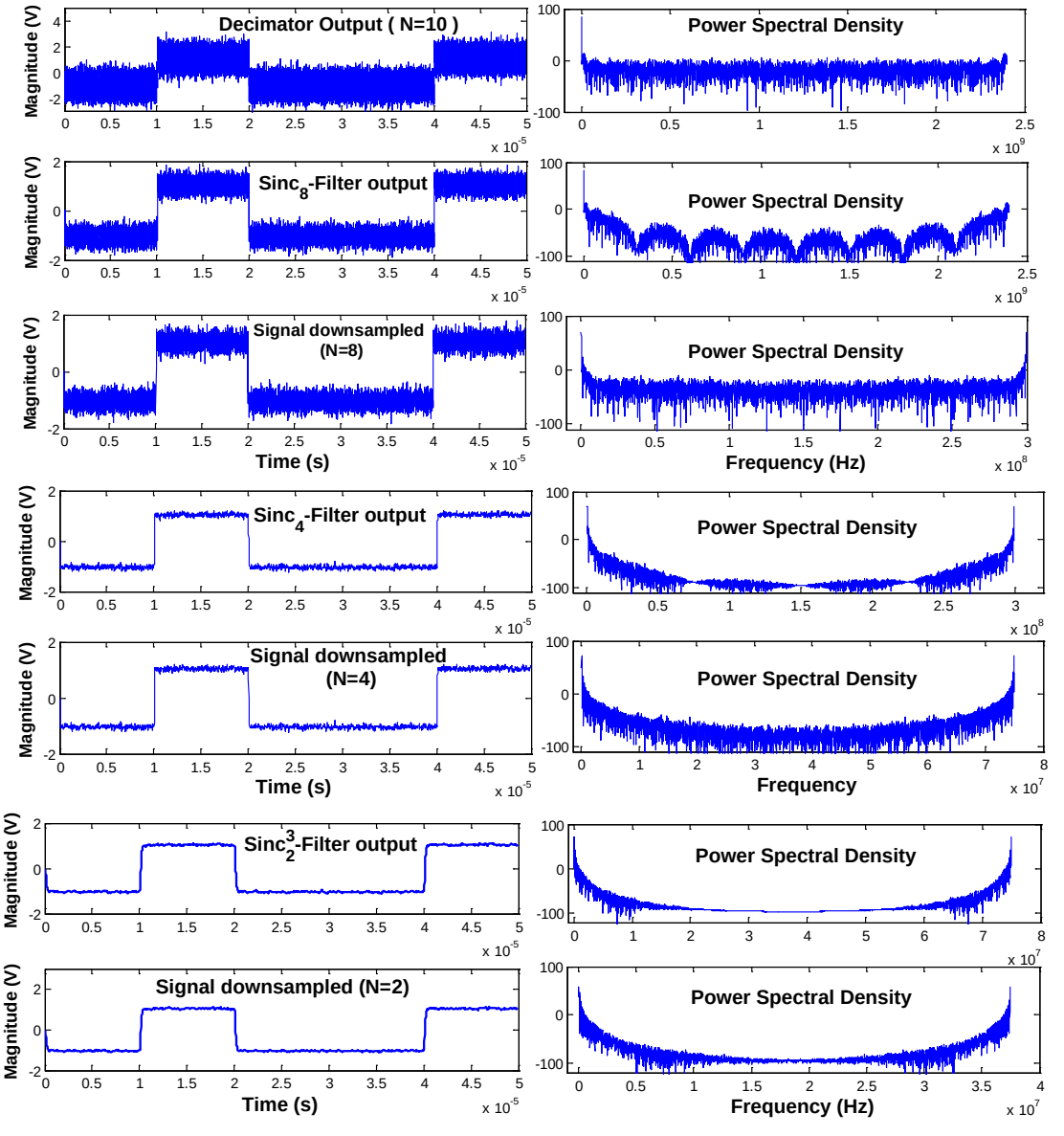

Fig. 13. Step by step simulation results for receiver stage to reach the desirable signal