Modelling of Drain Current of MOSFET Transistor in Terms of Gate Oxide Thickness

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Received: December 2015 Revised: January 2016 Accepted: February 2016

ABSTRACT:
Study on effects of changing the oxide thickness, can give us a view of the aspects of MOSFET, in field of design of the transistor elements. Changing the oxide thickness affects on both C_{ox} and V_t. At first, in this paper, the relation between the threshold voltage and oxide thickness will be discussed. Then, the relation between the drain current and oxide thickness will be modeling. The result is a nonlinear and parabolic relationship between the drain current and oxide thickness. To ensure the authenticity of the obtained model, a MOSFET parameters, based on 5 µm CMOS technology was designed. This MOSFET was simulated with COMSOL software and obtained mathematical model analyzed with MATLAB. Finally, the data were compared, which confirmed the authenticity of the mathematical model.

KEYWORDS: Drain current, Insulator thickness, Modelling, MOSFET, Threshold voltage.

1. INTRODUCTION

In designing a MOSFET for various applications as a switch to an amplifier, it must be precisely examined many aspects of the design; Including the length and width of the gate, concentration and type of substrate doping, doping concentration of the drain and source, and many other parameters can be mentioned. One of the most important parameters in designing a MOSFET is determining the insulator material and thickness exactly. Silicon oxide (SiO2) is preferred as the insulator in MOSFET transistors. Over the years, Oxide thickness decreased from 300 nm for 10 µm technology to only 1.2 nm for 65 nm technology. There are two reasons for the relentless reduction of the oxide thickness; first, the thinner oxide means a larger oxide capacitance (C_{ox}), which increases the MOSFET's turn on current (I_{on}), and a larger I_{on} increase the circuit speed. The second reason is controlling the threshold voltage (V_t) - and therefore the threshold current leakage - when the channel length is reduced [1], [2]. Thereby reducing the thickness of gate oxide is deserved. But in practice it is confronted with major problems; first, it is difficult to make thin and uniform insulator layer of SiO2. Oxide breakdown is next problem. Electric field could be a cause for destructive breakdown if oxide is too thin. Another factor which prevents the further reduction in oxide thickness is that the long-term run in a strong electric field, especially at the high temperature of the chip, leads to break in weak chemical bonds at the interface between Si and SiO2. And therefor, electric charge is generated that leads to change in threshold voltage. Another limiting factor in insulator thickness thinner than the 1.6 nm is gate current leakage to channel in form of tunneling [3].

To solve these problems, various methods such as the use of carbon nanotubes as transistor channel or use other materials to replace SiO2 such as HfO2, Al2O3 and ZrO2 as the insulator has been suggested [4]. Aside from solutions that have been used to overcome these problems, study on the effects of changing in thickness of oxide on the functional aspects of MOSFET can give us a good view in the field of transistor elements designing. It can be noted from previous works on study of the oxide thickness effects on the threshold voltage [5].

In this paper, we present a mathematic model for MOSFET drain current versus oxide thickness. A MOSFET transistor with all of its parameters as a sample was suggested in section 3. And it analyzed with MATLAB in section 3.1, then it simulated with COMSOL Multiphysics software in section 3.2. Finally, all results were compared in section 3.3.

2. DRAIN CURRENT VERSUS GATE OXIDE THICKNESS MODELLING

An N-type MOSFET suggested to investigate the effect

of reducing the thickness of oxide on the drain current. The MOSFET is consists of a P-type substrate, two heavy doped N-type wells to forming the drain and source, oxide and poly-silicon gate. The structure shown in Figure 1.

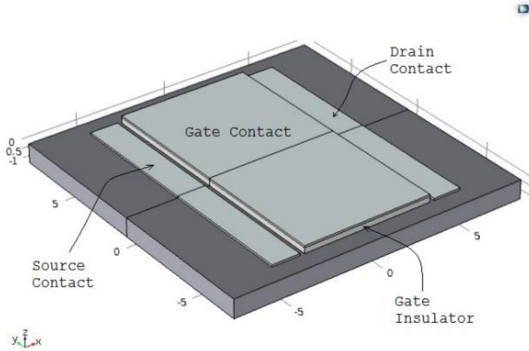

Fig. 1. The suggested MOSFET transistor structure.

Equation (1) governs on drain current in the saturation region [6]. Drain-source voltage effect is ignored.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \quad (1)$$

Where μ_n, W, L and V_{GS} are the electron mobility, channel width, channel length and gate voltage of MOSFET, respectively. In this equation, in addition to C_{ox}, V_t also depends on the thickness of the oxide. At first, MOSFET's threshold voltage dependence on the thickness of the oxide will be discussed. The structure of a MOS capacitor with its energy band diagram, when any voltage is applied to its gate, shown in Figure 2.

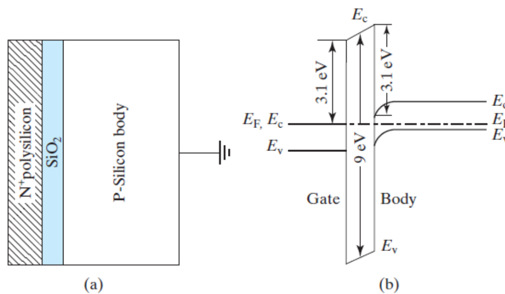

Fig. 2. (a) The structure of a MOS capacitor, (b) MOS energy band diagram when any voltage is applied to its polysilicon gate.

A channel of majority carriers (the electron, in this report) must be established between the drain and source, to electric current flow between them. Therefore, by applying a voltage to the gate, an electric field is created along the oxide, which cause to drift holes and the accumulation of electrons in substrate below the oxide. Which creates a conductive channel between the drain and source. This increasing voltage in gate leads MOSFET to change its mode from accumulation to depletion, weak inversion and then strong inversion, respectively. Finally, necessary conditions for current establishment are provided in the strong inversion mode. Figure 3 shows the energy band diagrams of a MOS capacitor in the absence of the polysilicon gate voltage applied to it. As can be seen, Fermi level near the oxide is closer to conduction band, and as it gets away from oxide, gets closer to valence band.

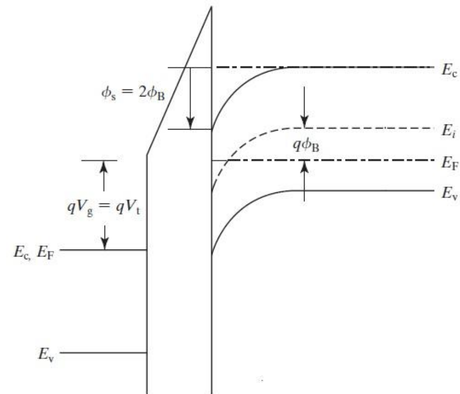

Fig. 3. MOS energy band diagram when a gate voltage equals to threshold voltage is applied.

In summary, from (2) to (5) are the most important equations for calculation of the MOS capacitors threshold voltage.

$$V_{fb} = \psi_g - \psi_s + (-Q_{ox} / C_{ox}) \quad (2)$$

Where ψ_g, ψ_s and Q_{ox} are the gate work function, silicon work function and total charge trapped in the oxide, respectively.

$$\begin{aligned} V_g &= V_{fb} + \phi_s + V_{ox} + \phi_{poly} \\ &= V_{fb} + \phi_s + Q_s / C_{ox} + \phi_{poly} \end{aligned} \quad (3)$$

Where ϕ_s and V_{ox} are the silicon surface potential at bent portion of band diagram and the voltage across the oxide, respectively.

$$\phi_{st} = 2\phi_B \quad (4)$$

Where ϕ_{st} is surface potential level at bent portion of band diagram in threshold mode.

$$V_t = V_{fb} + \phi_{st} + \frac{\sqrt{qN_{sub} 2\varepsilon_s |\phi_{st}|}}{C_{ox}} \quad (5)$$

Where N_{sub} and ε_s are substrate doping concentration which is equivalent to N_a and silicon relative permittivity, respectively.

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} \quad (6)$$

The drain current equation, in terms of oxide thickness will be simplified according to (7).

$$I_D = \frac{1}{2}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\frac{W}{L} \cdot \left(V_{GS} - V_{fb} - 2\phi_B - \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{\varepsilon_{ox}} t_{ox} \right)^2 \quad (7)$$

The equations from (8) to (10) will be replaced in (7), for simplification.

$$\frac{1}{2}\mu_n \varepsilon_{ox}\frac{W}{L} = \alpha \quad (8)$$

$$V_{GS} - V_{fb} - 2\phi_B = \beta \quad (9)$$

$$\frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{\varepsilon_{ox}} = \gamma \quad (10)$$

The result will be as follows:

$$I_D = \frac{\alpha}{t_{ox}}\left(\beta - \gamma t_{ox}\right)^2 \quad (11)$$

For more simplicity, equations from (12) to (14) can be replaced in (11).

$$A = \alpha\beta^2 = \frac{\mu_n \varepsilon_{ox} W \left(V_{GS} - V_{fb} - 2\phi_B\right)^2}{2L} \quad (12)$$

$$B = \alpha\gamma^2 = \frac{2\mu_n W q N_a \varepsilon_s \phi_B}{L\varepsilon_{ox}} \quad (13)$$

$$C = 2\alpha\beta\gamma = \frac{\mu_n W \sqrt{qN_a 2\varepsilon_s 2\phi_B}\left(V_{GS} - V_{fb} - 2\phi_B\right)}{L} \quad (14)$$

Final result will be as (15).

$$I_D = \frac{A}{t_{ox}} + Bt_{ox} - C \quad (15)$$

If (15) is differentiate, the slope behavior can be realized.

$$\frac{dI_D}{dt_{ox}} = -\frac{A}{t_{ox}^2} + B \quad (16)$$

3. COMPUTER AIDED MODEL ANALYSIS

Today, there's no denying the impact of computer softwares in various stages of design, testing and implementation of engineering products. One type of software that is highly developed in recent decades, are physical phenomena simulators and analyzers. Therefore, it will be simulated and analyzed in MATLAB and COMSOL Multiphysics, to verify the obtained mathematical model.

3.1. MATLAB Study of Result Term

A MOSFET is designed with the parameters in Table 1, to study of the behavior of drain current equation that obtained in previous.

Table 1. MOSFET's design parameters.

Parameters	Symbols	Values
Electron Mobility	μ_n	1450 $Cm^2/V.S$
Oxide Relative Permittivity	ε_{ox}	3.9
Channel Width	W	14 µm
Channel Length	L	7 µm
Acceptor Density (for substrate)	N_a	10^{17} Cm^{-3}
Donor Density (drain & source)	N_d	10^{20} Cm^{-3}
Surface Potential, Band Bending	ϕ_s	0.86 V
Gate Work Function	ψ_g	4.1 V
Gate-Source Voltage	V_{GS}	5 V
Drain-Source Voltage	V_{DS}	2 V

For using (15) in MATLAB, The α, β and γ constants must be determined, at first. Then, the A, B and C constants can be found with some simple operations. The approximate values of these constants are given as follows:

$$\alpha \simeq 5.0046\times10^{-4}\left(\frac{\mu A.Cm}{V^2}\right) \quad (17)$$

$$\beta \simeq 4.518(V) \quad (18)$$

$$\gamma \simeq 4.9021\times10^5 (V/Cm) \quad (19)$$

Figure 4 was obtained by analyzing the (15) in the MATLAB software in the range from 6 to 30 nm for oxide thickness. As you can see, as expected based on (16), relation between the current reduction with increasing the oxide thickness is not linear. It should be noted that, gate voltage sets on a voltage that prevent MOSFET out of the saturation region by increasing the oxide thickness. However, it will be closed to linear region, when the oxide thickness increases.

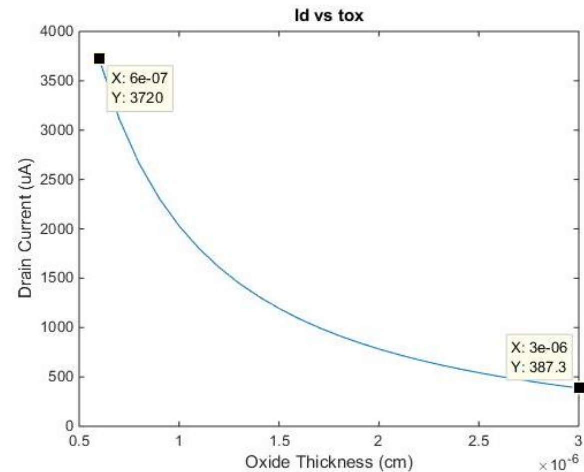

Fig. 4. Drain Current in terms of oxide thickness diagram that analyzed with MATLAB.

Figure 4 can be interpreted that changing the oxide thickness from 6 to 30 nm change the current of about 3700 µA down to about 400 µA, it shows the importance of accurately determining the oxide thickness.

3.2. COMSOL Multiphysics Simulation of Designed MOSFET

To ensure accuracy of the obtained model and more detailed study on the designed MOSFET, It was simulated in the COMSOL Multiphysics software. Because the COMSOL can simulate semiconductor physics phenomena with high accuracy, the results can provide adequate assurance of the correctness of the model. The COMSOL model will be according to the Figure 5, by using the Table 1 parameters and load the initial values in COMSOL interface. In this figure, drain, source and gate connections with oxide, for the better view of doping diffusion, temporarily hidden.

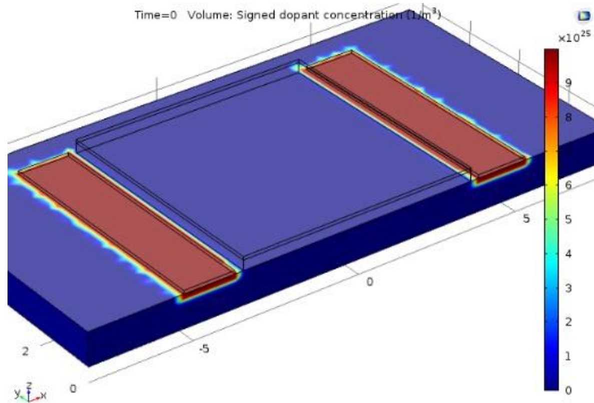

Fig. 5. The MOSFET cross section view, which shows the depth of the drain and source impurities diffusion.

At first, transistor must be biased at an appropriate operating point. The most important condition of this point is that MOSFET must not be inter in to the linear region with changing the oxide thickness at a specified interval. Therefore, MOSFET's turn on voltage (threshold voltage) must be determined, at first. To determine the threshold voltage, a very small voltage (about 10 mV) is applied to the drain, and gate voltage will be increased until the channel below the oxide formed and began to flow the current. Result shown in Figure 6.

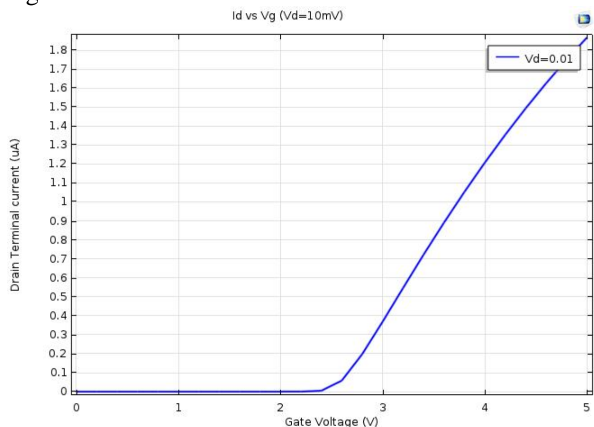

Fig. 6. Determining of the MOSFET threshold voltage.

Then, to get a better view to determining the operating point of the transistor, the drain's voltage–current characteristic diagram in several different gate voltage is plotted. Result shown in Figure 7. As can be seen in Figure 6, the threshold voltage of the MOSFET is about 2.4 V. According to the Figure 7, when the gate and drain voltage rises up to 5 and 2 V, respectively, it can be almost sure that the transistor is in the saturation region.

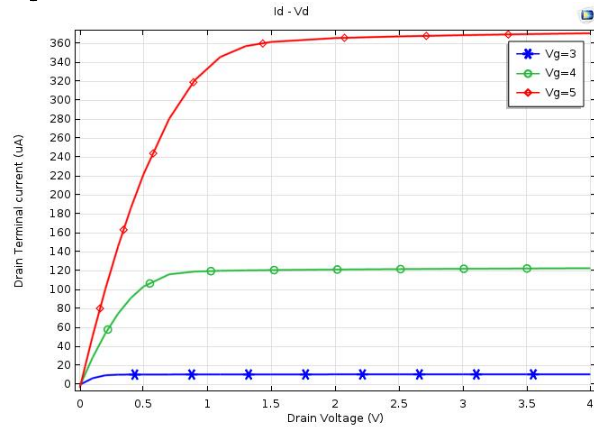

Fig. 7. The drain's voltage-current characteristic diagram in several different gate voltage.

The formed channel below the oxide can be seen in Figure 8.

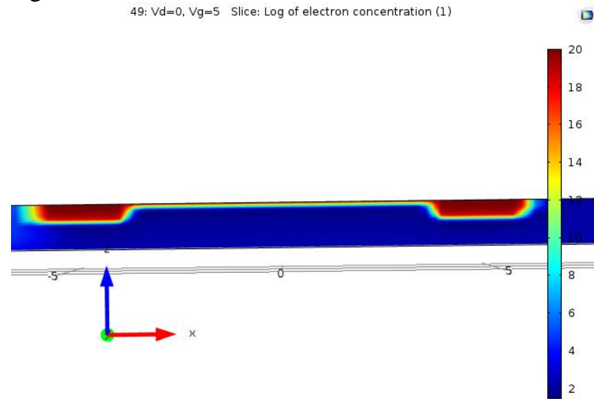

Fig. 8. Channel formed under the oxide by applying a voltage to the gate.

While the drain and gate voltages are 2 and 5, respectively, the oxide thickness will increase from 6 to 30 nm. Figure 9 shows the drain current in terms of oxide thickness diagram. As can be seen, and is expected, current changing versus change in the oxide thickness does not follow a linear relationship. And a changing about 20 nm in oxide thickness, will be followed with changing about 2 or 3 A in drain current.

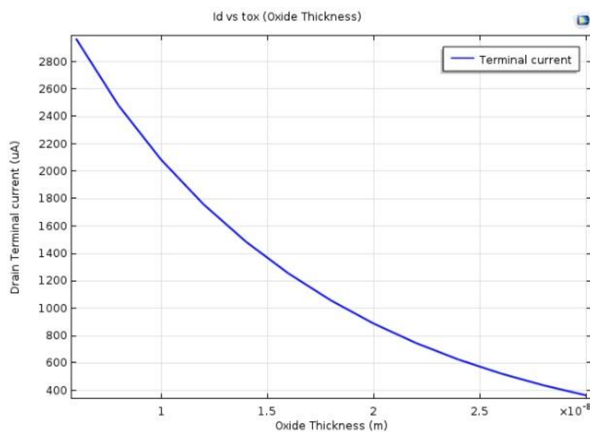

Fig. 9. Diagram of drain current in terms of oxide thickness.

The drain voltage – current characteristic diagram is plotted in Figure 10, to ensure that the transistor is not out of the saturation region.

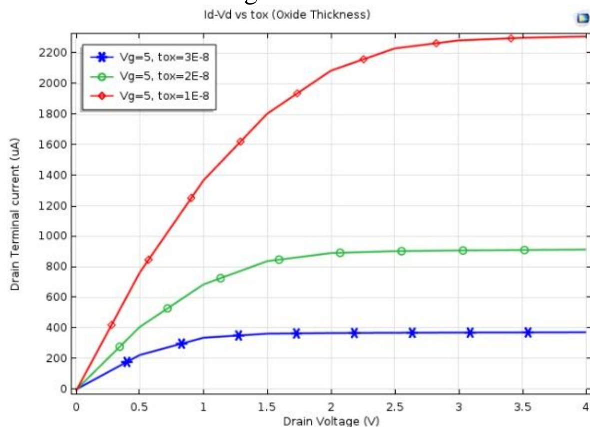

Fig. 10. Drain current-voltage characteristic diagram at different thickness of oxide.

3.3. Comparing the Results

Now, to comparison and verification the results, the diagrams resulting from MATLAB analysis and COMSOL simulation, were plotted together in Figure 11. As can be seen, the results are very close together, which confirms the validity of the model. Approximation and ignored parameters in the model, like potential across the oxide which is the result of the trapped charge in it, is the reason for little difference between the two graphs in Figure 11.

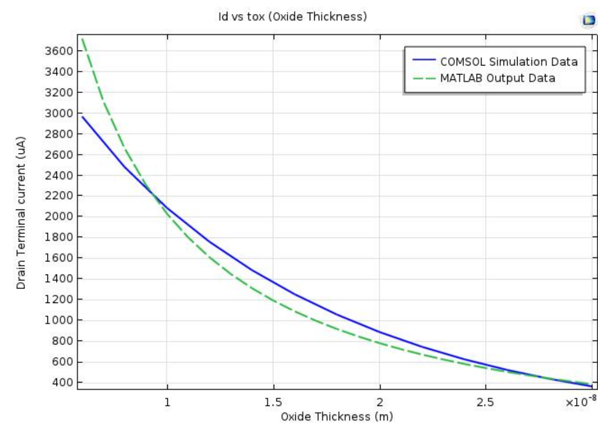

Fig. 11. Comparison of the MATLAB analysis and COMSOL simulation results.

4. CONCLUSION

At first, the general equation of the MOSFET's drain current in saturation region was rewritten in terms of the oxide thickness, and then it was simplified. That equation was analyzed using MATLAB, with a MOSFET, which designed based on 5 µm CMOS technology. Then, it was simulated using COMSOL software. At first, to select the appropriate operation point, it must be found the threshold voltage of the transistor, after finding it, and to see the different operation region of transistor, the drain's voltage–current characteristic diagram in several different gate voltage is plotted. After the transistor appropriate operation point was found, with sweeping the transistor oxide thickness from 6 to 30 nm, drain current changing was plotted, with comparison of it with the MATLAB result, the accuracy of the mathematical model confirmed.

REFERENCES

[1] C. C. Hu, **"Modern Semiconductor Devices for Integrated Circuits"**, *California, Berkeley: Prentice Hall,* 2009.

[2] M. Zabeli, N. Caka, M. Limani and Q. Kabashi, **"The impact of MOSFET's physical parameters on its threshold voltage, "** in *6th WSEAS Int. Conf. Microelectronics, Nanoelectronics, Optoelectronics*, Istanbul, Turkey, 2007.

[3] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara and S. Miyazaki, **"Limit of Gate Oxide Thickness Scaling in MOSFETs due to Apparent Threshold Voltage Fluctuation Induced by Tunnel Leakage Current, "** *IEEE Trans. on Electron Device,* Vol. 48, No. 2, pp. 259-264, 2001.

[4] I. Safayat-Al, **"Effects of gate insulator thickness and diameter over on/off current ratio in ballistic CNTFETs, "** *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,* Vol. 2, No. 11, pp. 5424-5429, 2013.

[5] N. Gupta, **"Threshold voltage modelling and gate**

oxide thickness effect on polycrystalline silicon thin-film transistors, " *IOP Publishing, Physica Scripta,* Vol. 76, pp. 628-633, 2007.

[6] S. M. Sze and K. K. Ng, **"Physics of Semiconductor Devices"**, *Wiley-Interscience*, 2006.