A 0.4V, 790µW CMOS low noise amplifier in sub-threshold region at 1.5GHz

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ABSTRACT:
A fully integrated low-noise amplifier (LNA) with 0.4V supply voltage and ultra low power consumption at 1.5GHz by folded cascode structure is presented. The proposed LNA is designed in a TSMC 0.18 µm CMOS technology, in which all transistors are biased in sub-threshold region. Through the use of proposed circuit for gain enhancement in this structure and using forward body bias technique, a very high figure of merit is achieved, in comparison to similar structures. The LNA provides a power gain of 14.7dB with a noise figure of 2.9dB while consuming only 790µW dc power. Also, impedance matching of input and output of the circuit in its operating frequency is desirable and in the whole bandwidth of the circuit, input and output isolation is below -33dB.

KEYWORDS: Low noise amplifier, folded cascode structure, forward body bias, ultra low power, ultra low voltage.

1. INTRODUCTION

Increasing demands for mobile wireless systems have stimulated the development of radio frequency integrated circuits (RFICs). Reduction in power dissipation causes battery to last longer in these systems. In applications like wireless medical telemetry, low power consumption plays a significant role. In such applications, the portable device should be able to work with ultra low supply voltage or environment energy such as solar cells. As a result, the power consumption and supply voltage are two essential parameters which should be optimized by the designer [1]. Considering that LNA is a key part in the RF front-end receivers, designing this stage is full of trade-offs between input and output impedance matching, minimum noise figure, appropriate gain, high linearity, and satisfactory isolation between output and input of amplifier. Additionally, in portable systems, optimization and developing a balance between the above mentioned parameters would be more complicated, considering power consumption and supply voltage. One of the restrictions in designing LNAs with low power consumption is threshold voltage (V_t) of MOSFETs and it has been a serious challenge for manufacturers of semiconductor devices to reduce it [2]. So far, some techniques have been offered for reducing power dissipation and supply voltage such as biasing transistors in sub-threshold region and applying forward body bias in order to reduce threshold voltage (V_t) [3-5]. Also, using non-stacking structures such as complementary current-reused structure and folded cascode structure would be effective in reducing supply voltage [6-9], but, on the other hand, in sub-threshold biasing state, the gain of amplifier would decrease and noise figure would increase. Also, in non-stacking structures, there is weak isolation between input and output. Considering the research done into this subject, little research on LNAs has been reported with ultra low supply voltage and ultra low power, simultaneously [7]. In this study, it is attempted to present an LNA with 0.4V supply voltage and 790µW power consumption and high figure of merit by considering all aspects of designing LNAs with ultra low supply voltage and ultra low power consumption.

This paper is organized as follows. In Section II, folded cascode structure is reviewed in brief. In section III, proposed LNA and related topics are introduced. In section IV simulation results are described and compared to other reported LNAs. Section V gives the conclusion.

2. LNA WITH FOLDED CASCODE STRUCTURE

Folded cascode structure is one of the conventional structures for designing low noise, low voltage amplifiers (Fig. 1). Transistors M1 and M2 form the first and second stage of this structure, respectively. Inductances L_g and L_s are used for impedance matching of input, and inductance-capacitance network (L_o and C_o) of output is employed for impedance matching of output.

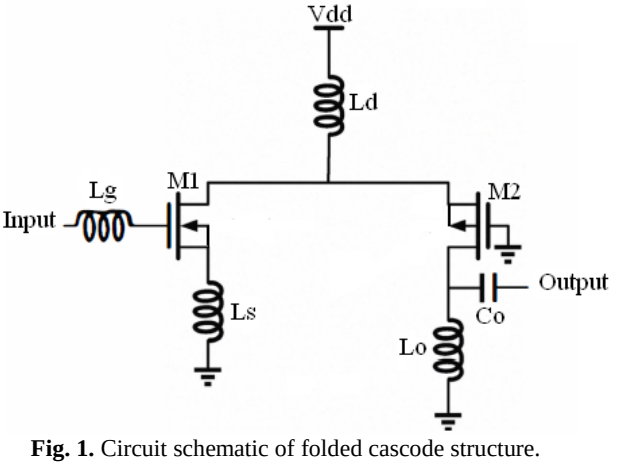

Fig. 1. Circuit schematic of folded cascode structure.

Due to the absence of stacking gain stages, it is possible to reduce supply voltage up to the threshold voltage. In addition, it is feasible to slightly reduce threshold voltage by using forward body bias technique [8,9]. Furthermore, in folded cascode structure, parasitic capacitors in drain of the common source transistor (M1) simply resonate with inductance L_d at the operating frequency and their effect is obviated and reduces noise share of common gate transistor (M_2) in output.

One of the shortcomings in the above mentioned amplifier structure is its fairy low gain [8]. Particularly in designing amplifiers with ultra low supply voltage and power consumption with transistors in sub-threshold region, transconductance of transistors decrease dramatically compared to strong inversion region. The decline in transistors transconductance on the one hand causes a decrease in gain and on the other hand leads to a rise in noise figure of amplifier. The modified structure to overcome the above mentioned problems has been presented in the following section.

3. PROPOSED LNA

Fig. 2 illustrates proposed LNA's schematic circuit. In Fig. (2) capacitors C_1 and C_2 are coupling capacitors and resistor R_1 connects gate of transistor M_2 to the ground in DC mode. In order to reduce power consumption, all transistors are biased in sub-threshold region. In this region, current of MOSFETs' drain (I_d) and their transconductance (g_m) is given by:

$$I_d = I_0 \exp(\frac{V_{gs}}{\zeta V_t}) \quad (1)$$

$$g_m = \frac{I_0}{\zeta V_t} \exp(\frac{V_{gs}}{\zeta V_t}) \quad (2)$$

Where ζ is the nonideal factor, V_{gs} is the gate-to-source voltage and V_t is the threshold voltage of transistor.

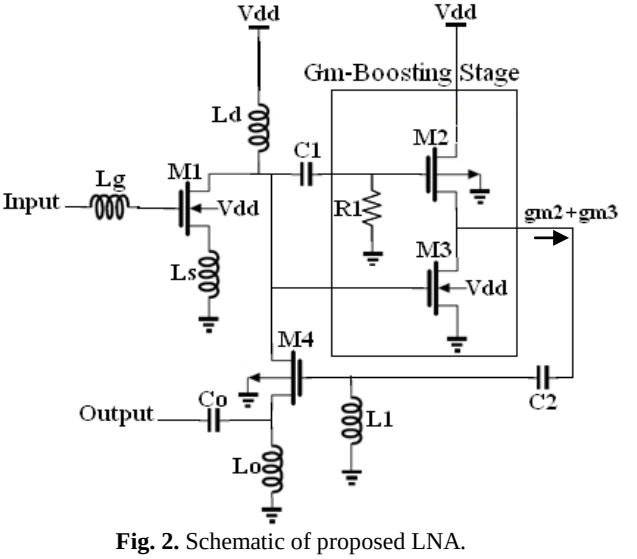

Fig. 2. Schematic of proposed LNA.

Forward body bias technique is employed to reduce supply voltage of the circuit and prevent a substantial drop in transistors transconductance in sub-threshold region. Also, to boost amplifier's gain in sub-threshold region, the circuit shown in square in Fig 2 is added to the folded cascode structure by using G_m-boosting technique [10].

Input signal is amplified by transistor M_1 and then amplified by added stage including transistors M_1 and M_2 and applied to the gate of transistor M_4. Thus, gate-to-source voltage of this transistor increases and leads to an increase in its effective transconductance.

As it can be seen from Fig. 2, transistors M_1 and M_2, added to folded cascode structure, do not lead to an increase in supply voltage of the circuit. Also, considering that these two transistors consume the same current, and output transconductance of this stage is the result of transconductances of transistors M_1 and M_2, added together ($g_t=g_{m2}+g_{m3}$), it is possible to lower this stage's current consumption by selecting an appropriate width for these two transistors. Therefore, the proportion of power consumption to total transconductance of this stage would be insignificant in comparison to common source and common gate stages. In other words, this stage raises total gain of the circuit with ultra low power consumption. Power consumption of each stage and transistors'

transconductance with 0.4V supply voltage is presented in table I. The length of all transistors is 0.18µm.

Table I. Power consumption of the stages and transconductance of transistors.

	Stage 1 (M_1)	**Stage 2 (M_2 & M_3)**	**Stage 3 (M_4)**
Width (µm)	46×8	64×8 , 22×8	64×8
P_{DC} (µW)	444	176	168
g_m (mA/V)	21	8.5+8.2	8

3.1. Forward body bias technique

Threshold voltage (V_t) in MOSFETs is defined as:

$$V_{th} = V_{th0} + \gamma(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}) \quad (3)$$

where V_{th0} is the threshold voltage when V_{bs}=0, γ is the body-effect coefficient, φ_f is the bulk fermi potential, V_{bs} is the body-to-source voltage. According to equation (3), the threshold voltage can be reduced by applying V_b>V_s for n-type transistors and V_b<V_s for p-type transistors.

Fig. 3 demonstrates Simulated threshold voltage (V_{th}), drain current (I_d) and body leakage current (I_{body}) of the MOSFET with a forward body bias for n-type transistor where its width is W=46×8µm and length is L=0.18µm. Applied body biasing voltage is much lower than the turn-on voltage of P-N junction between body and source in MOSFETs (0.7). Thus, the body leakage current could then be negligible.

For p-type transistors with similar scaling and biasing conditions, by applying V_{body}=0V, body leakage current and threshold voltage are 2µA and 0.41V, respectively.

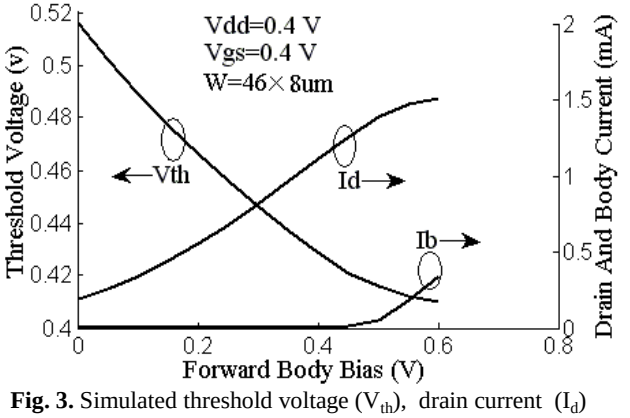

Fig. 3. Simulated threshold voltage (V_{th}), drain current (I_d) and body leakage current (I_{body}) of the MOSFET with a forward body bias sweeping from 0 V to 0.6 V.

3.2. Circuit analysis

One of important parameters in designing LNAs is noise figure which is significantly affected by input stage. Noise figure in multistage amplifiers is expressed as follows:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \ldots + \frac{NF_m - 1}{A_{p1}\ldots A_{p(m-1)}} \quad (4)$$

From (4), added stage to folded cascode structure causes gain boosting and consequently improves in noise figure. Due to the use of the inductive degeneration technique, noise and power matching in input can be simultaneously achieved. To have a better understanding of the input matching in first stage, the noise equivalent circuit of the first stage is demonstrated in Fig. 4.

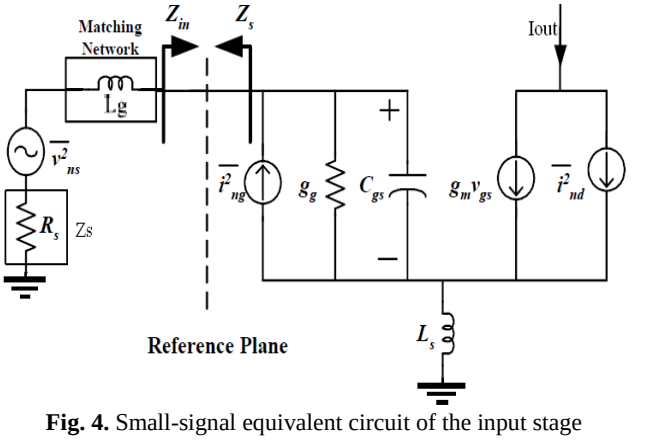

Fig. 4. Small-signal equivalent circuit of the input stage with noise sources.

Where $\overline{V_{ns}^2}$ represent the mean-square value of the circuit input noise source, $\overline{i_{ng}^2}$ is the mean-squared value of induced gate noise current, and $\overline{i_{nd}^2}$ is the mean-squared value of the channel thermal noise current. The expressions of the noise currents in MOSFETs are given by:

$$\overline{i_{nd}^2} = 4KT\gamma g_{d0}\Delta f \quad (5)$$

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f \quad (6)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \quad (7)$$

In above equations, K is Boltzmann constant, T is the absolute temperature on the Kelvin scale, γ is a constant with a value of 2/3 for long-channel devices, g_{d0} is transistor's transconductance when drain-to-source voltage (V_{ds}) is zero and Δ_f is band width. In (6), δ is a constant with a value of 4/3 for long-channel devices. By calculating total output noise current, $\overline{i_{nout,tot}^2}$,in the small-signal equivalent circuits of the input stage, and divide it by output noise current of the

circuit derived from input noise source, $\overline{i_{nsout}^2}$, minimum noise figure of the circuit (F_{min}), noise resistance (R_n)and the optimum source impedance (Z_{opt}) to reach optimum noise can be derived as follows:

$$R_n = \frac{\gamma}{\alpha g_{m1}} \tag{8}$$

$$F_{\min} = 1 + \frac{2\omega}{\sqrt{5}\omega_T}\sqrt{\gamma\delta(1-C^2)} \tag{9}$$

$$Z_{opt1} = j(\frac{1}{\omega C_{gs}} - \omega L_s) + \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|C|^2)}}}{\omega C_{gs}\left[\frac{\alpha^2\delta}{5\gamma(1-|C|^2)} + (1+\alpha|C|\sqrt{\frac{\delta}{5\gamma}})^2\right]} \tag{10}$$

Where $\alpha=g_{m1}/g_{d0}$ and C is a correlation coefficient of gate noise to channel noise and equals to 0.395j for long-channel transistors. Based on small signal analysis, input impedance of first stage can be derived as:

$$Z_{in1} = j(\omega L_s - \frac{1}{\omega C_{gs}}) + \frac{g_m L_s}{C_{gs}} \tag{11}$$

According to (10) and (11), for simultaneous power and noise matching, the following condition should be met:

$$Z^*_{in1} = Z_{opt1} = Z_s \tag{12}$$

By carefully choosing transistor's parameters, it is possible to make real part of optimum noise impedance equal to real part of input impedance in operating frequency of the circuit.

$$\frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|C|^2)}}}{\omega_0 C_{gs}\left[\frac{\alpha^2\delta}{5\gamma(1-|C|^2)} + (1+\alpha|C|\sqrt{\frac{\delta}{5\gamma}})^2\right]} = \frac{g_m L_s}{C_{gs}} \tag{13}$$

By employing input matching network (L_g), according to (12), to have maximum power gain and minimum input return loss, amount of inductances L_g and L_s at operating frequency of the circuit can be derived from (14) and (15) by choosing proper size for M_1. Input source impedance (R_s) is assumed to be 50Ω.

$$L_g = \frac{C_{gs}R_s}{g_m} \tag{14}$$

$$(L_g + L_s)C_{gs}\omega_0^2 = 1 \tag{15}$$

In scaling of transistors M_2 and M_3 charge carrier mobility in transistor (μ_x) should be considered. Considering that electron mobility (μ_n) in n-type transistors is 2.5 to 3 times more than hole mobility (μ_p) in p-type transistors. Therefore, size of transistor M_2 should be chosen correspondingly larger than transistor M_3 size.

4. SIMULATION RESULTS

The proposed LNA has been simulated by HSPICE RF simulator using 0.l8µm CMOS process BSIM3 model. Spiral inductors are used as inductors and metal-insulator-metal (MIM) capacitors are used as capacitors in simulation. Characteristics of applied devices in simulation are tabulated in table II.

Table II. Characteristics of applied devices in simulation.

Devices	Design Values
M_1	46×8µm/0.18µm
M_2	64×8µm/0.18µm
M_3	22×8µm/0.18µm
M_4	64×8µm/0.18µm
L_s	N=1,R=35µm
L_g	N=5.5,R=125µm
L_d	N=4,R=115µm
L_1	N=2,R=125µm
L_o	N=4.5,R=112µm
C_o	0.6pF

N: Number Of Inductor Turns, R: Inner Radius of Inductor, For All Inductors W=15µm.

Proposed LNA operates with 0.4V supply voltage and consumes 790µW power. Figures 5 and 6 show input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}), respectively. Noise figure of the circuit (NF) and minimum noise (F_{min}) are shown in Fig. 7. It can be seen from Fig. 7 that noise figure of the circuit in frequency of 1.5GHz is very close to F_{min} which indicates the desirability of noise matching in input. Gain power (S_{21}) and reverse isolation (S_{12}) are depicted in Fig. 8 and Fig. 9, respectively. In 1.5GHz, noise figure and power gain are 2.9dB and 14.7dB, respectively. Also, input reflection coefficient is -11dB and output reflection coefficient is less than -20dB. In whole bandwidth of the circuit, isolation is less than -33dB.

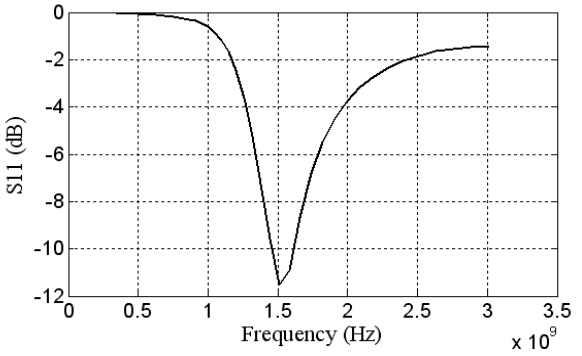

Fig. 5. Simulated input reflection coefficient.

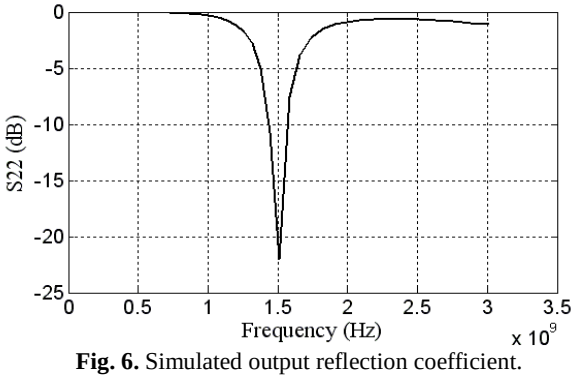

Fig. 6. Simulated output reflection coefficient.

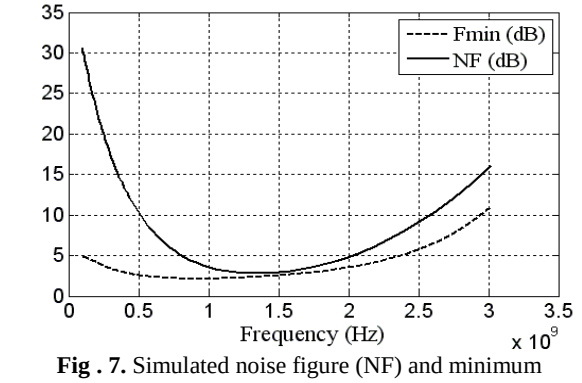

Fig . 7. Simulated noise figure (NF) and minimum noise(F_{min}).

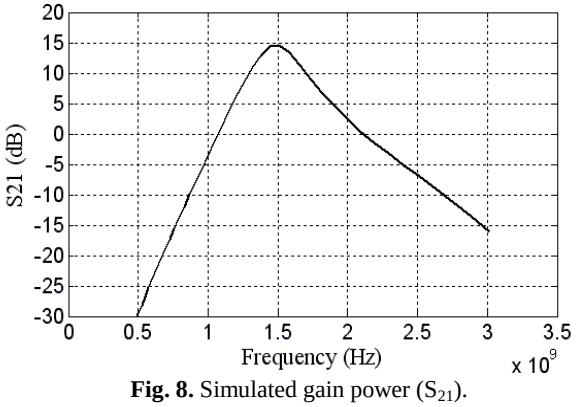

Fig. 8. Simulated gain power (S_{21}).

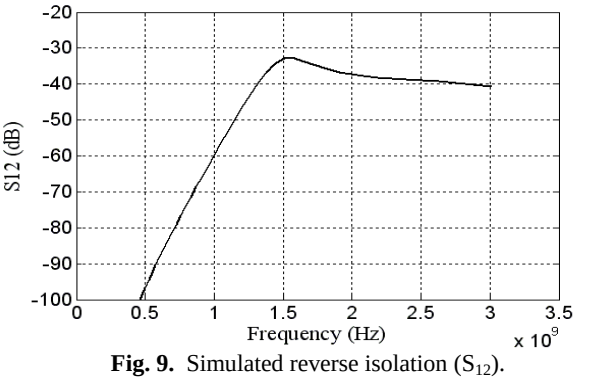

Fig. 9. Simulated reverse isolation (S_{12}).

In order to evaluate linearity of the proposed LNA, a two-tone test was conducted. For this purpose, two single-tone signals with identical power at the frequencies of 1.5GHz and 1.51GHz were applied to the circuit to measure 1dB compression point and input third order intercept point ,IIP3 (Fig. 10). The 1dB compression point and the input third order intercept point were measured as -11.14dBm and -23dBm, respectively.

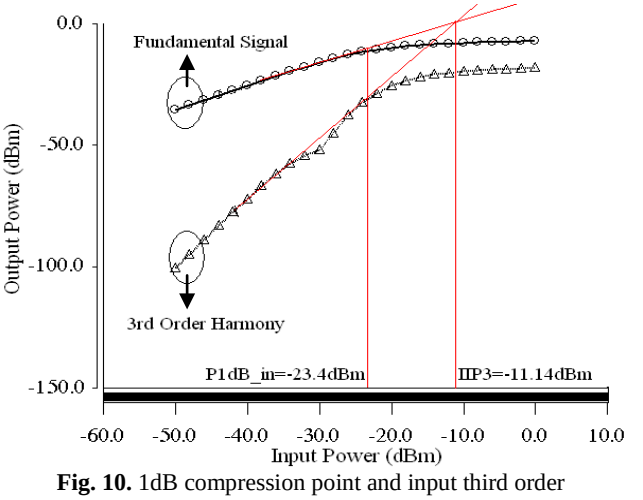

Fig. 10. 1dB compression point and input third order intercept point (IIP_3).

To evaluate the performance of LNAs and to draw a better comparison between them, various figures of merit are defined and used. A commonly used figure of merit (FOM_1) is the ratio of power gain to dc power consumption. Furthermore, it can be extended to include the NF and supply voltage as follows [9]:

$$FOM_2 = \frac{Gain[abs]}{NF[abs].V_{DD}[v].P_{DC}[mW]} \quad (16)$$

FOM_1 and FOM_2 for proposed LNA are 18.6(dB/mW) and 8.81$(V.mW)^{-1}$ respectively. Table III summarizes the performances of the proposed LNA and data included in previously published works for comparison.

5. CONCLUSION

In this paper, an ultra low voltage, ultra low power LNA in 0.18µm CMOS technology is presented. By adding proposed circuit for gain boosting (G_m-boosting stage) to folded cascode structure and using body bias technique, performance of the circuit in sub-threshold region was improved significantly, with only a slight increase in power consumption. Proposed LNA at 0.4V supply voltage and 0.790µW power consumption has a gain of 14.7dB and noise figure of 2.9dB and at the operating frequency, has the desirable input and output impedance matching. Moreover, considering the simulation results, proposed LNA is perfectly suitable for ultra low voltage and ultra low power applications.

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Table III. Performances summary and comparison of this work and prior published LNAs.

Ref.	This Work	[9]	[12]	[5]	[8]	[4]	[3]	[11]
F_0(GHz)	1.5	1.5	1.5	5	5.2	5.1	3	1.6
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.13	0.13	0.18
V_{DD}(v)	0.4	0.5	0.6	0.6	0.6	0.4	0.6	0.6
Power(mW)	0.79	2.5	2.6	0.8	1.08	1.03	0.4	1.2
NF(dB)	2.9	1.9	2.1	4.1	3.37	5.3	4.7	4.8
S_{21}(dB)	14.7	22	23.1	10.23	10	10.3	9.1	6.4
S_{11}(dB)	-11.5	-9.5	-14	-17.9	-13.4	-17.7	-13	---
S_{22}(dB)	-22	-9.5	-14	-10.6	-10.6	-11.4	-20	---
IIP_3(dBm)	-11.1	-12.5	---	-15	-8.6	---	-11	---
FOM_1	18.60	8.80	8.88	12.79	9.26	10	22.75	5.33
FOM_2	8.81	6.50	5.64	2.63	2.24	2.34	4.02	0.97
Year	2012	2011	2009	2009	2008	2007	2006	2004