A New Dual-Frequency LC oscillator: Analysis and Design

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ABSTRACT:
In this paper, a new dual-frequency LC oscillator is introduced. This new architecture is designed taking the advantage of a Wheatstone-bridge LC resonator concept that enables the oscillator to generate two different frequencies simultaneously. In contrast to previous designs, no transistor switches are incorporated in the structure of this dual-frequency circuit. So, the proposed configuration is suitable for low phase noise applications. The performance of the oscillator has been verified using circuit simulations in 0.18 μm CMOS technology. Circuit simulations show phase noises of -109 dBc/Hz and -105 dBc/Hz for 1.8 GHz and 2.7 GHz frequency bands respectively in 100 kHz offset frequency.

KEYWORDS: Dual-frequency oscillator, LC oscillator, oscillator, phase noise.

1. INTRODUCTION

Recent advances in wireless communication networks caused a great interest in the systems with capabilities of operating in multiple frequency bands or compatible with different standards [1] [2]. Local and voltage controlled oscillators are essential parts of many communication systems [3] [4]. But, a simple oscillator is not capable of producing pure and low phase noise signal in a wide range of frequency. So, this will be more desirable to design the oscillators with the capability of producing two or more frequency bands. A simple and primitive way of implementing multi-frequency system is to use multiple oscillators for different frequency bands and switching between them [5]. But, this will increase the fabrication cost and also the power consumption of the system. Therefor, it is more preferable to design one oscillator which can oscillate in two or more different frequencies. The major issue in designing of multi frequency oscillators is when they switch between different frequencies modes; the phase noise performance of the oscillator will be degraded [6]. This is mostly because of the transistor switches used in the major signal path which adds unwanted noise sources to the circuit [7]. Recently, a mode switching design has been proposed in [8] to solve this problem. However, the privious works can not produce two frequencies simultaneously.

This work represents a dual-band *LC* oscillator which uses a Wheatstone bridge resonator. As shown in Figure. 1, the new architecture does not include any swiches or additional circuits connected to the *LC* tank. Therefore, it provides frequency swiching without degrading phase noise performance. Also, it has the ability to generate two different pure frequencies at the same time.

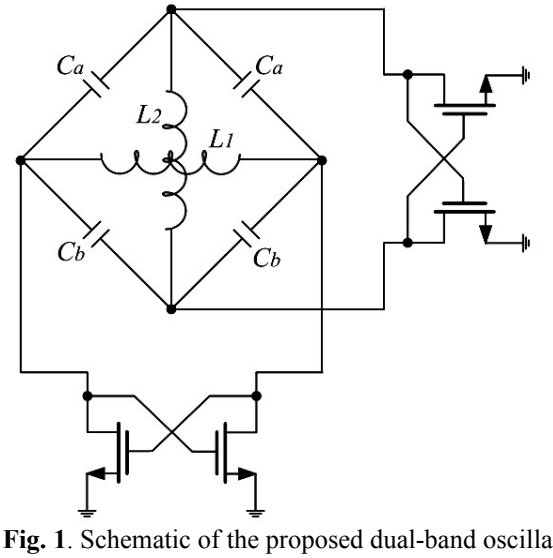


Fig. 1. Schematic of the proposed dual-band oscillator.

2. CIRCUIT ANALYSIS

2.1. LC Tunk

As illustrated in Figure 2, the designed *LC* tank consists of a Wheatstone-bridge structure. If the resonator is stimulated from Port1, then we will have a zero voltage across Port2 because the capacitors produce a balanced Wheatstone-bridge and therefore, L_2 will be idle and similarly, if the resonator is stimulated from Port2 then Port1 (L_1) experiences a zero voltage and L_1 will be idle.

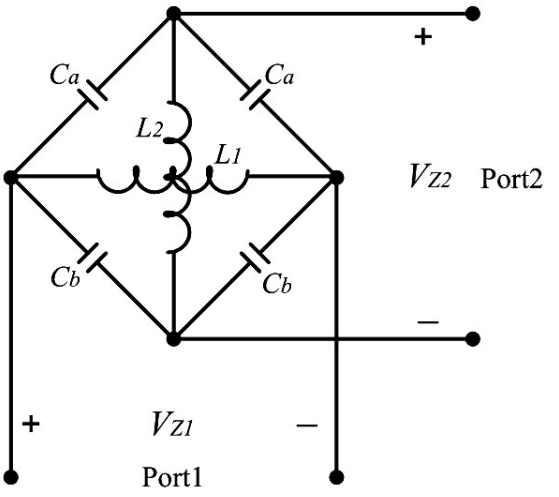


Fig. 2. Proposed Wheatstone-bridge *LC* resonator.

Therefore, from Port1 point of view, the resonator acts as a *LC* tank with resonant frequency of

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}}, \quad C_1 = \frac{C_a + C_b}{2} \tag{1}$$

And from Port2 point of view, the resonator acts as a *LC* tank with resonant frequency of

$$\omega_2 = \frac{1}{\sqrt{L_2 C_2}}, \quad C_2 = \frac{2C_a C_b}{C_a + C_b} \tag{2}$$

This claim will be verified if we model the resonator of Figure 2 as a two port network and write its impedance matrix (Z matrix) as follow

$$Z(s) = \begin{pmatrix} \dfrac{2}{C_1 + C_2} s & 0 \\ \dfrac{}{(s^2 + \omega_1^2)} & \\ 0 & \dfrac{C_1 + C_2}{2C_1 C_2} s \\ & \dfrac{}{(s^2 + \omega_2^2)} \end{pmatrix} \tag{3}$$

The two resonant frequencies are clearly shown by Z_{11} and Z_{22} elements. Also $Z_{12}=Z_{21}=0$ approves the Wheatstone-bridge based nature of the resonator and shows that the two ports are acting independently. As an illustration, the impedances seen from the two ports $|Z_{11}(j\omega)|$ and $|Z_{22}(j\omega)|$ of a typical resonator of Figure 2 are simulated and plotted in Figure 3. As predicted by the analysis, $|Z_{11}(j\omega)|$ and $|Z_{22}(j\omega)|$ experience their peak values at two different frequencies.

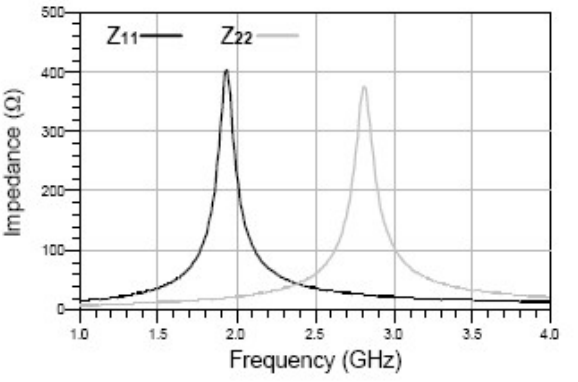


Fig. 3. Simulated Z_{11} and Z_{22} of the LC tank.

2.2. Considering of The Conductance Parameters

Figure 4 illustrates the oscillator structure considering the trans-conductance parameters. In Figure 4

- G_1 is the parallel conductance of the inductor L_1.
- $-G_{m1}$ is the negative conductance of the active MOS differential pair connected to the Port1.
- G_2 is the parallel conductance of the inductor L_2.
- $-G_{m2}$ is the negative conductance of the MOS differential pair connected to the Port2.

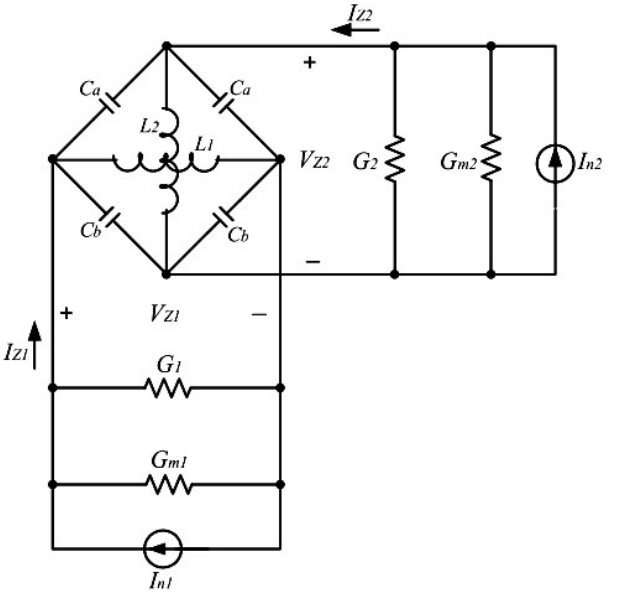


Fig.4. Two port network model of the proposed oscillator considering the trans-conductance parameters.

Now, considering the model in Figure 4, the impedance matrix of the two port oscillator network is derived as

$$Z(s)=\begin{pmatrix} \dfrac{\dfrac{2}{C_a+C_b}s}{s^2+\dfrac{2(G_1-G_{m1})}{C_a+C_b}+\omega_1^2} & 0 \\ 0 & \dfrac{\dfrac{C_a+C_b}{2C_aC_b}s}{s^2+\dfrac{(C_a+C_b)(G_2-G_{m2})}{2C_aC_b}+\omega_2^2} \end{pmatrix} \quad (4)$$

Based on the presented mathematical model, the response of the oscillator to the input noise current sources I_{n1}, I_{n2} of the Port.1 and Poert.2 respectively will be calculated as

$$\begin{pmatrix} V_{Z1} \\ V_{Z2} \end{pmatrix}(s)=(Z)\begin{pmatrix} I_{n1}(s) \\ I_{n2}(s) \end{pmatrix} \quad (5)$$

And from (4)

$$V_{Z1}(s)=\frac{\dfrac{2}{C_a+C_b}s}{s^2+\dfrac{2(G_1-G_{m1})}{C_a+C_b}+\omega_1^2}.I_{n1}(s) \quad (6)$$

$$V_{Z2}(s)=\frac{\dfrac{C_a+C_b}{2C_aC_b}s}{s^2+\dfrac{(C_a+C_b)(G_2-G_{m2})}{2C_aC_b}+\omega_2^2}.I_{n2}(s) \quad (7)$$

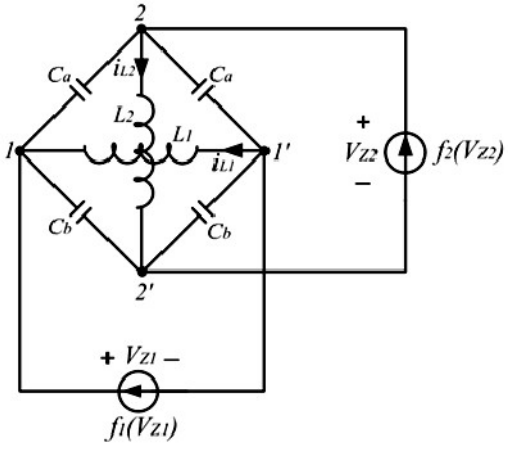


Fig. 5. Nonlinear model of the proposed dual-band oscillator.

Therefore, if we design the circuit with $G_{m1} > G_1$ then V_{Z1} has its poles on the right half plane and Port1 will oscillate with the frequency of ω_1. Also, if $G_{m2} > G_2$, then, Port2 will oscillate with frequency of ω_2. It should be noted that the ports will oscillate independently and therefore, we will have oscillation with frequency of ω_1 in Port1 and at the same time Port2 will oscillate with frequency of ω_2. This specification is resulted from the Wheatstone-bridge structure of the *LC* resonator. Considering Figure 5, this result can also be verified by writing the differential equation governing the circuit [9] [10]. In Figure 5

- $f_1(V_{Z1})$ is the nonlinear I-V characteristic of the differential pair connected to the Port1 and $V_{Z1}=V_1-V_{1'}$.
- $f_2(V_{Z2})$ is the nonlinear I-V characteristic of the differential pair connected to the Port2 and $V_{Z2}=V_2-V_{2'}$.

Writing *KCL* equations at nodes *1, 1', 2* and *2'* results in the following equations respectively

$$-f_1(V_{Z1})+C_b\frac{d(V_1-V_{2'})}{dt}+C_a\frac{d(V_1-V_2)}{dt}+i_{L1}=0 \quad (8.a)$$

$$f_1(V_{Z1})+C_b\frac{d(V_{1'}-V_{2'})}{dt}+C_a\frac{d(V_{1'}-V_2)}{dt}-i_{L1}=0 \quad (8.b)$$

$$-f_2(V_{Z2})+C_a\frac{d(V_2-V_1)}{dt}+C_a\frac{d(V_2-V_{1'})}{dt}+i_{L2}=0 \quad (8.c)$$

$$f_2(V_{Z2})+C_b\frac{d(V_{2'}-V_1)}{dt}+C_a\frac{d(V_{2'}-V_{1'})}{dt}-i_{L2}=0 \quad (8.d)$$

Taking derivatives of (8.a) and (8.b) and subtracting them results in (9) which is the nonlinear differential equation governing on Port1.

$$\frac{d^2V_{Z1}}{dt^2}-\frac{2}{C_a+C_b}\frac{df_1(V_{Z1})}{dt}+\omega_1^2V_{Z1}=0 \quad (9)$$

Also, multiplying (8.c) and (8.d) by C_b and C_a respectively and subtracting them results in (10) which is the nonlinear differential equation governing on Port2.

$$\frac{d^2V_{Z2}}{dt^2}-\frac{C_a+C_b}{2C_aC_b}\frac{df_2(V_{Z2})}{dt}+\omega_2^2V_{Z2}=0 \quad (10)$$

Interestingly, both of (9) and (10) independently show a form of a nonlinear *Van der Pol* equation of (11) which describes the behavior of second-order oscillatory systems [4].

$$\frac{d^2V}{dt^2}+\varepsilon F(V)+\omega_0^2V=0 \quad (11)$$

In (11), $\varepsilon F(V)$ models the characteristic of the nonlinear part of the system and ω_0 is the oscillation frequency. As seen, the nonlinear analysis also proofs the independent oscillations of Port1 and Port2.

3. PHASE NOISE ANALYSIS

Phase noise is one of the most important design parameters in oscillators. In dual-frequency oscillator designs, it is very important to design the circuit in a way that the frequency switching does not degrade the phase noise performance. In other words, phase noise performance of the dual-frequency oscillator should be same as the single frequency oscillator counterpart. So, here we have focused on a comparison between the phase noise performance of the designed oscillator and the single frequency counterpart. The phase noise analysis is based on impulse sensitivity function (ISF) method [11].

3.1. ISF Discussion

Firstly, consider a single frequency oscillator of Figure6. In this circuit, if an impulse noise current of $i_n = \delta(t-\tau)$ is injected to the *LC* tank, we will see a voltage jump of $\Delta V_O = 1/C$. This jump will cause a phase shift of $\Delta\varphi_0(\tau)$ depending on the state of oscillation at $t = \tau$. So, $\Delta\varphi_0(\tau)$ varies with the same frequency of the oscillator output voltage and it is called the ISF function [11]. Assuming that the maximum output voltage swing is V_p, ISF is calculated as

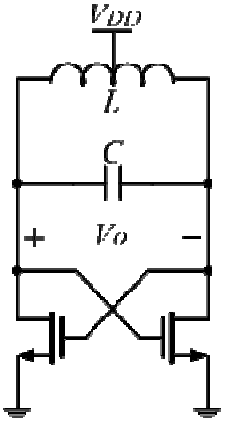


Fig. 6. A single-frequency oscillator.

$$\left|\mathrm{ISF}\right|_{\mathrm{Single}} = \left|\frac{\Delta V_O}{V_m}\right| = \frac{1}{CV_P}. \tag{12}$$

Now, consider the dual-frequency oscillator of Figure 1. If an impulse noise current is injected to the port1 of the *LC* tank, then it will cause to a voltage jump of $2/(C_a + C_b)$ across port1. Assuming that the oscillation swing in dual-frequency configuration is the same as the single frequency oscillator, ISF is calculated as

$$\left|\mathrm{ISF}\right|_{\mathrm{Dual}} = \left|\frac{\Delta V_O}{V_m}\right| = \frac{2}{(C_a + C_b)V_P}. \tag{13}$$

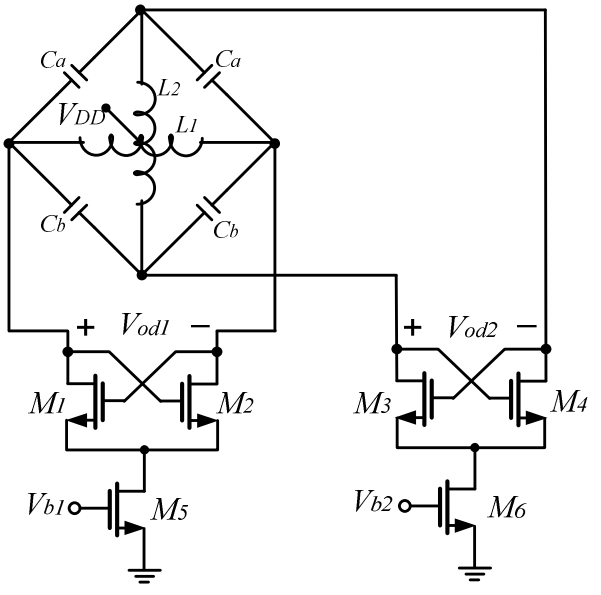
If the two oscillators use the same *L* and designed to operate at the same frequency, we must have $C = \frac{C_a + C_b}{2}$ and in this condition, from (12) and (13)

$$\left|\mathrm{ISF}\right|_{\mathrm{Dual}} = \left|\mathrm{ISF}\right|_{\mathrm{Single}}. \tag{14}$$

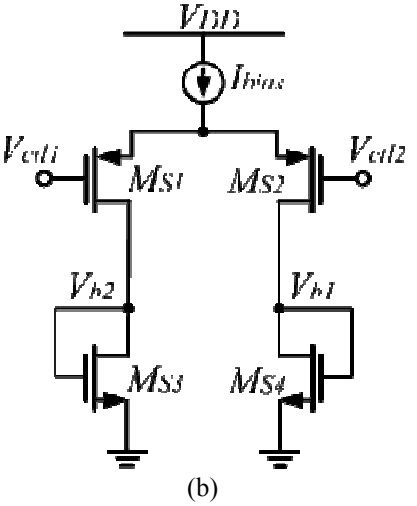
This means that the two oscillators have the same phase noise performance. Also, the same result will be obtained if we compare a single frequency oscillator and port2 of Figure 1.

4. CIRCUIT IMPLEMENTATION

The final schematic of the designed dual-frequency oscillator is shown in Figure 7. Each output port of the *LC* resonator tank is connected to a current biased cross-coupled CMOS pair to produce oscillation [9]. As discussed before, port1 will oscillate with ω_1 and port2 will oscillate with frequency of ω_2 independently. Also, a switching circuit is designed by M_{S1}-M_{S4} transistors for switching ON or OFF each frequency. As seen, this circuit is designed using a PMOS differential pair of M_{S1}, M_{S2} for current switching and two NMOS current mirrors of M_{S3}, M_{S4} for biasing of M5 and M6. If $V_{ctl1}=V_{ctl2}$, then all of M_{S1}-M_{S4} transistors are active with the drain current of $I_{bias}/2$. So, both of the cross-coupled pairs of M1-M2 and M3-M4 are biased through M5 and M6 and therefore, the oscillator will generate ω_1 and ω_2 oscillation frequencies at port1 and port2 respectively. Now, if for example, $V_{ctl1} > V_{ctl2}$ ($V_{ctl1} - V_{ctl2} = 2|V_{tp}|$), all of the I_{bias} current will flow through M_{S1}, M_{S3} transistors and M_{S2}, M_{S4} will be off. So, M1-M2 cross-coupled pairs are biased through M5 and port1 will oscillate with the frequency of ω_1. On the other hand, M3-M4 cross-coupled pairs are deactivated because M_{S2} and M_{S4} transistors are off and therefore, M6 is not biased and we will not have the oscillation with frequency of ω_2 at port2. Also, if $V_{ctl2} > V_{ctl1}$, then ω_1 will be deactivated whereas, port2 is oscillating with the frequency of ω_2.



(a)



(b)

Fig. 7. Implementation of the proposed dual-frequency oscillator (a) oscillator core circuit (b) frequency switching circuit.

5. SIMULATION RESULS AND DISCUSSIONS

In order to verify the presented dual-frequency oscillator concept and clarifying the analysis, the designed oscillator of Figure 7 has been simulated using Agilent Advanced Design System circuit simulator using 0.18 µm CMOS technology. The transistors sizes and element values are listed in Table1.

Firstly, the circuit is simulated choosing V_{ctl1}=V_{ctl2} and output wave forms at port1 (V_{od1}) and port2 (V_{od2}) are shown in Figure8. As seen, port1 is oscillating with the frequency of 1.8 GHz and port2 is oscillating with 2.7 GHz simultaneously as discussed in section2.

Table1. Transistor Sizes and Elements Values

Element		**Value**	
Thechnology		CMOS 0.18 µm	
V_{DD}		*1.8* volt	
I_{bias}		*5.4* mA	
Transistors dimensions (W/L) M1-M6		*20/0.2* (µm/µm)	
Transistors dimensions (W/L) M_{S1}-M_{S2}		*10/0.2* (µm/µm)	
Transistors dimensions (W/L) M_{S1}-M_{S2}		*20/0.2* (µm/µm)	
L_1	L_2	*1.5* nH	*0.8* nH
C_a	C_b	*3* pf	*6* pf

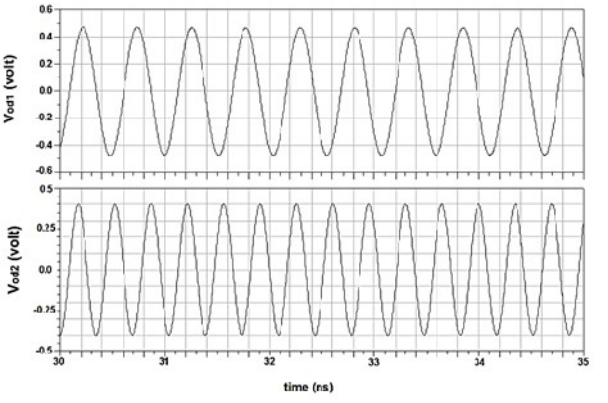


Fig. 8. Output voltages of the oscillator for V_{ctl1} = V_{ctl2}.

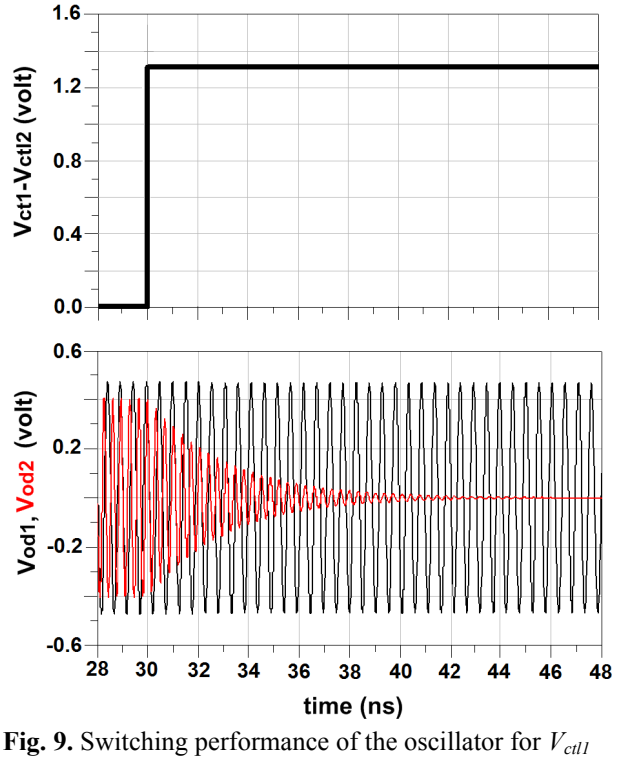


Fig. 9. Switching performance of the oscillator for V_{ctl1} - V_{ctl2} > *0*.

In next step, the switching performance of the oscillator is investigated by considering a voltage jump in V_{ctl1} - V_{ctl2} control voltage and the results are presented in Figure 9. As seen, when V_{ctl1} - $V_{ctl2} > 0$, the oscillation at port2 (ω_2) will be completely damped. Also, when $V_{ctl1} - V_{ctl2} < 0$, the oscillation at port1 (ω_1) will be completely damped and this verifies the acceptable performance of the switching circuit.

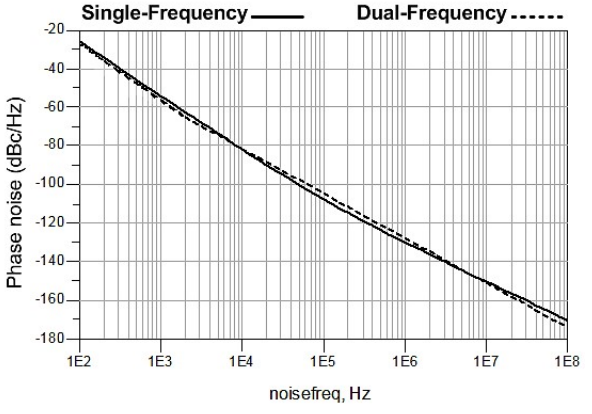


Fig. 10. Comparison between the phase noise of the single-frequency oscillator and the dual frequency oscillator for f_1=1.8 GHz oscillation frequency.

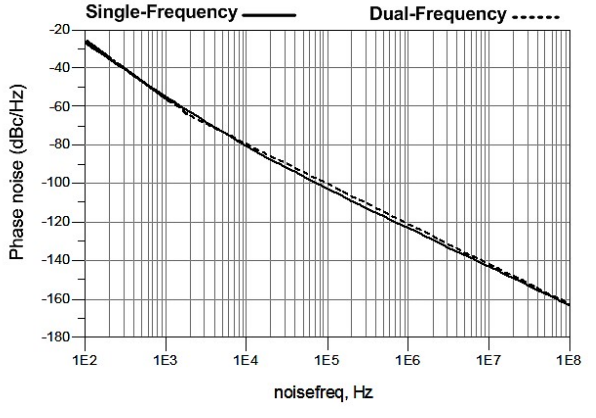


Fig. 11. Comparison between the phase noise of the single-frequency oscillator and the dual frequency oscillator for f_2=2.8 GHz oscillation frequency.

The phase noise analysis of the oscillator presented in section3 predicted that the phase noise performance of the dual-frequency oscillator in each of its frequency bands is the same as a single-frequency oscillator counterpart. In order to validate this prediction, two single-frequency oscillators have been designed separately with the oscillation frequencies of ω_1 and ω_2 like Figure6. Transistor sizing and element values of these two single-frequency oscillators are exactly the same as the designed dual-frequency oscillator for having an equal oscillation amplitude and fair comparison. Figure10 indicates the comparison between the phase noise behavior of single-frequency oscillator with oscillation frequency of ω_1 and the phase noise of the oscillation at port1. As seen, the phase noise performances are really close whereas the solid line con not be discriminated from the dashed one. Furthermore, the phase noise performance of the single-frequency oscillator of ω_2 is compared with the oscillation at port2 in Figure 11 showing the same result as Figure9 confirming the phase noise analysis of section3.

6. CONCLUSION

A new concept of dual-frequency oscillator has been proposed and designed for low phase noise applications. The proposed topology can provide two different output frequencies at the same time. Also, a switching mechanism is provided to switch ON or OFF each output frequencies without any switching transistors in critical signal path. A complete benchmark is provided using circuit simulations. The circuit simulations all verify the analysis and acceptable performance of the oscillator.

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