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System and Circuit Design of a SC 2-1-1 MASH Sigma-Delta Modulator for High Resolution and Low Power Applications

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Abstract:

In a switched-capacitor (SC) sigma-delta (∑Δ) analog-to-digital converter (ADC) with a large oversampling ratio (OSR), the first integrator of the loop filter is typically the largest consumer of power in the ADC. Without the noise shaping effect for the first integrator, maintaining thermal noise floor below the overall accuracy requirement of the modulator puts severe demands on the operational transconductance amplifier (OTA) power consumption. The ability of the multistage noise-shaping (MASH) structures to provide stable conversion has been utilized in this design for high resolution of the converter. In this paper, a MASH 2-1-1 switched capacitor sigma-delta converter (∑Δ ADC) with cascade structure has been presented. System level results show a signal to noise ratio SNR=146dB and a dynamic range of DR=151dB. Due to thermal and flicker noise of transistors and nonlinear effects of switches and Opamps, the SNR of circuit has decreased to SNR=133dB in circuit level. The high resolution of this type of the converter is ideal for applications in medical instruments and seismology. The designed sigma-delta converter has 24-bit resolution with 160Hz input signal bandwidth and consumes 26mW of power and SR=2.44V/μs.

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1. INTRODUCTION

Sigma-delta or delta-sigma (ΣΔ or ΔΣ) analog to digital converters are the best choice in low frequency and high precision applications. By exchanging speed for precision, these converters can achieve higher accuracy than any other convertors with low power consumption and simple structure. Sigma-delta converters are used in applications such as temperature and pressure measurement, industrial control process, accurate sensors of photography, medical and biomedical devices, especially in electrocardiogram (ECG) and electroencephalogram. The resolution of these converters has been reported to be in the range of 20-24 bits [1-5]. The sigma-delta converters use noise shaping principle to reduce quantization noise in the signal bandwidth. In this way high resolution can be achieved without high precision components. Therefore, these converters can be implemented using digital fabrication process without sophisticated analog components. The resolution of the sigma-delta converter increases with the order of the modulator in the system. In contrast, increasing order of modulator will result in instability.

Power consumption is one of the main constraints of sensory systems. Small output signals produced by sensors put severe demands on the power consumption of the interface circuits processing such signals [6]. In high resolution switched-capacitor (SC) systems with small inputs, for a given sampling capacitor size, a large oversampling ratio (OSR) is typically required to lower the thermal noise level below the accuracy requirement of the system, and this leads to an increased operational transconductance amplifier (OTA) power consumption. Even though technology scaling has considerably reduced the digital power in sensory systems, analog front-end circuits including the analog-to-digital converters (ADCs) have not benefited from scaling in terms of power dissipation [8, 9].

A common technique for digitizing sensory signals with high resolution and low bandwidth is to use a converter with a high OSR [6]. To reduce the power consumption within the scope of ADCs several techniques have been utilized. Double sampling effectively halves the required ADC sampling-rate, hence reduces its power consumption [12, 6].

OTA sharing has allowed the implementation of ADCs with only one OTA. Turning off the OTA for half a clock cycle has also been used to save analog power. Comparator-based switched-capacitor (CBSC) circuits replace the OTAs with more power efficient circuits such as comparators and current sources [15-6] .

to significantly reduce the OTA power consumption in thermal noise limited SC integrators proposed capacitive chargepumps (CPs) technique [18]. In another paper is described a circuit technique using capacitive charge pumps, to maintain the thermal noise performance of the integrator while reducing Its power dissipation to approximately a quarter of that of a conventional parasitic-insensitive SC integrator [13]. model is used to analyze the linearity and to select a suitable architecture for the $\Delta\sum$ modulator, that decision for proper structure of each MOSCAP depending on its significance on the output linearity [11]. In this paper MASH structure has been used to overcome the stability issue and increase resolution of the converter.

This paper has been arranged as follows. The principle of sigma-delta converters are discussed in section II. Section III describes MASH modulators. Section IV and V describe system and circuit implementation. Conclusion remarks are at the end.

2. SIGMA-DELTA CONVERSION PRINCIPLE

In terms of sampling frequency, analog to digital converters can be divided into two major categories: the Nyquist rate convertors and over-sampling converters [21]. In the Nyquist rate converters the analog input signal is sampled at Nyquist rate which is at least twice the maximum frequency component in the signal. In this type of convertor, there is a one-to-one correspondence between the output and the input signal. It is noteworthy to mention that these convertors are rarely used in high resolution converters because of low accuracy and difficulties to design a practical anti-aliasing filter. These types of converters include pipeline, flash, interpolating and folding analog to digital converters [1-6].

In over-sampling converters, analog input signal is sampled at multiples of the Nyquist frequency. The signal to noise ratio (SNR) of the ADC increases by filtering quantization noise out of the signal bandwidth. Sigma-delta converter is a good example of over-sampling converters. By noise shaping technique, over-sampling converters achieve high accuracy without using sophisticated analog components. These converters are resistant to non-ideal effects of analog circuits. The overall structure of a sigma-delta convertor is shown in the fig. 1 [1].

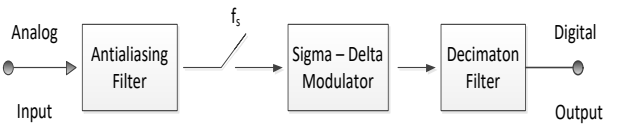

Fig. 1 Sigma-delta converter block diagram [1]

Analog input signal enters an antialiasing filter to eliminate folding effect after sampling. Using over-sampling technique to shape the quantization noise, sigma-delta modulator provides a medium speed and high precision signal at the output of the modulator. The output signal of the modulator is converted to a Nyquist rate digital signal using a decimation filter. The decimation filter eliminates the shaped noise and maintains digital nature of the modulator output by reducing sample rate. This filter reduces the sample rate to a reasonable level (Nyquist frequency). This step is called decimation or reduced rates [6]. Typically, a sigma-delta modulator samples input analog signal at high frequency, providing the output as a single-bit digital data stream.

Sigma-delta modulators are feedback modulators which prevent reinforced DAC errors by setting feedback gain to unity and large gain within the direct path to undermine the quantization error [10]. Nevertheless, DAC errors remain a major concern even in the sigma-delta modulators, since these errors are directly attached to the modulator input. Therefore, the nonlinearity of the DAC is indistinguishable from the input signal. In particular, linearity of DAC must match the linearity of the modulator. This issue is very important in modulators with high precision. To meet the high accuracy requirements of the DAC, a single bit quantizer is mainly used. A single-bit quantizer has only two levels of the output and changing these levels can only cause an offset gain error and no nonlinear effect. As a result, good linearity of the DAC and a good linearity of the whole modulator can be achieved. Fig. 2 shows a first-order sigma-delta modulator. This modulator consists of a discrete time integrator and a single bit quantizer [13-22].

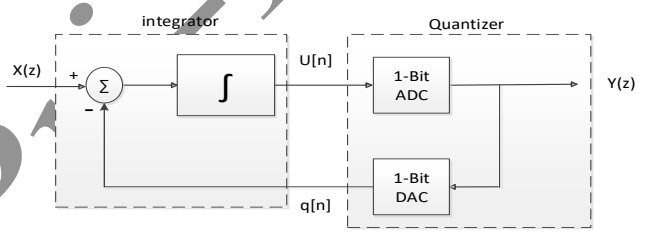

Fig. 2 A first-order single-bit sigma-delta modulator [6]

A mathematical model of the modulator is shown in fig. 3. Unfortunately, the definition of the quantizer gain (G) has no sense for a single-bit quantizer, because of undefined size of the input step. An approximation for quantizer gain, which is consistent with the simulation results and hardware implementation is a single gain approximation in which the gain G is selected to be equal to one.

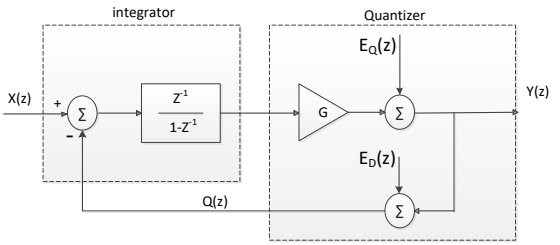

Fig. 3 linearized model of a first-order modulator [6]

Approximating G with 1 in fig. 3, modulator output will be as follows:

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)E_Q(z) - z^{-1}E_D(z) \quad (1)$$

Clearly, the output of the modulator is composed of three terms. The first is the input signal which is delayed by one sample. The second term is the quantization error which is filtered by the transfer function. This type of filtering is known as noise shaping where a zero at DC response of the transfer function attenuates quantization noise at low frequencies. The third term, the modulator output, is DAC error which is delayed only by one sample.
If DAC errors of quantizer are discarded, then:

$$Y(z) = H_X(z)X(z) + H_Q(z)E_Q(z) \quad (2)$$

For an L-order sigma-delta modulators $H_Q(z)$ and $H_X(z)$ are as follows:

$$H_Q(z) = (1 - z^{-1})^L \quad (3)$$

$$H_X(z) = z^{-L} \quad (4)$$

Thus, the quantization noise is attenuated by L zeros (L: number of integrators) in DC and the input signal is only delayed without any changes in the spectrum [2].
Dynamic range of an L-order modulator is approximated by equation (5):

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)M^{2L+1} \quad (5)$$

Sigma-delta modulator can be divided into two major categories, single-loop and multi-loop. In single-loop modulators, only one quantizer and negative feedback is used, while in the multi-loops or cascades, multiple loops are used. Each of these structures can have single-bit or multi-bit DAC [1].
A 2-order single-loop modulator is shown in Fig. 4. This structure is frequently used due to good qualities of implementation, lack of sensitivity to adjustment of coefficients and non-ideal effects of analog circuits. The modulator is composed of two integrators, a comparator and a DAC. To increase the dynamic range of modulator, it is required to increase over-sampling ratio M, or use a multi-bit DAC. Application of multi-bit DAC for high precisions is virtually impossible due to its inherent nonlinearity. Increasing M increases the sampling frequency and faster circuits are required [27].

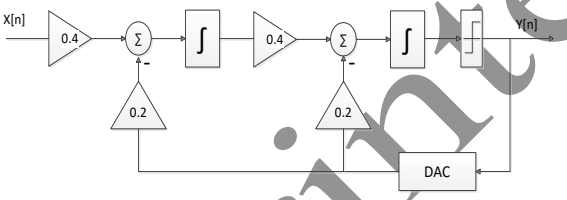

Fig. 4 Second-order sigma-delta modulators [27]

To increase the dynamic range and achieve high accuracy, the order of the modulator can be increased. Fig. 5 shows a 4-order single-loop modulator. 2-order and higher order modulators are prone to instability for input signals close to the full range of the modulator. It has been shown that a sigma-delta modulator is stable when its quantizer input does not exceed an allowable range. In higher order single-loop modulators, quantizer input increases faster by increasing input signal amplitude due to consecutive integrators. This causes overloaded quantizer and as a result the negative feedback loop is opened; therefore, the modulator becomes unstable.

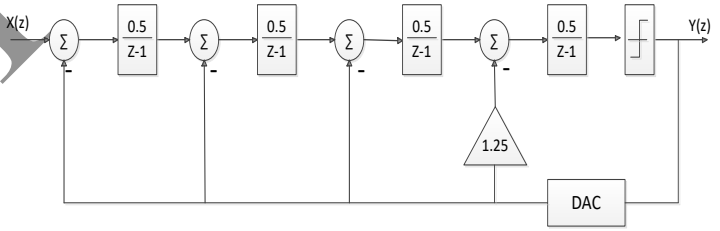

Fig. 5 4-order single-loop modulator [27]

In order to increase the order of the modulator in the MASH structures, a combination of first and second order modulators which are always stable, is used. Since the stability of this kind of modulators are guaranteed, these modulators have a dynamic range greater than single-loop modulators. In a multistage sigma-delta modulator, the quantization error of the first stage will be input to the second stage and error on the second stage will be input to the third stage and so on. The output signal of each stage of a modulator is given to a digital circuit. If the combination of digital outputs is perfect, only the effect of quantization error of last stage will appear at the output signal. Thus, only quantization error of the last stage will appear in the output of a cascade modulator. Quantization error of the last stage is moved to frequencies outside the signal band by shaping the quantization noise and eventually is filtered out .
The main advantage of MASH structure is its stability. Considering the fact that first and second order modulators which are always stable are used in each stage of a cascade modulator, these modulators have guaranteed stability comparing to second-order and higher order single-loop modulators. This will cause cascade modulators remain stable for input signals close to the feedback reference signal, resulting in a higher level of overloading therefore, greater accuracy.

2.1 PROPOSED CASCADE SIGMA-DELTA MODULATOR

Fig. 6 shows a schematic of 4-order MASH 2-1-1 $\Delta\sum$ modulator with cascade structure. The first stage is a second-order single-loop system and the second and third stages use first-order single-loop modulators [21].

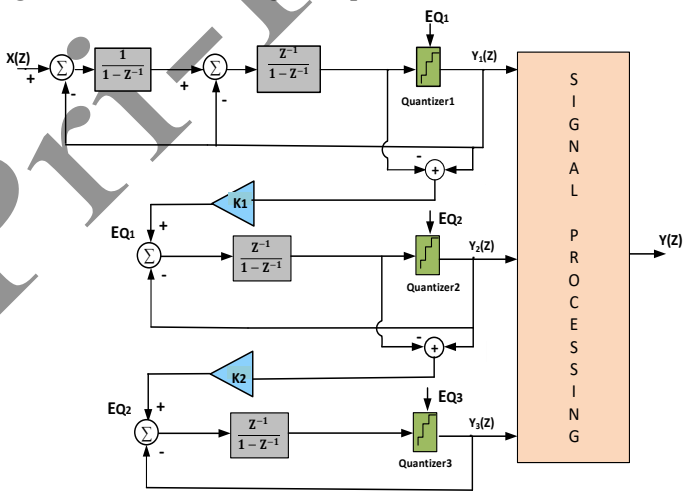

Fig.6 Schematic of MASH2-1-1 fourth-order sigma-delta modulator (proposed modulator)

For a MASH 2-1-1 sigma-delta modulator, the equation can be written as:

$$\begin{aligned} Y_1(z) &= Xz^{-2} + E_{Q1}(1-z^{-1})^2 \\ Y_2(z) &= E_{Q1}z^{-1} + E_{Q2}(1-z^{-1}) \\ Y_3(z) &= E_{Q2}z^{-1} + E_{Q3}(1-z^{-1}) \end{aligned} \quad (6)$$

To eliminate the noise error in the initial stages, digital filters are used to attenuate the quantization noise, as shown in (8).

$$Y(z) = Y_1 z^{-2} - Y_2 z^{-1}(1-z^{-1})^2 + Y_3(1-z^{-1})^3 \quad (7)$$

$$Y(z) = Xz^{-4} + E_{Q3}(1-z^{-1})^4 \quad (8)$$

2.2 SYSTEM LEVEL RESULTS

A MASH 2-1-1 $\Delta\sum$ modulator is shown in fig. 7 with all the required coefficients. There are 10 unknown variables in this figure. For high SNR and dynamic range, different combination of coefficients should be examined. In first step, 5 coefficients are calculated and in the next step, using these data the other coefficients are calculated as shown in fig. 8. These coefficients are implemented by capacitance ratio in switched capacitor implementation including a_{f1}, a_{i2}, a_{u3}, a_{u4}, a, a_{f2} , a_{f3}, a_{f4}, a_{f4}, a_{i1}, a_{i2}.

These factors are both related to each other and to the factors obtained in the system level simulation. To achieve stability and high SNR, these relations are required between factors. If four modes are assumed for each unknown in the first and second stages, the number of mappings will reduce to 512 modes.

Digital functions $H_1(z)$, $H_2(z)$, $H_3(z)$ (digital factors) in terms of the new variables are as follows:

$$H_1(z) = z^{-2}\left(1-(1-\lambda_1)(1-z^{-1})^2\right) \quad (9)$$

$$H_2(z) = z^{-1}(1-z^{-1})^2\left(1-(1-\lambda_2)(1-z^{-1})\right) \quad (10)$$

$$H_3(z) = (1-z^{-1})^3 \quad (11)$$

For capacitive switches considering V_{p-p}=3V for output swing of the delay integrators, the proper factors are shown in fig. 8.

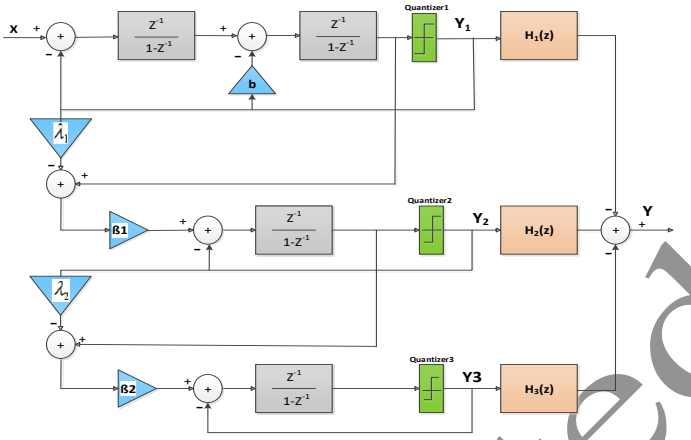

Fig. 7 Block diagram of the fourth-order cascade sigma-delta convertor (proposed modulator)

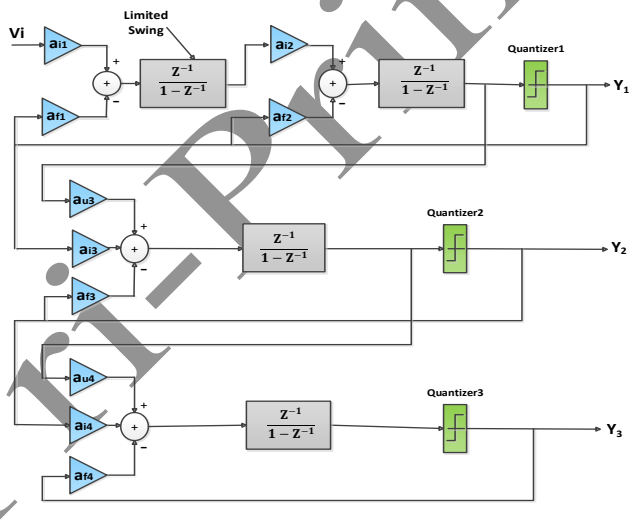

Fig. 8 Block diagram of the fourth-order cascade sigma-delta convertor with capacitive switch factors (proposed modulator)

Fig. 9 shows simulation results, in which factors $\lambda_2 = 3.5$, $b = 2$, $\beta_2 = 1.375$, $\beta_1 = 0.625$, $\lambda_1 = 4$, SNR=146dB and DR=151dB have the highest DR and high SNR for possible coefficient combinations. Fig. 9 also shows that the SNR of the desired structure is greater than the other two structures. Systemic simulation results and factor calculations are listed in the following table 1.

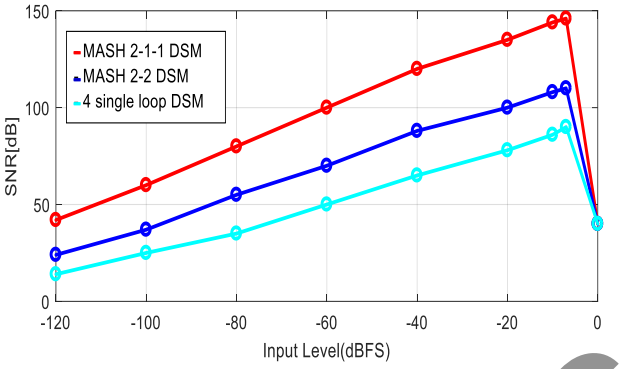

Fig. 9 SNR versus input amplitude with optimal coefficients

Table 1: List of calculated and simulated coefficients proposed 2-1-1 DSM

b=2 λ_1=4 λ_2=3.5 β_1=0.625 β_2=1.375 a_{f1} = 0.5 a_{i2} = 0.375 a_{u3} = 1.5 a_{u4} = 0.25	$a_{i1} = a_{f1}$ = 0.5 $a_{f2} = 2 \times a_{f1} \times a_{i2}$= 0.375 $a_{f3} = a_{i3} / (\lambda_1 \beta_1)$ = 0.45 $a_{i3} = \lambda_1 \times a_{i2} \times a_{f1} \times a_{u3}$ =1.125 $a_{i4} = \lambda_2 \times a_{f3} \times a_{u4}$= 0.39375 $a_{f4} = a_{i4} /(\lambda_2 \beta_2)$ = 0.0818182	SNR=146 dB DR=151 dB Resolution=24 bit Gain=10 K GBW(Hz)=10 M

3. Circuit Level Implementation

Implementation of a second-order sigma-delta modulator requires two integrators, one comparator and one digital to analog convertor. To implement the circuit shown in figure 8, we start from constituents of a differential first-order modulator; then, we convert the first-order circuit to a second-order one. Using these circuits, a fourth-order cascade delta-sigma convertor (MASH2-1-1) is implemented. Its signal-to-noise ratio is obtained by Cadence software. Three delay functions are used in cascade digital structure to eliminate quantization noise of the output.

Fig. 10 shows block diagram of a first-order sigma-delta modulator using an integrator, a comparator and a DAC. Fig. 11 shows different configuration of an integrator.

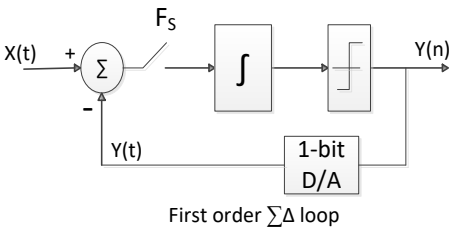

Fig. 10 Block diagram of a delta sigma modulator

Fig. (11.a) is a delayed integrator sensitive to noisy capacitors. Fig. 11.b and fig. 11.c show integrators insensitive to noisy capacitors, while fig. 11.c shows an integrator without a delay. This type of integrator is not suitable for sigma-delta convertors due to lack of delay. Gain of each integrator is shown in figure 11 without considering non-ideal effects [22].

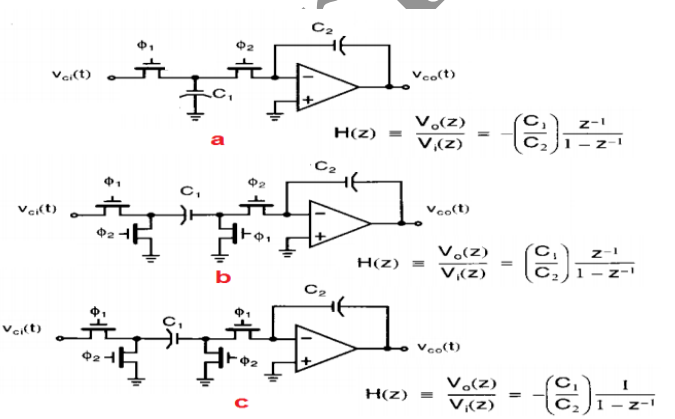

Fig. 11 Gain of different integrator configuration without considering non-ideal effects [22]

If the number of integrators increases in a circuit, it will be too hard to write the equation of the load; therefore, Mason formula can be used for convenience. In other words, domain transfer function Z of key elements are obtained first, then using Mason formula can obtain input-output relation. For this purpose, key elements are modelled in fig. 12. Using Mason's rule, transfer functions can be obtained as follows:

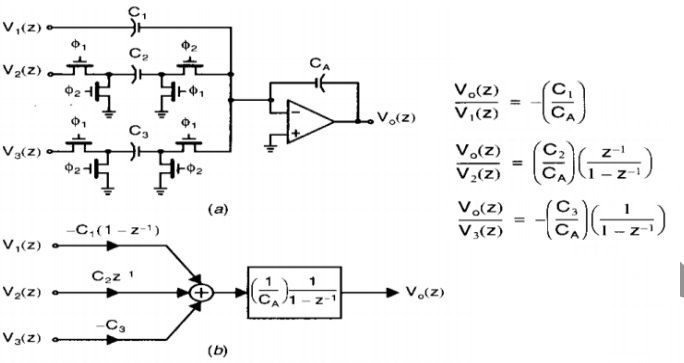

Fig. 12 Modelling of key elements of the integrator [24]

In a sigma-delta modulators, two other operations happen after integration, first quantization of the integrator output, second return or output feedback of the quantizer to the integrator input. Quantizer used in the MASH 2-1-1 fourth-order cascade modulator is either positive or negative such as a sign function. Therefore, quantizer can be made by a simple comparator. If the comparator does not have a large linear range, some part of the data will be lost. Thus, the circuit needs to react quickly to the input differences. In cascade modulators, single bit quantizer is used, because higher order quantizer non-linearity can make the whole system non-linear [2]. If the feedback loop breaks, the modulator becomes unstable. For this reason, positive feedback is mostly used in the circuits. To return the comparator output signal, a digital to analog convertor (DAC) is required. Because the output signal of the comparator has two-levels, this signal is directly added to the integrator input with opposite polarity.

A fully differential first-order modulator is shown in fig. 13. Differential structures have potential of removing common mode noise signals. In this figure, bottom plate sampling is used to remove the offset. In this method, two switches turn off later to minimize the offset [25-26].

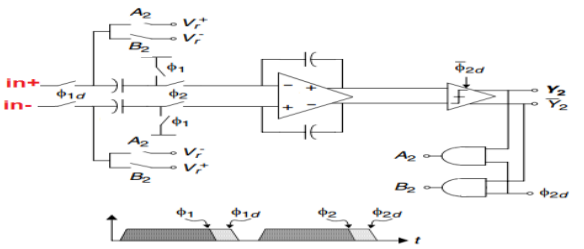

Fig. 13 Implementation of first-order differential modulator [6]

To implement a second-order sigma-delta convertor, another integrator is added to the circuits. Fig. 14 shows a second-order sigma-delta convertor composed of two integrators, a quantizer and a single-bit DAC. Using capacitor ratio, required factors can be produced. To implement the fourth-order cascade proposed modulator (MASH 2-1-1), it is enough to cascade the second-order modulator with two first-order modulators and finally remove quantizer noises by a digital filter. In this modulator, concern of instability is very low, because of feed forward paths and using modulators with high stability.

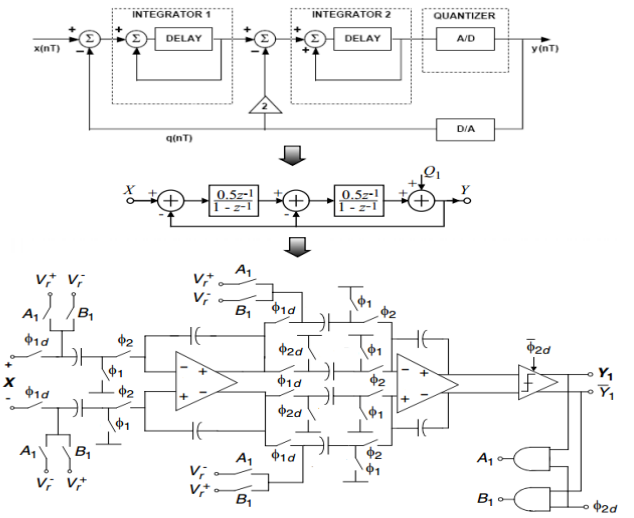

Fig. 14 Second-order delta sigma convertor [6]

The complete circuit implementation of the proposed MASH 2-1-1 modulator is shown in fig. 15. To implement digital functions, flip-flops representing digital delay are used as shown in fig. 16 [25-26].

The integrator is composed of an Opamp with several switches and capacitors. The most important task of Opamps is to create an ideally virtual ground at the integrator input. To achieve this, high gain amplifier should be used.

Obviously, Opamp gain affects quantization noise power causing reduced dynamic range. The other problem that increases noise floor is the noise in other circuit elements and switches. In general, total noise power can be calculated as follows:

$$\text{Total noise power} = \overbrace{P_Q + P_{th-switch} + P_{th-OTA} + P_{1/f-OTA}}^{\text{Circuit Noise}} + P_{\text{Distrotion}} \quad (12)$$

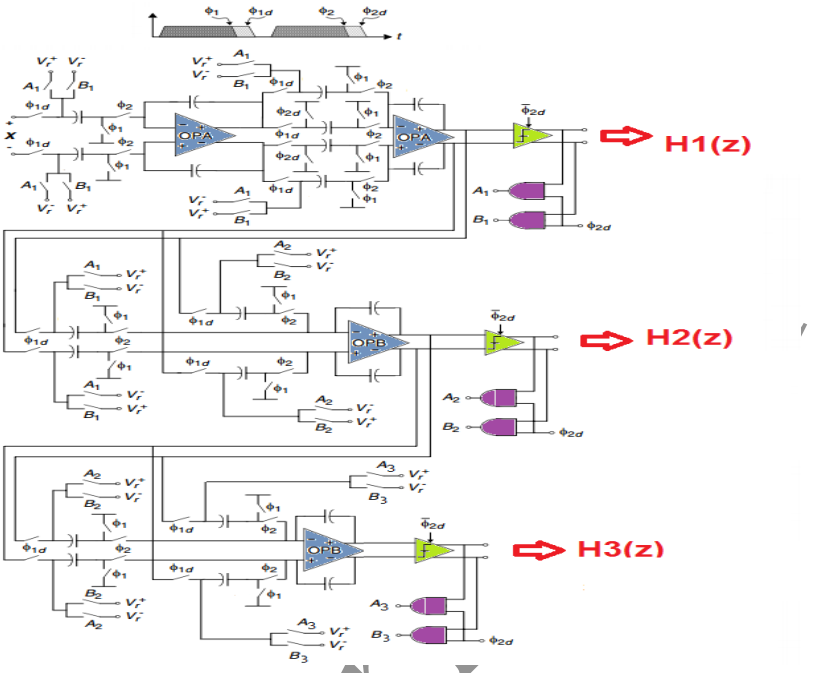

Fig. 15 Implementation of proposed MASH 2-1-1 modulator without digital functions

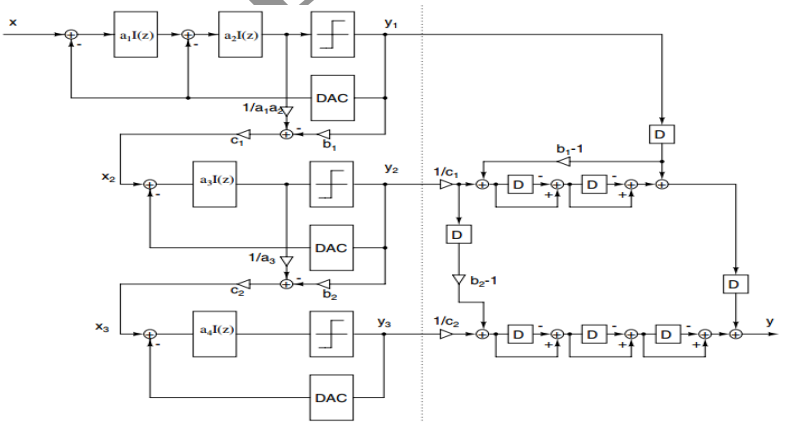

Fig. 16 Block diagram digital functions of the proposed modulator

Where the terms in (12) are quantization noise power, switch thermal noise power, OTA thermal noise power, flicker noise power and distortion power respectively.

3.1 SELECTION OF OPAMPS

Operational amplifiers are basic elements of many analog and mixed signal systems. Opamps are widely used in many applications of different complexities from generating DC bias, and filtering to amplification. The most important block of switched capacitor circuits are Opamps. The virtual ground created by an ideal Opamp is required in switched capacitor circuits to convert voltage to charge and form switched capacitor integrator. However, non-ideal Opamps are used in practical switched capacitor circuits, including limited bandwidth and limited DC gain. In these circuits, Opamp must reach its extremes in half clock period. This is why bandwidth is so important. Hence, different sources assume Opamp bandwidth from 5 to 10 times greater than clock frequency.
To satisfy the above-mentioned specifications, Opamp of fig. 17 has been used. Opamp is fully differential; therefore, a common mode feedback circuit should be used. For low power consumption, a capacitive common mode feedback was used to achieve zero DC power consumption [25].

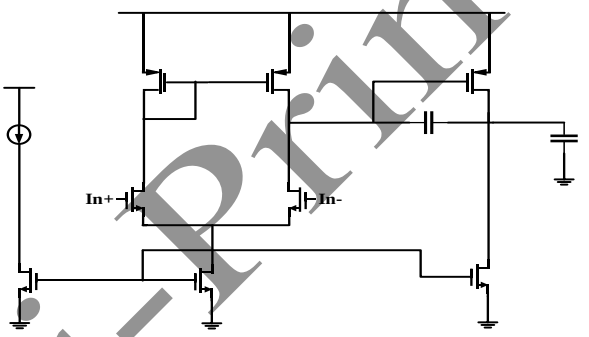

Fig. 17 Opamp configuration

An opamp have been designed and used in the circuit with the listed specifications as shown in table 2.

Table 2. Some of the specifications of the Opamp used

	DC-Gain	GBP	PM	Power	SR	Tech.
Opamp	53 dB	60 MHz	58.5	558 uW	95 V/us	180 nm

3.2 COMPARATOR

Function of a comparator is to convert an analog signal to a digital multi-level signal. To achieve linear characteristics of an ADC, it is designed in 1 level or

one bit. In fact, one (OTA or Opamp) can be a comparator provided that it does not have any negative feedback.
In this design, the comparator shown in fig. 18 has been used which has low power consumption and all other requirements of a comparator including noise, offset, gain, precision and the rate of output change. The flip-flop in comparator output maintains data in the considered time.

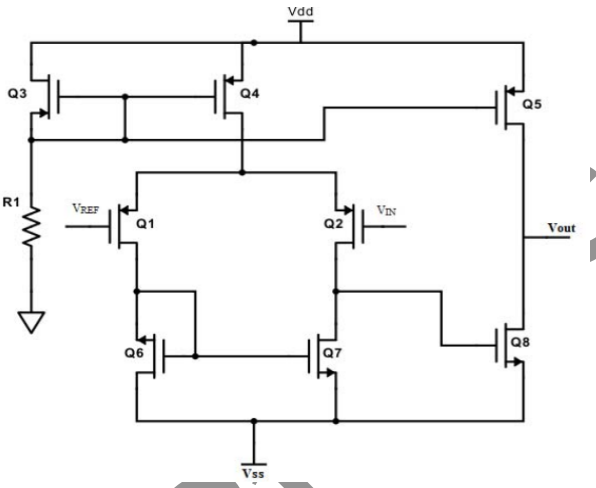

Fig. 18 The comparator

3.3 IMPLEMENTATION OF DIGITAL FILTERS

A digital filter is composed of delay units. Fig. 19 shows a D-flip-flop representing a delay. In fact, the element (Z-1) can be implemented by the circuit. To implement ($1-Z^{-1}$), the circuit shown in fig. 20 is used.

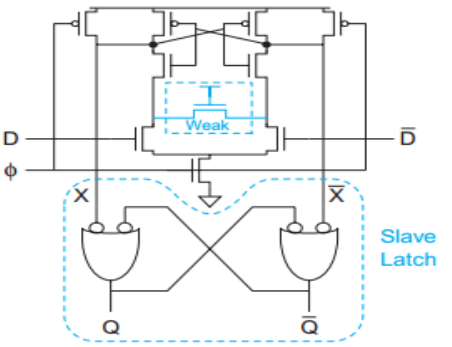

Fig.19 The D Flip-Flop

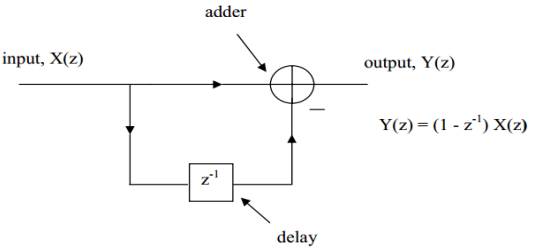

Fig. 20 Implementation of 1-Z^{-1}

The last part of discussion is about 180nm CMOS process which is used in the circuit implementation. For this purpose, all strengths and weaknesses of the process need to be recognized as well.

3.4 Circuit Design and Results

The circuit in fig. 21 shows a schematic of the modulator based on factors obtained from the systemic design [25-26].

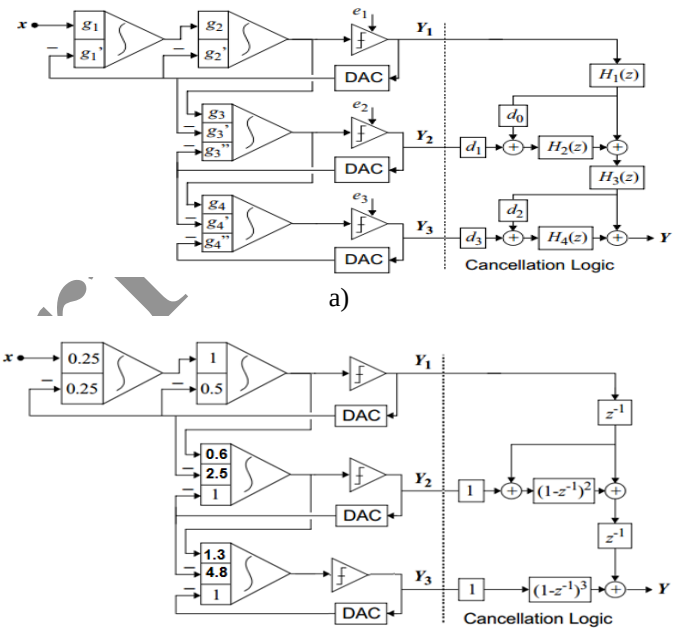

Fig. 21 Schematic modulator based on factors obtained from systemic design a) parametric, b) with coefficients.

To achieve SNR of 146 dB, factors of Table 3 are used. To calculate factors and the relationship with circuit, Table 4 is used. According to fig. 22 and Table 4, capacitors of integrators are calculated.

Table 3. factors to achieve SNR=146dB

MASH 2-1-1 ∑ΔM		
Analog	Digital	
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$	$H_1(z) = z^{-1}$
$g_4' = g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1 - z^{-1})^2$
	$d_2 = 0$	$H_3(z) = z^{-1}$
	$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$	$H_4(z) = (1 - z^{-1})^3$

Table 4. Factors and their relations with circuit

1st Integrator	2nd Integrator	3rd Integrator	4th Integrator
$g_1 = \frac{C1}{C2}$	$g_2 = \frac{C3+C4}{C5}$	$g_3 = \frac{C6+C7}{C8}$	$g_4 = \frac{C9+C10}{C11}$
$g_1' = \frac{C1}{C2}$	$g_2' = \frac{C4}{C5}$	$g_3' = \frac{C6}{C8}$	$g_4' = \frac{C9}{C11}$
-	-	$g_3'' = \frac{C7}{C8}$	$g_4'' = \frac{C10}{C11}$

To satisfy the requested characteristics, amplifiers have been designed with 68dB gain, 62° phase margin with 2pF load capacitor. Unity gain bandwidth was obtained to be 70MHz with 5pF load capacitor. Because of switching, noise and frequency response of the circuit nonlinear PSS and PAC as well as QPSS analyses were performed to obtain gain and noise. Finally, the input referenced noise was obtained at 15.4nVrms within the Opamp bandwidth.

In digital or on/off circuits, transistor aspect ratio is 10 with channel length of 180nm. Minimum capacitor of the circuit was also considered 125fF to achieve high speed, when reaching the maximum outputs of Opamp. Finally, modulator was assembled in Cadence software. The clock frequency was selected to be 200 kHz and Spectral density of output samples were calculated by MATLAB Simulink for two quantities of the minimum capacitor value.

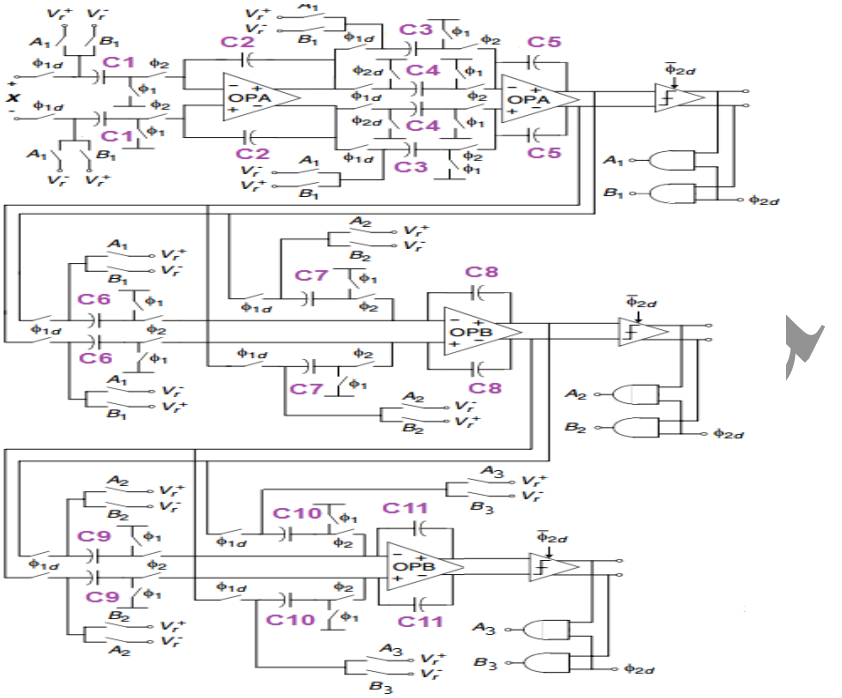

Fig. 22 Factors and their relations with circuit

Eventually, the best-simulated SNR was 133dB with 26mW of power dissipation. Fig. 23 shows spectral density of the output signal. Table 5 shows Comparison of the results from circuit simulation of proposed modulator with several state-of-the-art modulators.

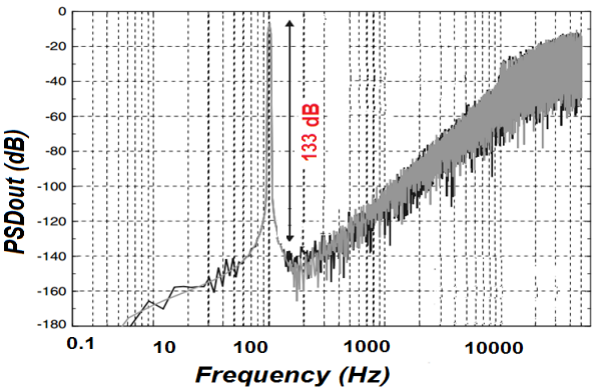

Fig. 23 Spectral density of proposed MASH 2-1-1 modulator output power

Table 5. Comparison of the results from circuit simulation of proposed modulator with several state-of-the-art modulators

Reference	[29]	[30]	This Work
Year	2016	2017	**2024**
Bandwidth(kHz)	0.3	2	**0.16**
SNR(dB)	85	100	**133**
DR(dB)	88	107	**138**
Supply(V)	1	5	**1.8**
Power (mW)	0.023	3.2	**26**
Technology (μm)	0.18	0.35	**0.18**

4. CONCLUSION

This paper presents design and simulation of a fourth order MASH 2-1-1 sigma-delta analog to digital converter. Using MATLAB simulation of the system in combination to Cadence circuit implementation provides more insight into the system design. The ability of the cascade systems to provide stable conversion has been utilized in this design for high resolution of the converter. Fourth order converters are prone to instability, but the cascade version of the fourth order is stable, because of internal stability of each unit.

More specifically, sampling capacitors are sized to achieve sufficiently low thermal noise and for a given sampling rate and settling accuracy this translates to certain bandwidth and power dissipation for the first integrator OTA. A result a 24-bit resolution has been achieved with an over sampling rate of 1024. The integrators can reach 3Vpp of the output voltage with 160Hz of the input signal bandwidth. SNR of 133 dB has been obtained which is smaller than what system simulation predicts. This is because of thermal and switching noise, lack of high gain Opamp and non-linearity of the switches. The converter consumes 26mW of power with 1.8V supply voltage and 180nm CMOS technology parameters.

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