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Performance Study and Analysis of Heterojunction Gate All Around Nanowire Tunneling Field Effect Transistor

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Abstract: In this paper, we have presented a heterojunction gate all around nanowire tunneling field effect transistor (GAA NW TFET) and have explained its characteristics in details. The proposed device has been structured using Germanium for source region and Silicon for channel and drain regions. Kane's band-to-band tunneling model has been used to account for the amount of band-to-band tunneling generation rate per unit volume of carriers which tunnel from valence band of source region to conduction band of channel. The simulations have been carried out by three dimensional Silvaco Atlas simulator. Using extensive device simulations, we compared the results of presented heterojunction structure with those of Silicon gate all around nanowire TFET. Whereas due to thinner tunneling barrier at the source-channel junction which leads to the increase of carrier tunneling rate, the heterojunction gate all around nanowire TFET shows excellent characteristics with high on-state current, superior transconductance and high cut-off frequency.

Keywords: Heterojunction GAA NW TFET, Silicon GAA NW TFET, On-State, Off-State, Cut-Off Frequency

1. INTRODUCTION

Scaling limitations of traditional planar bulk CMOS technologies, such as short-channel effects or leakage currents, require the introduction of novel device concepts which used different mechanisms or non-planar structures [1-9]. Nanowire-based transistors are promising candidates for gate length scaling in nanometer due to the improved electrostatic control of the channel as compared to planar devices [10]. The cylindrical gate all around geometry also allows for a thicker body and gate oxide as compared to planar gate geometry [11-12]. However, nanowire transistors suffer from a thermal limit of 60mV/dec on the subthreshold swing (SS) and need a high supply voltage for achieving

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SS<60mV/dec [13]. So, in recent years, there has been an increasing desire to explore novel devices that can provide low subthreshold swing at low V_{DD}, while maintaining a low off current. Thus, with the goal of replacing the GAA nanowire transistors by devices based on a new carrier injection mechanism different from diffusion over a potential barrier, the tunneling field effect transistors (TFETs) have been proposed [14-15]. As such devices utilize tunneling injection of carriers through a tunneling barrier rather than thermionic injection over a barrier, and the barrier width can be controlled by the gate voltage, they have good immunity to short channel effect, drain induced barrier lowering, and superior electrostatic control (lower OFF current and steeper subthreshold swing) which enable transistor operation at low voltages [16-17].

In TFET, the carriers can be transported from source to channel by the band-to-band tunneling (BTBT) mechanism. The carrier injection on the BTBT of electrons from a degenerate p^+ source into the channel conduction band causes high-energy carriers which are filtered out by the semiconductor band gap that yields lower on-state current. Various techniques have also been reported for improving the on-state current of TFET such as use of semiconductors with lower band gap and high carrier mobility, gate dielectric scaling, source and drain doping engineering [18-21].Germanium material has a small effective band gap, low-temperature process, relatively low cost, high symmetry, and easy integration on Silicon platform [18]. The use of Germanium material promises the improvement of speed performance of devices.

In this paper, we present a gate all around heterojunction nanowire tunneling FET (GAA NW TFET) structure and compare with Silicon nanowire Tunneling FET. Then, the simulation results are analyzed which exhibit enhanced gate-controlled band- to- band tunneling current and high frequency parameters due to using Germanium as source material in the proposed structure.

2. DEVICE STRUCTURE AND SIMULATION METHOD

Fig. 1 shows the gate all around nanowire tunneling field effect transistor (GAA NW TFET). The parameters used for devices modeled in this work, are summarized in Table I.

All simulations are carried out by 3D Silvaco Atlas simulator [22]. High doping concentrations band gap narrowing (BGN) [23] and Auger recombination [24] models are included in the simulations. Because of the presence of high impurity atom and also consideration of an interface trap (or defect) effect, Shockley-Read-Hall (SRH) [25-26] model is also included. In the simulations, the concentration dependent mobility model for low field mobility related to doping density and the field-dependent mobility model for high field velocity saturation depending on the parallel electric field in the direction of current flow are also considered.

Table I: Parameters used for devices modeled in this work.

	Heterojunction GAA NW TFET	Silicon GAA NW TFET
Source/channel/drain	20nm/20nm/20nm	20nm/20nm/20nm
Source material/doping	Germanium/1×10^{20} cm^{-3}	Silicon/1×10^{20} cm^{-3}(p-
Channel	Silicon/1×10^{16} cm^{-3}(n-	Silicon/1×10^{16} cm^{-3}(n-
Drain material/doping	Silicon/1×10^{19} cm^{-3}(n-	Silicon/1×10^{19} cm^{-3}(n-
Oxide thickness	1nm	1nm
Body diameter	10nm	10nm

Also, we use Kane's band-to-band tunneling model to account for the amount of band-to-band tunneling generation rate per unit volume of carriers which tunnel from valence band of source region to conduction band of channel. The Kane model assumes that the electric field is constant over the tunneling length [27-29].

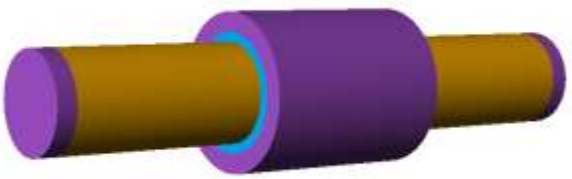
The drive current of structures is calculated using Kane's model which states about the generation rate of the carriers on the volume (*v)* of the device structure [30]

$$I_D = q\int G_{BTB}dv \tag{1}$$

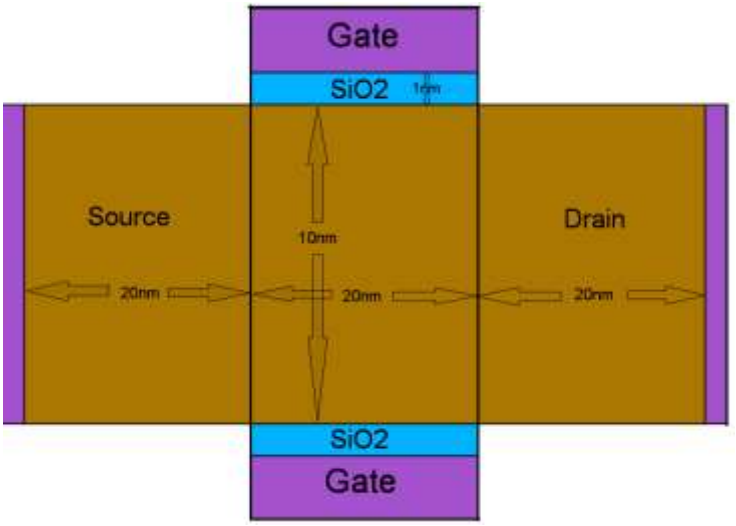
G_{BTB} which represents the generation rate of the carriers, can be obtained by Kane's model [28-30]

$$G_{BTB}(E) = A_k E^{D_k} \exp\left[-\frac{B_k}{E}\right] \tag{2}$$

E is the magnitude of electric field and Kane's default parameters $A_k=4\times10^{14}$ $cm^{-1}s^{-1}V^{-2}$ and $B_k=19\times10^6$ Vcm^{-1} are adopted for Silicon. In heterojunction GAA NW TFET, the Kane's parameters are $A_k=9.1\times10^{16}cm^{-1}$ s^{-1} V^{-2} and $B_k=4.9\times10^6$ Vcm^{-1} for Germanium material which rely on the electron effective mass at conduction and valance bands [18]. D_k is an adjustable parameter taken as 2.5 because of indirect tunneling [31].



(a)

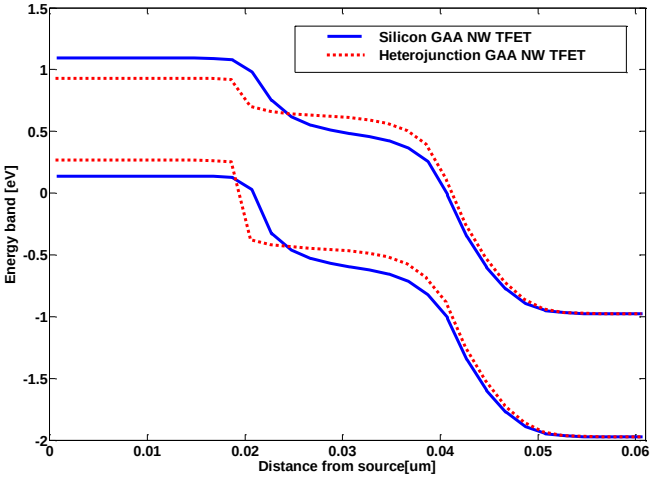


(b)

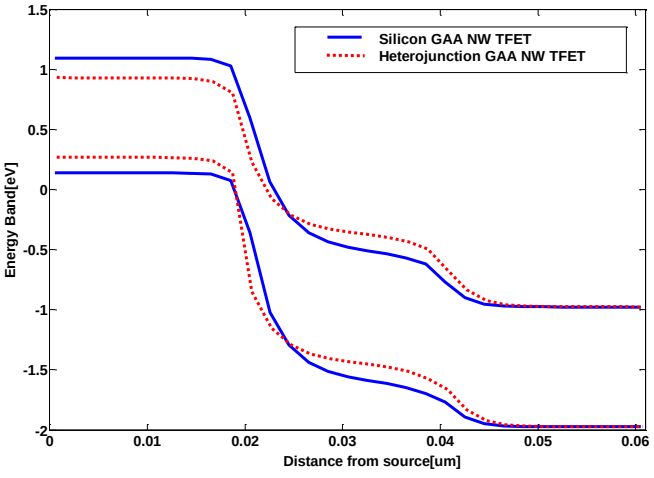
Fig. 1. The structures investigated in this paper (a) schematic view (b) cross sectional view.

3. RESULTS AND DISCUSSION

Fig. 2 shows the energy band diagrams for the heterojunction GAA NW TFET and Silicon GAA TFET structures in the off-state (V_{DS} = 1 V, V_{GS} = 0 V) and the on-state condition (V_{DS} = 1 V, V_{GS}= 1 V) along the positions located close to the channel-gate oxide interface. In the off-state, channel is depleted. For this reason, a low off-state current is obtained. When the gate voltage increases, the devices enter into flat band region. If the voltage increase continues to threshold voltage, the devices begin to conduct and then enter into accumulation region resulting in a high on-state current.



(a)

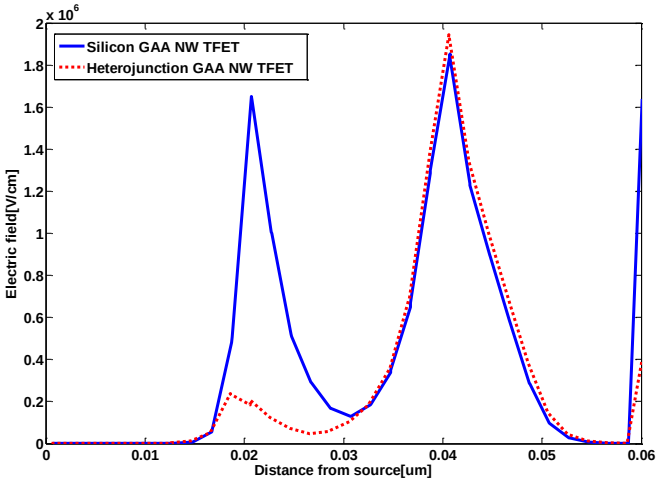


(b)

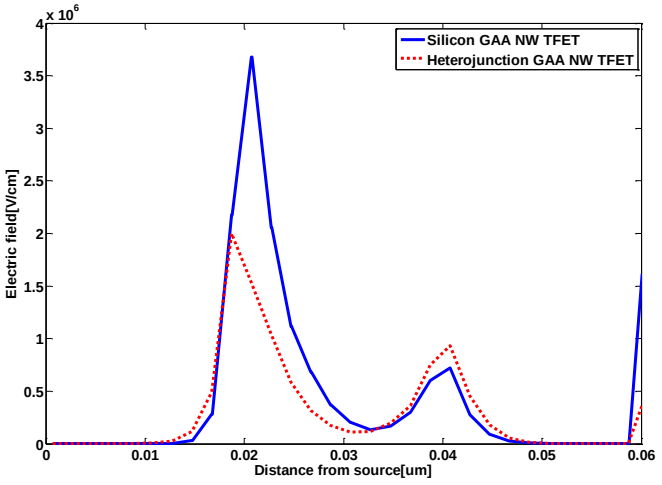
Fig. 2. (a) off-state (V_{DS}=1V, V_{GS}=0V) and (b) on-state (V_{DS}=1V, V_{GS}=1V) energy band diagrams of heterojunction and Silicon GAA NW TFETs.

Also, in off-state, the tunneling barrier width between source and channel junction in the case of Silicon GAA NW TFET is large enough to give small current (I_{OFF}) and the probability of band-to-band tunneling of electrons is negligible. However, in the heterojunction GAA NW TFET, as shown in Fig. 2, the tunneling barrier between source and channel decreases because of using Ge as source material.

As the gate voltage becomes increasingly positive from the off-state, the barrier width reduces and the electrons in the valence band of source region have a chance to penetrate the depletion region then enter the conduction band of the channel region. The electrons tunnel from the valence band of the source side to the conduction band of the channel side when the barrier width is sufficiently reduced.



(a)



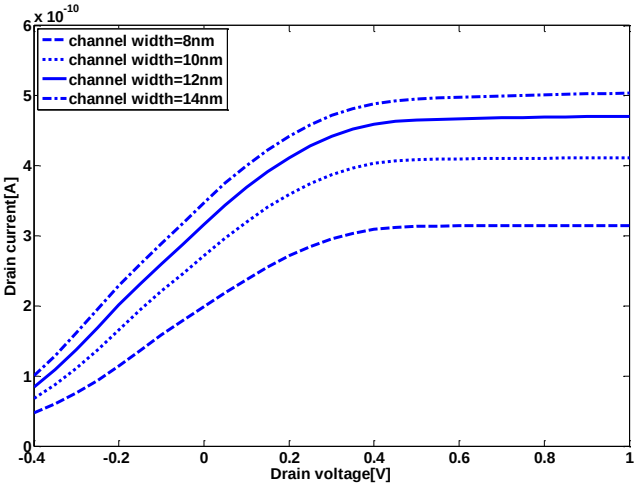
(b)

Fig. 3. (a) off-state (V_{DS}=1V, V_{GS}=0V) and (b) on-state (V_{DS}=1V, V_{GS}=1V) electric field profiles of heterojunction and Silicon GAA NW TFETs.

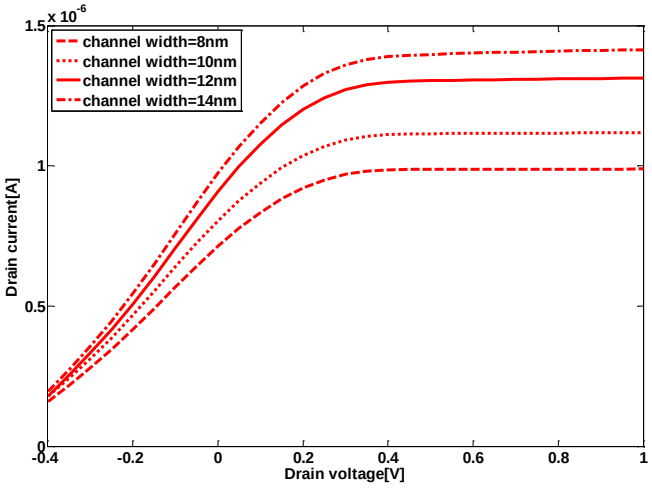
In Fig. 2, it can be seen that the heterojunction GAA NW TFET forms the narrower tunneling barrier at the source-channel interface which yields high on-state tunneling current. The off-state and on-state of the electric field profiles of the heterojunction GAA NW TFET and Silicon GAA NW TFET are shown in Fig. 3. In both on-state and off-state, two electric field peaks have been created at the source-channel and drain-channel junctions for both structures. The heterojunction device has lower values of lateral electric field because of smaller tunneling barrier which leads to the increase of carrier tunneling.

As Shown in Fig. 3(b), the presence of gate-to-source voltage has created one strong electric filed peak at the source-channel junction which implicates the tunneling probability goes up in that region. The heterojunction structure creates thinner tunneling barrier at the source-channel junction because of using Germanium as source material.

Fig. 4(a) and (b) represent the drain current as a function of drain voltage for Silicon and heterojunction GAA NW TFETs, respectively, when V_{GS}=1V and channel width varies from 8 to 14 nm. It can be seen that drain current in the heterojunction GAA NW TFET is larger than the drain current for the other structure. Also, Fig.4 shows increase of drain current with increase in channel width. So, we can conclude the channel conductance efficiency is enhanced with channel width increment.



(a)



(b)

Fig. 4. Drain current versus drain voltage of (a) heterojunction and (b) Silicon GAA NW TFETs at V_{GS}=1V.

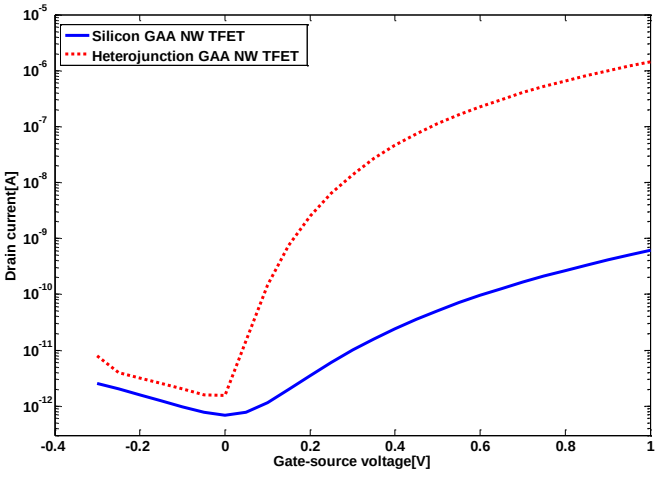


Fig. 5. Drain current versus gate-source voltage of heterojunction and Silicon GAA NW TFETs at V_{DS}=1V.

The I_{DS}-V_{GS} characteristics of structures at V_{DS}=1V are shown in Fig. 5. As compared to the Silicon GAA NW TFET, in the heterojunction GAA NW TFET, the on-state current and subthreshod swing are significantly improved. For fair comparison, the work function of the gate metal for all cases was adjusted to start the tunneling mechanism close to V_{GS}=0. The workfunction of

the gate metal for heterojunction device is 4.8eV and for the other structure is 4.65eV. Electrical characteristics of heterojunction and Silicon GAA NW TFETs are summarized in Tables II. Both on-state and off-state currents of structures are given in Tables II.

Table II: Comparison of heterojunction and Silicon GAA NW TFETs.

	heterojunction GAA NW TFET	Silicon GAA NW TFET
Off-state current [A]	1.6×10^{-12}	1.0×10^{-12}
On-state current [A]	1.43×10^{-6}	7.0×10^{-10}
I_{ON}/I_{OFF}	8.93×10^{5}	7.0×10^{2}
Subthreshold swing [V/dec]	0.025	0.08

The off-state current (I_{OFF}) is determined as the drain-to-source current at V_{GS}=0 V and V_{DS} =1 V, as well as the on-state current (I_{ON}) which is determined as the drain-to-source current at V_{GS}=V_{DS} =1V. It appears that heterojunction GAA NW TFET provides larger on-state current and higher I_{ON}/I_{OFF} ratio. Furthermore, it is clear from the Fig. 5, the heterojunction device gives the improved average subthreshold swing due to the higher slope of drain-to-source current.

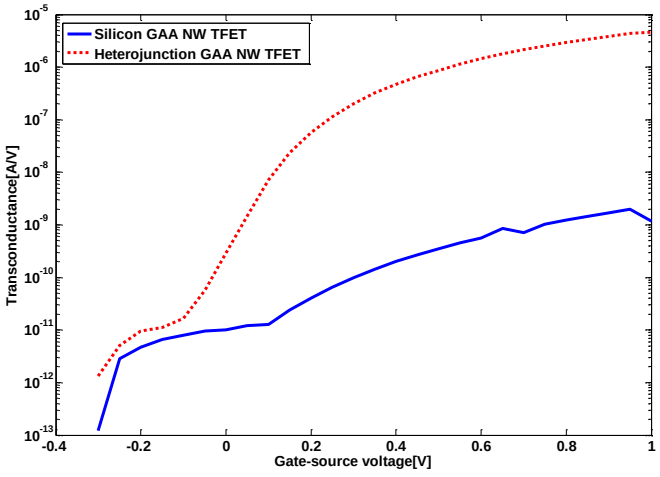


Fig. 6. Transconductance of heterojunction and Silicon GAA NW TFETs at V_{DS}=1V.

The effect of gate voltage variation on transconductance (g_m) is shown in Fig. 6. The value of transconductance is calculated using $\partial I_{DS}/\partial V_{GS}$. The g_m is an important analog performance parameter, which is a measure of the amplification given by device. The higher g_m means more efficient amplification and more suitability for analog applications. Fig. 6 indicates that

the transconductance of heterojunction GAA NW TFET is enhanced at high gate-source voltage, compared with that of Silicon GAA NW TFET. This enhancement in transconductance of heterojunction structure is due to current conduction occurring by carrier tunneling between source and channel junction.
The total gate capacitance is an important parameter for the high frequency performance analysis. The total gate capacitance is extracted from small signal AC device simulation at an operating frequency of 1 MHz. The total gate capacitance consists of gate to channel capacitance plus gate to source/drain capacitance. The variation of total gate capacitance (C_{GG}) versus gate-source voltage is plotted in Fig. 7. It is observed that the value of gate capacitance for the heterojunction GAA NW TFET is higher than that of the silicon GAA NW TFET for all values of gate-source voltages. In the heterojunction GAA NW TFET, because of lower energy band gap at source side, more carriers can tunnel from the source valence band to the conduction band of the channel. Therefore, the population of carriers and consequently the gate capacitance for heterojunction GAA TFET is larger than that of Silicon GAA NW TFET.
In Fig. 8, we can see the cut-off frequency which is calculated from $f_T = g_m/2\pi C_{gg}$, where g_m and C_{GG} are the transconductance and the total gate capacitance, respectively. The cut-off frequency f_T in heterojunction device is higher than that in silicon GAA NW TFET because of much higher transconductance in heterojunction device.

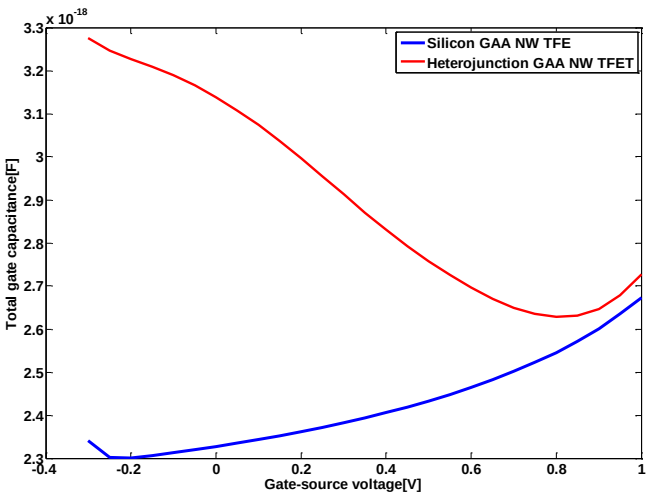


Fig. 7. Total gate capacitance of heterojunction and Silicon GAA NW TFETs at V_{DS}=1V.

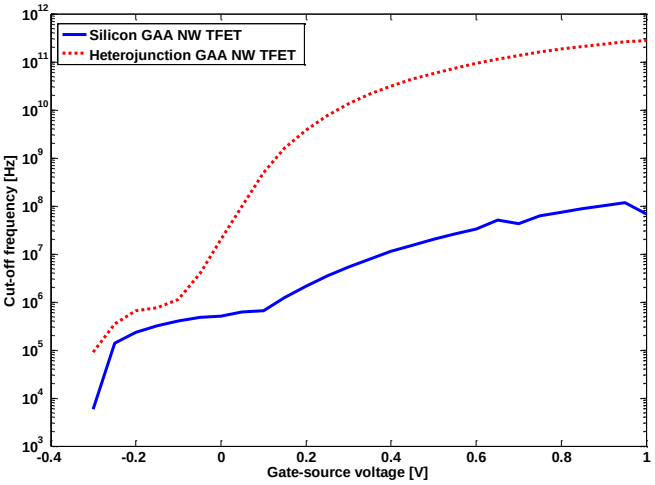


Fig. 8. Cut-off frequency of heterojunction and Silicon GAA NW TFETs at V_{DS}=1V.

4. CONCLUSION

In this paper, a heterojunction gate all around nanowire tunneling field effect transistor has been presented and its physical operations have been explained in details. We have shown that within the scope of Kane's model, the heterojuncton GAA NW TFET structure can achieve high on-state current and an improved subthreshold swing as compared with the Silicon GAA NW TFET structure. The gate capacitance of heterojunction GAA TFET is larger than that of Silicon GAA NW TFET. This happens because of the population of carriers in comparison with Silicon GAA TFET. Despite the large capacitance, due to the much higher transconductance, the cut-off frequency (f_T) in heterojunction device is higher than that of silicon GAA NW TFET.

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