Research Paper

Performance Optimization of an Electrostatically Doped Staggered Type Heterojunction Tunnel Field Effect Transistor with High Switching Speed and Improved Tunneling Rate

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Abstract

In this paper, we demonstrate an electrostatically doped junctionless tunnel field effect transistor which is composed of a staggered band alignment at the heterojunction. The proposed structure reduces the tunneling barrier width to have a higher on-sate current using Ge/GaAs heterojunction at the source-channel interface. Due to the employment of electrostatically doped strategy for creating p^+-n^+ tunneling junction, the introduced device has low temperature simple fabrication process. The device has on-state current of 1.5×10^{-4} (A/μm), subthreshold swing of 5.15 mV/dec and on/off current ratio of 1.56×10^{10}, manifesting the design of a fast switching device. In addition, statistical analysis is conducted to investigate the sensitivity of device performance with respect to the variation of critical design parameters. The results demonstrate that gate workfunction and polarity gate bias are fundamental design parameters and optimum value should be determined for them to assess efficient device performance.

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1. INTRODUCTION

Nowadays, technology of electronic is extensively developed with the aim of designing high speed devices and breaking the speed limit of emerging electronic systems. Electronic devices and integrated circuits are continuously progressing to become more efficient, reliable, cost effective and highly integrated in the chip, are due to the down scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) dimensions. However, continuous device scaling down to nanoscale regime degrades the device performance due to the short channel effects [1-5]. Basically, among these effects, the increase in subthreshold swing, SS, and degradation of threshold voltage are two fundamental factors that may deteriorate the device performance. In principle, due to the drift-diffusion current mechanism and the Boltzmann limit, the lowest value of subthreshold swing, at 300K is predicted to be equal to ≈ 60 mV/dec. However, this value cannot meet the demands of rapid growth of electronic devices with high switching speed. Tunnel-Field-Effect Transistor (TFET) is presented as a reliable replacement for the conventional MOSFET, that provides subthreshold swing lower than the Boltzmann limit [6-8]. Basically, the common TFET device is a gated p-i-n diode with reverse bias in which carriers move from the source region into the channel via band to band tunneling mechanism. The gate voltage modulates the width of the space charge region at the interface of the source and channel regions. The critical challenges of the conventional TFET are the complex fabrication process of the device as well as low drive current. In order to amplify the drain current, different techniques including employment of multi-gate structures, source and channel material engineering and channel doping engineering are introduced. Basically, in multi-gate TFETs better gate control over the channel conductance is achieved and as a consequence, the electric field at the tunneling area is amplified [9-11]. In this situation, the increment of tunneling probability is expected. In addition, the energy band alignment at the source-channel interface is a fundamental factor, which affects the tunneling probability. Material engineering or in particular bandgap Engineering at the tunneling junction is an efficient method for performance improvement of the TFET [12-15]. In principle, type II heterojunction that is designed by III-V materials, in which the channel conduction band is located above the source valence band (in the off-state), can facilitated band to band tunneling in a narrow tunneling window as it requires a lower gate bias to align the energy levels (in the on-state) [16-19]. However, the main challenge of complex fabrication process for the conventional TFET has not yet been solved. Moreover, the main drawback of III-V materials is their

poor solubility for dopants and as a consequence, heavily doped source region can hardly be achieved.

In this paper, a new type of TFET is demonstrated, that greatly benefits from electrostatic doping rather than physical doping to form the consecutive p+-n+ tunneling junction. This approach requires low temperature fabrication process and can be utilized for designing devices in nanoscale regime. The source region is germanium (Ge) and the channel as well as the drain regions are GaAs, forming a type II heterojunction band alignment at the source-channel interface. Basically, the staggered type heterojunction implementation is suitable for applications that requires high switching speed and low consumption of power. The doping profile for the source, drain and channel regions are the same and there are no p-n junctions, so they are less costly to be fabricated. The electrical characteristics of the proposed staggered type electrically doped junctionless TFET is comprehensively studied and the impact of main physical and geometrical design parameters on the device electrical characteristics is evaluated. Moreover, statistical analysis is conducted to investigate the variation of the proposed device electrical performance with respect to the change of critical design parameters. The statistical calculation is conducted via computing Coefficient of Variation (CV) for each electrical measure [20]. Basically, CV is defined as the ratio of standard deviation over mean value (in percentile) and it shows the extent of variability of a parameter in relation to the mean of the dataset.

The paper is outlined as follows: next, device structure and important simulation models are outlined. In the following impact of essential design parameters on the feasibility of the device is comprehensively assessed. Finally, the paper is outlined in the conclusion.

2. STRUCTURE OF THE DEVICE AND SIMULATION MODELS

The schematic of the electrostatically doped heterojunction tunnel field effect transistor (EDHTFET) is illustrated in Fig.1 (both in equilibrium and electrically doped source region). The device has the same doping for all regions and no doping concentration gradient exists. The proposed device has two separated metal gates with similar workfunction but different polarities on the top of channel and source regions. The gate over the channel is known as the control gate (V_{CG}) and it controls the carrier flow in the channel. However, the gate over the source region, better known as the polarity gate is responsible for electrostatically doping of the source region. Basically, by employing negative gate voltage to the polarity gate, the source n^+ region is electrically and without

any additional physical doping is converted to a hole accumulated area. In principle, it is certified that electrical doping is nothing but to transition of the Fermi level in the direction of either valence band or to the conduction band by applying appropriate bias to the polarity gate. In the off-state, the workfunction variation between cannel and the gate material depletes the channel from mobile holes and their path in the channel becomes blocked. However, the polarity gate with negative polarity creates a hole accumulated source region. It is evident that in this case, the tunneling barrier is not thin enough to allow band to band tunneling. When the control gate voltage becomes greater than an adequate positive value, electron accumulation takes place in the channel and as a consequence, band to band tunneling current starts to flow from source to channel.

The initial device parameters are presented in Table.1. The simulation design parameters are extracted from experimentally designed heterojunction TFET structures [21-22]. The simulations are carried out via Silvaco [23] and following models are considered for simulation of the device:

(a) Band to band tunneling model, which considers nonlocal band to band tunneling as the principal current mechanism of the device. This quantum phenome happens when at sufficient control gate voltage, the conduction band of the channel region lines up with the valence band of the hole accumulated source.

(b) Bandgap narrowing model, which considers reduction of the bandgap energy in heavily doped semiconductors.

(c) Mobility models which examines the effect of doping concentration besides vertical and horizontal electric field on the mobility of carriers. The carrier mobility in the device can be influenced by the presence of charged impurities. Basically, impurity scattering is attributable to the crystal defects such as ionized impurities. In addition, the vertical and horizontal electric field can effectively modify the mobility of carriers.

(d) Quantum confinement models, which considers transition of the energy states as well as reduction of energy states in the conduction band due to the channel thickness scaling.

(e) Trap-assisted tunneling. This model considers the possibility of indirect tunneling through

the trap levels. In principle, the trap-assisted tunneling current cannot be controlled by the control gate and it can deteriorate the switching characteristics of the device.
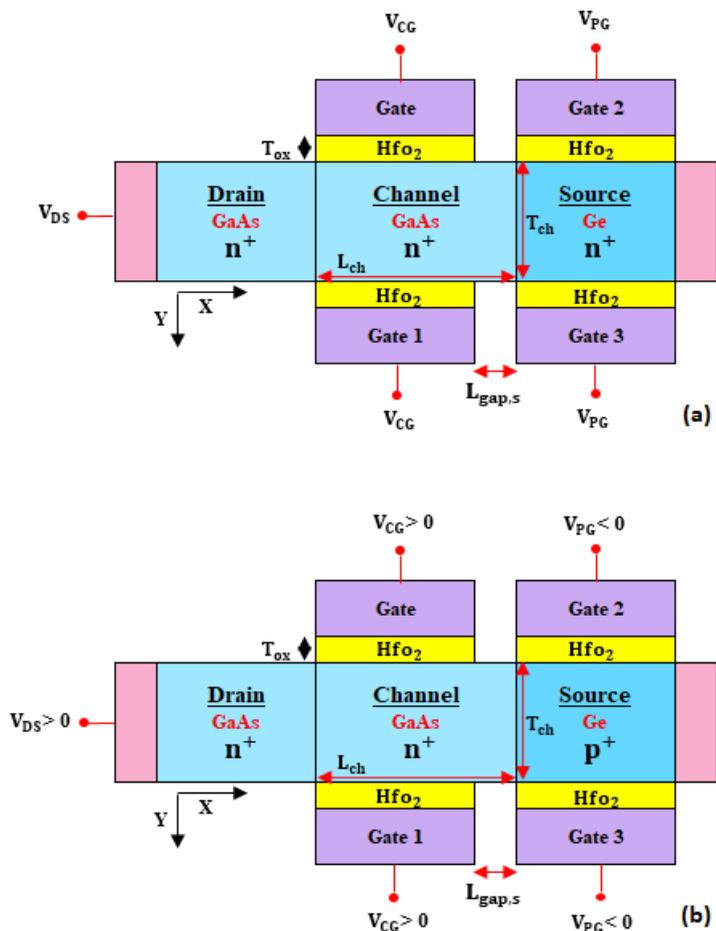
Fig. 1. Schematic of the EDHTFET (a) device structure in equilibrium, (b) device structure with electrically doped source region.

TABLE I
INITIAL DESIGN PARAMETERS OF EDHTFET

| Design Parameters	Initial Values
Source Material	Ge
Channel and Drain Materials	GaAs
Gate Insulator Material	Hfo_2
Gate Insulator Thickness T_{ox}/nm	2
Channel Length L_{ch}/nm	25
Channel Thickness (T_{ch}/nm)	5
Source, Drain and Channel Doping Density $(cm)^{-3}$	1e19
Spacer Length (L_{gaps}/nm)	5
Control Gate Bias (V_{CG}/V)	+1
Polarity Gate Bias (V_{PG}/V)	-1
Drain Bias (V)	+1
Gate Workfunction (eV)	4.15
Temperature (k)	300

3. RESULTS AND DISCUSSIONS

The energy band profile of the proposed EDHTFET is depicted in Fig.2, both in the off and on-state. Basically, the EDHTFET operates by controlling the tunneling rate between the source and the channel regions via the control and polarity gate electrodes. In the off-state (V_{CG}=0V, V_{DS}=1V, V_{PG}=-1 V), the potential barrier width between maximum of the source valence band and minimum of the channel conduction band is not thin enough to create tunneling energy window. In this situation, no band to band tunneling can take place and only the reverse leakage current of p-i-n structure caused by the minority carriers flow. However, in the on-state (V_{CG}=1V, V_{DS}=1V, V_{PG}=-1V), as the control gate bias increases towards high enough positive values, the potential barrier width between source and channel becomes narrow enough to permit a considerable tunneling current. In this context, the channel energy bands are pulled down by the gate voltage until the channel conduction band is aligned

with the source valence band to allow direct tunneling carrier transition. The results demonstrate that the energy band profile of junctions have type-II heterojunction features, which may be suitable for providing a low resistance tunneling barrier.
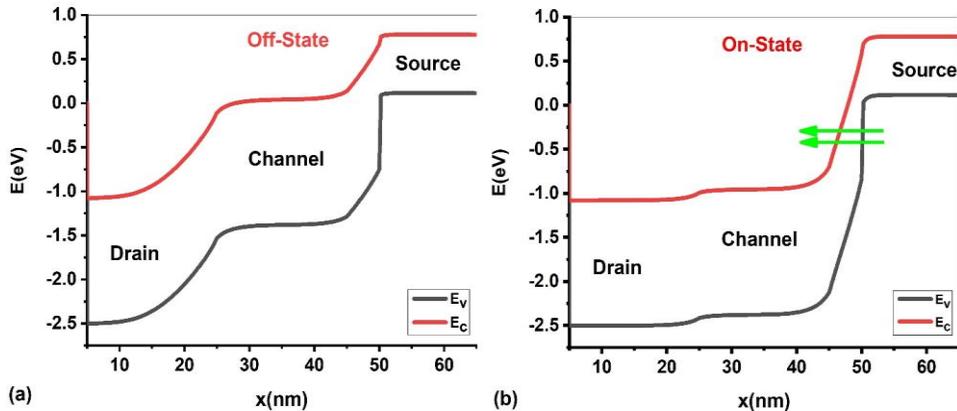
Fig. 2. Energy band profile of EDHTFET in the off and on-state from source to drain.

The corresponding electron and hole density of EDHTFET is depicted in Fig.3 both in the off and on-state along the current transport direction. Basically, an abrupt p^+-n^+ doping density at the tunneling area is critical. To reduce the electrostatic potential barrier width, the intrinsic channel region should be electrically converted to a heavily doped region. In the off-state, the electron density in the channel is not high enough to minimize the barrier width at the source-channel junction. The negative bias of the polarity gate electrically converted the n^+ source region to a p^+ region. However, in the on-state, the electron concentration of the channel rises and therefore causes the energy of sub bands for the holes and electrons to be aligned.
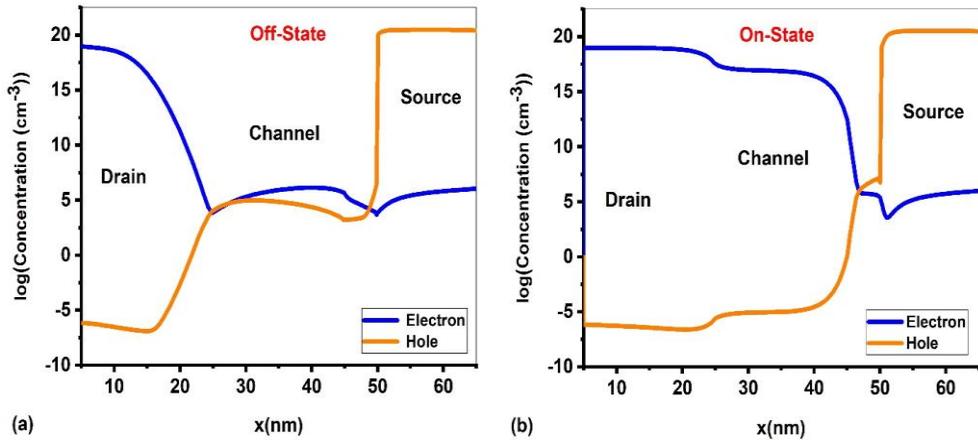
Fig. 3. Electron and hole density in the off and on-state along carrier transport direction.

Figure.4 shows the I_D-V_{CG} curves of EDHTFET as the drain bias is varied. It is clearly demonstrated that a step like characteristic is achieved in the drain current of EDHTFET. The threshold voltage of the device is computed as the adequate gate voltage for the bands overlap or in other words the amount of voltage the device needs to transit form low off-state drain current to high conductance. In principle, for an adequate positive gate bias, a significant amount of energy states is aligned to contribute for band to band tunneling and as a consequence, a steep switching behavior can be achieved. The results demonstrate that the off-state current of the device is less responsive to the drain bias change. This effect is mainly attributed to two phenomena: first, the workfunction variation between the gate and the corresponding channel, which depletes the channel for electrons in the off-state and next, the employment of a wide band gap material in the drain and channel which damps the electric field resulting from the drain bias at the tunneling junction. These features of enhancing the off-state tunneling barrier distance by reducing the channel electron density besides employing a wide band gap material at the drain region, degrades drain induced source tunneling effect. This effect makes the performance of extremely scaled EDHTFET improve. However, the on-state current of the device increases as the drain bias enhances. It is evident that the carrier velocity increases for higher drain voltages. The main electrical characteristics of the device for $V_{DS}=1V$ are summarized in Table.2. the device shows a steep subthreshold swing of 5.15 mV/dec, making the EDHTFET architecture an attractive device to implement high speed digital logic circuits.

TABLE I I
MAIN ELECTRICAL MEASURES OF **EDHTFET** FOR V$_{DS}$=1V.

Parameter	Value
I_{on} (A/µm)	1.5×10^{-4}
I_{off} (A/µm)	9.59×10^{-15}
I_{on}/I_{off}	$1.56 \times 10^{+10}$
V_{th} (V)	0.02
SS (mV/dec)	5.15
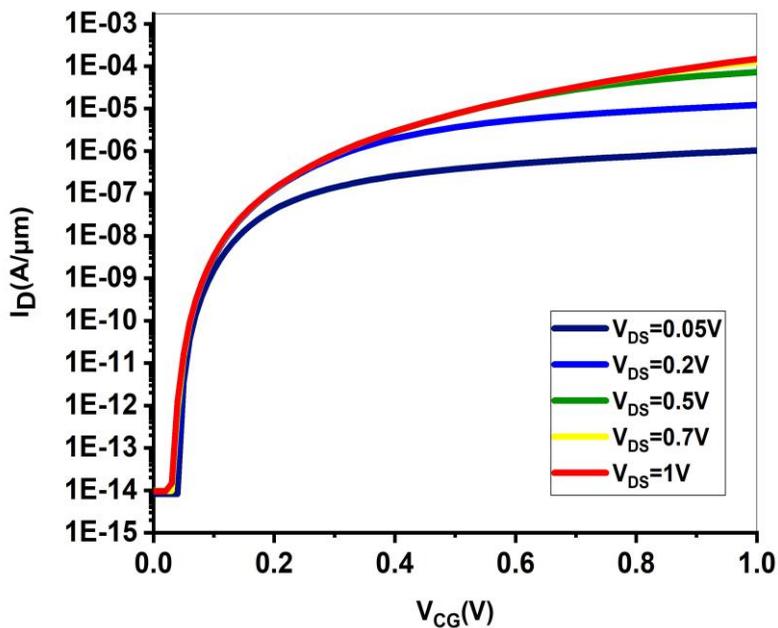
**Fig. 4.** The transfer characteristics of EDHTFET as the drain bias is parametrized.

The transfer characteristics of EDHTFET are compared with the device with the homojunction electrically dope TFET with Silicon as the source, drain and channel materials, depicted in Fig. 5. The gate workfunction of the homojunction device is calibrated to achieve same off-state current with the EDHTFET device. The results show that the on/off current ratio of 1.56×10^{10} and 9.66×10^{6} and subthreshold swing of 5.15 mV/dec and 42 mV/dec are obtained for EDHTFET and conventional lateral TFET, respectively. Due to the creation of staggered type band alignment at the interface of source and channel as well as smaller carrier effective mass of germanium that improves the tunneling probability, a higher on-state drive current (about 1000 times) with improved switching speed has been achieved for EDHTFET in comparison with the homojunction electrically doped TFET.
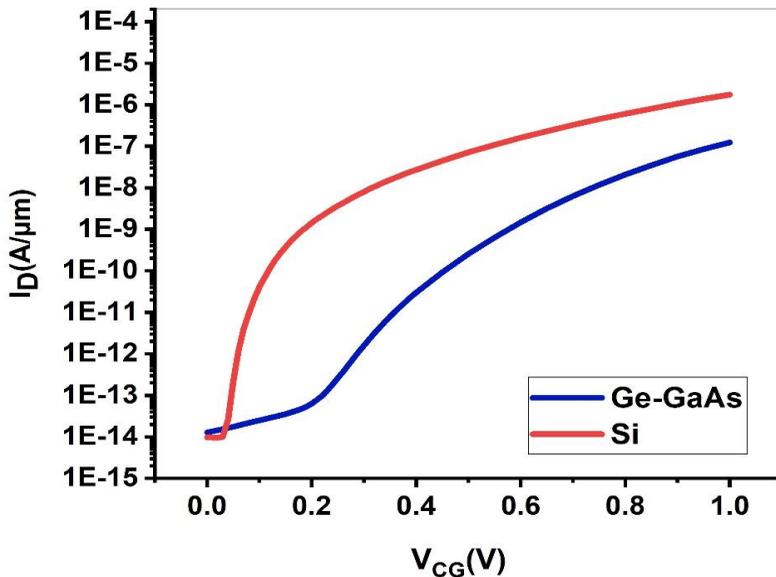
Fig. 5. I_D-V_{CG} curves of EDHTFET and homojunction Si based electrically doped TFET, for V_{DS}=1V, V_{PG}=-1 V.

The workfunction of control and polarity gates are very critical for estimating electrical performance of EDHTFET. The transfer characteristics of EDHTFET are illustrated in Fig. 6 for V_{DS} = 1V, as the workfunction of the gate electrode is varied. The gate workfunction modifies the electrostatically accumulated electrons of the channel region, which ultimately changes the barrier width at the source-channel junction. It is observed that as the workfunction of gate

electrodes increases, the threshold voltage moves toward higher positive values due to the reduction of electron density in the channel. This effect eventually leads to the enhancement of the tunneling resistance and higher control gate bias is required to transit from off-state to on-state. In Table.3, critical electrical parameters of the device are summarized as the gate workfunction value varies. It is observed that in n-channel EDHTFET, optimized gate workfunction should be determined to achieve the lowest possible positive threshold voltage.
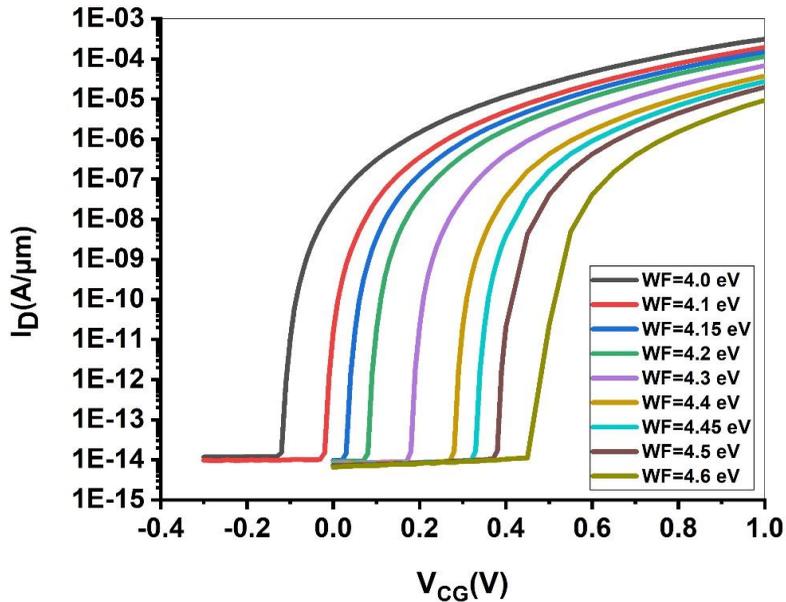

Fig. 6. I_D-V_{CG} curves of EDHTFET as the gate workfunction value is varied.

TABLE II

CRITICAL ELECTRICAL ELEMETS OF **EDHTFET** FOR VARIOUS VALUES OF METAL GATE WORKFUNCTION.

Electrical Parameters / Gate Workfunction	I_{on} (A/μm)	I_{off} (A/μm)	I_{on}/I_{off}	V_{th} (V)	SS (mV/dec)
WF= 4.0 eV	3.12×10^{-4}	1.18×10^{-14}	$2.66\times 10^{+10}$	- 0.13	5.39
WF= 4.1 eV	1.93×10^{-4}	9.63×10^{-15}	$2\times 10^{+10}$	- 0.03	4.65
WF= 4.15 eV	1.5×10^{-4}	9.59×10^{-15}	$1.56\times 10^{+10}$	0.02	5.15
WF= 4.2 eV	1.16×10^{-4}	9.21×10^{-15}	$1.26\times 10^{+10}$	0.07	5.05
WF= 4.3 eV	6.77×10^{-5}	8.48×10^{-15}	$7.99\times 10^{+9}$	0.17	4.86
WF= 4.4 eV	3.78×10^{-5}	7.85×10^{-15}	$4.81\times 10^{+9}$	0.27	4.92
WF= 4.45 eV	2.76×10^{-5}	7.29×10^{-15}	$3.78\times 10^{+9}$	0.32	4.97
WF= 4.5 eV	1.98×10^{-5}	7.12×10^{-15}	$2.78\times 10^{+9}$	0.37	4.98
WF= 4.6 eV	9.42×10^{-6}	6.52×10^{-15}	$1.45\times 10^{+9}$	0.45	15.1

The electrically doped hole density in the source region depends upon two critical design measures: gate workfunction and polarity gate bias. Figure. 7 illustrates the hole density along the carrier transport direction in the off-state for V_{DS}=0.05V and for different values of polarity gate. It is essential to mention that minimum drain bias is chosen for clarifying the sole impact of gate electrode workfunction on the hole density in the source and channel regions. It is demonstrated that for negligible values of the polarity gate, the electrically induced hole density in the channel highly depends upon the workfunction variation. The higher value of the gate workfunction induces higher hole density in the source region. However, on the other side, the increment of gate workfunction over the channel (control gate), reduces the electron concentration in the channel, which may eventually enhance the sufficient gate voltage for the band alignment and start of the tunneling. The results demonstrate that as the polarity gate (absolute value) enhances, the sensitivity of the electrically induced hole concentration to the gate workfunction variation, is fundamentally diminished. In this situation, optimum value should be calculated for the gate

workfunction to achieve the lowest possible positive threshold voltage (for n-channel operation) with improved on-state current.
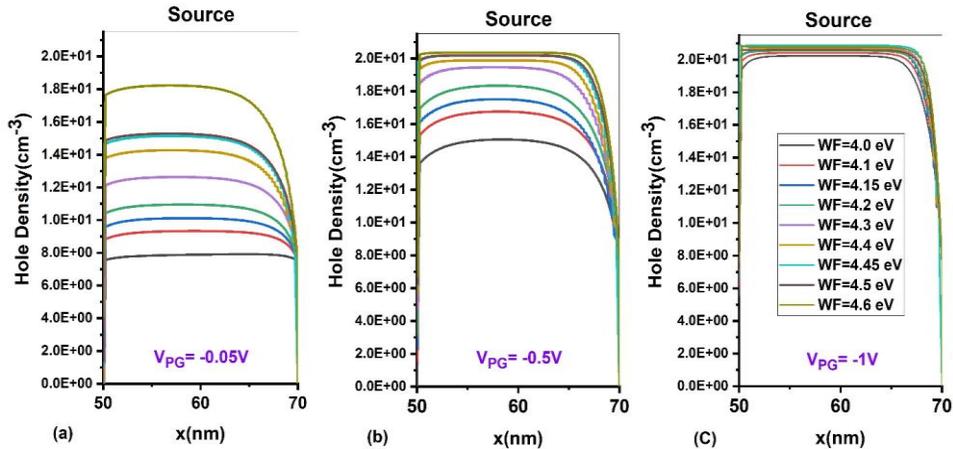
Fig. 7. Hole concentration along the device in the source region for different values of gate workfunction as the polarity gate voltage is varied. The drain bias is V_{DS}=0.05 V.

In principle, the probability of tunneling depends upon the formation of a steep p^+-n^+ junction at the interface of source-channel. It is expected that fundamental design variables may modify the tunneling rate. In order to assess this issue, statistical analysis is carried out to investigate sensitivity of EDHTFET essential electrical measures based on change of the fundamental design parameters. By definition, sensitivity is defined as:

$$Sensitivity(\%) = \frac{\sigma}{\mu} \times 100 \qquad (1)$$

Which is the ratio of standard deviation, σ, over the mean value, μ, in percentile. First, all the device parameters are considered in their initially defined values, omitting one. Next, the specified device parameter is changed and important electrical parameters of the device are calculated. Following that, the sensitivity of each electrical measures are calculated. The bar chart in Fig.8 shows the sensitivity of EDHTFET performance with reference to the change of design parameters. The results demonstrate that for the on-state current, channel thickness and gate workfunction play a fundamental role. The channel thickness

controls the gate coupling over the channel and gate workfunction modifies the carrier density both in the channel and source regions. It is evident that the drain bias affects the carrier velocity and it can significantly affect the on-state current. In addition, for the off-state current, temperature is a fundamental physical factor that affects the leakage current stems from minority carriers. However, at room temperature operation, polarity gate bias and channel thickness are important parameters that can affect off-state current. Both parameters also modify the minority carriers in the source. At room temperature operation, gate workfunction, channel thickness and polarity gates affects the threshold voltage. This is due to the high dependency of electron density in the channel and hole density in the source region to these parameters. Finally, all design parameters that may change the tunneling rate can modify subthreshold swing. In conclusion, for efficient performance of the device, gate work function and polarity gate bias value should be optimized for each channel thickness.
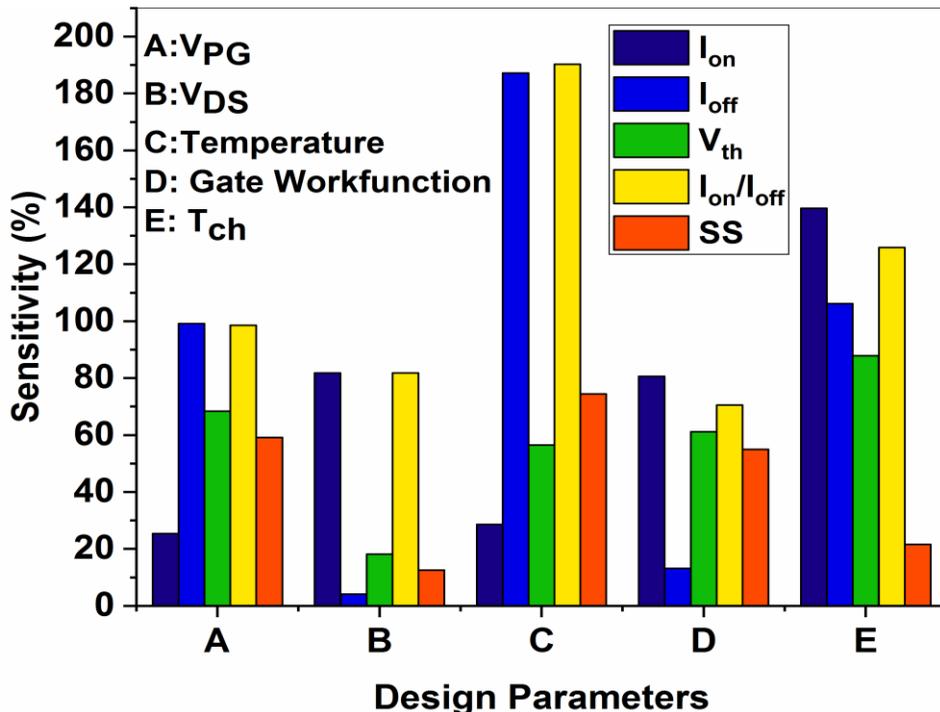

Fig. 8. Sensitivity bar chart of main electrical measures for the EDHTFET as a function of critical design parameters.

4. CONCLUSION

In this paper, performance of EDHTFET with electrostatic doping is comprehensively investigated as an emerging alternative for the conventional TFET. Basically, for improving performance of the device, Ge/GaAs staggered type heterojunction is employed as key materials for the tunneling junction. A parametric study of the effects of design factors on the efficiency of this device is carried out to evaluate the sensitivity of device main electrical measures while the device geometrical parameters are varied. The statistical analysis shows that by skillfully adjusting the gate material workfunction and also the polarity gate bias, a steep pseudo tunneling junction is formed in the aligned regions at the interface of the source-channel without any additional physical doping. The proposed EDHTFET shows significant improved performance such as amplified on-state current, steep switching characteristics (low subthreshold swing of 5.15 mV/dec) and low off-state current in comparison with the Si based TFET. Interestingly, it is showed that the wide band gap material of the channel region manifests screening of the tunneling junction at the source side from the drain voltage, suppressing short channel effects. This paper attempts to identify an advantageous replacement for low power, high speed applications and thus provides a roadmap for device designers in nanoscale regime.

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