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Design and Simulation of Two Low-Voltage, Low-Power Transresistance Instrumentation Amplifiers with Electronic Adjustment Capability

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Abstract

This article introduces two designs for transresistance amplifiers. The first and second precision instrument amplifiers (IAs) utilize ten and eight MOS transistors. Both proposed IAs were simulated with 0.18 µm CMOS technology and a supply voltage of ±0.7 V using Hspice software. According to the results, the Common Mode Rejection Ratio (CMRR) of the first IA can vary from 72.6 dB to 75.7 dB with a change in control voltage. In contrast, the second IA can range from 71.7 dB to 74 dB. The -3dB cutoff frequency for the CMRR of the first IA is accessible between 0.969 MHz and 16.4 MHz, and for the second IA, it ranges from 4.34 MHz to 40.8 MHz. The power consumption of the first proposed design varies from 203.33 µW to 372.77 µW within the adjustment range, and for the second proposed design, it changes from 234.57 µW to 338.73 µW. Time-domain analysis indicates that for a 20 µA(p-p) input signal, the maximum Total Harmonic Distortion (THD) at various frequencies for the first design is 3.37%. For the second design, it is 2.13%. The output impedance of the first proposed amplifier can vary from 779 to 1190 Ω with a change in control voltage, and the second proposed IA can change from 860 Ω to 1640 Ω. Therefore, these two circuits are suitable for amplifier applications with electronic adjustability in medical instruments, biosensor reading circuits, electrocardiography, and signal processing.

Keywords: Instrumentation Amplifier, Current Mode, Transresistance Mode, Common Mode Rejection Ratio (CMRR).

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1. INTRODUCTION

Instrumentation amplifiers, among the oldest and most utilized circuits, ensure the amplification of weak differential signals in the presence of noise and common-mode signals. Historically, instrumentation amplifiers were implemented using operational amplifiers and resistors [1]. Their main issue was the need for precise matching between resistors to achieve a high common-mode rejection ratio (CMRR). Another limitation associated with operational amplifier-based instrumentation amplifiers is their frequency-dependent gain. These weaknesses, coupled with the rapid scaling down of CMOS technology and lower allowable supply voltages, have made operational amplifier-based instrumentation amplifiers less attractive. In contrast to conventional voltage-mode signal processing, the new current-mode signal processing approach offers appealing features such as broad frequency performance, simpler circuitry, and low voltage operation. This new generation of instrumentation amplifiers is known as Current-Mode Instrumentation Amplifiers (CMIA) [2].

Numerous instrumentation amplifiers operate in voltage mode (VM) with voltage input and output or current mode (CM) with current input and output [3]. The rapid development of current-mode design and the emergence of many active elements have led to the introduction of amplifier structures based on Operational Transconductance Amplifier (OTA) [4], Differential Voltage Current Conveyor (DVCC) [5], Transconductance with Current Feedback or Current Feedback Operational Amplifier (CFOA) [6], Current-Controlled Current Conveyor Transconductance Amplifier (CCCCTA) [7], Current-Controlled Conveyor (CCCII) [8], and a resistorless current-mode instrumentation amplifier using 17 MOS transistors. On the other hand, low-voltage and low-power analog circuits are in high demand for easy integration and compatibility with digital systems [4,9].

In [10] the sensor uses a CNT as a movable electrode to sense gas pressure changes, and the proposed IA leverages the unique properties of CNTFETs to achieve high sensitivity, low noise, and low power consumption. This design eliminates the need for traditional resistors, providing a more efficient and compact solution for gas pressure sensing applications.

The article [11] examines various IA topologies with programmable gain capabilities (PG-IA). The study covers different implementation techniques, including Single Op-amp IA, Two and Three Op-amp IA, Switched Capacitor IA (SCIA), Current Feedback IA (CFIA), and Current Mirror IA (CMIA). The research highlights the advantages of using PG-IA in applications requiring high precision, high CMRR, low noise, and low power dissipation. The paper also discusses using V-to-I and I-to-V converters, Current Division Network (CDN), and Supply Current Sensing (SCS) approaches to enhance the performance of PG-IAs.

In [12], the amplifier is tailored for biomedical applications such as ECG, EEG, and EMG signal analysis. It features high CMRR, low power consumption, and the ability to operate at low voltages as shown in Table 2.

The device presented in [13], utilizes LM324/LM741 op-amps configured as an IA for precise signal amplification for portable ECG devices. It incorporates a 50 Hz notch filter and an active band-pass filter to eliminate noise and ensure signal integrity. The amplified signal is then digitized using an ESP-32 microcontroller, enabling the transmission of ECG data to an IoT platform for remote monitoring.

The article [14] presents a capacitively coupled chopper IA (CCIA) designed for biomedical applications. The amplifier operates with an ultra-low power consumption and utilizes a programmable bandwidth from 0.2 to 10 kHz. It incorporates a squeezed inverter amplifier (SQI) using a 0.2 V supply to efficiently address the primary noise source. The CCIA is implemented using 0.18 µm CMOS technology, achieving a high CMRR of 117.7 dB, and consuming only 0.47 µW of power. The design aims to provide flexible bandwidth without additional power consumption, making it suitable for wearable or implantable biomedical devices.

The development of a low-power, low-noise current-feedback IA for ECG acquisition is discussed in [15]. The design leverages a gm-boosted OTA to enhance performance while minimizing power consumption. Implemented in a 0.18 µm CMOS technology, the amplifier achieves a high CMRR and low power dissipation, making it suitable for portable and wearable biomedical devices.

The article [16] presents the design of a capacitively coupled IA using a novel hybrid feedback resistor. This IA is designed for physiological signal acquisition, addressing the need for high input impedance and precise amplification of low-frequency, low-amplitude signals. Implemented in a 130 nm CMOS process, the IA achieves a high-pass corner of 73.9 mHz and demonstrates robustness against process, voltage, and temperature (PVT) variations. Combining switched-capacitor (SC) low-pass filters, SC resistors, and continuous-time low-pass filters, allows the IA to achieve high resistance values with minimal sensitivity to PVT changes.

The current-mode approach has recently attracted attention in integrated circuit design due to its numerous advantages (such as high bandwidth, wide dynamic range, high linearity, low power consumption, and circuit simplicity) over the voltage-mode approach [3, 17-19]. Thus, this article will present an improved current-mode instrumentation amplifier with a differential input transconductance amplifier followed by a current follower. The second section elaborates on the principles and fundamentals of the proposed instrumentation amplifier. The third section presents the simulation results of the designed circuit to confirm the efficiency of the proposed structure. These results are compared with some of the recent works. Finally, the article concludes in the fourth section.

2. PROPOSED INSTRUMENTATION AMPLIFIERS

The first proposed instrumentation amplifier, which uses only ten MOS transistors, is shown in Fig. 1, and the second proposed amplifier, using only eight MOS transistors, is displayed in Fig. 2. These amplifiers are constructed from two current mirrors, a

unity-gain inverting amplifier, and two MOS transistors acting as a voltage-controlled resistor. Transistors M1 to M4 are utilized to invert the input current I1. The input current I2 is summed with the inverted current (I1) and converted to voltage through the equivalent resistance (R_{eq}).

The voltage difference across the gate inputs of M1 and M2 determines the current difference across their drains as Eq (1).

$$\Delta V_{GS} = V_{GS1} - V_{GS2} \quad (1)$$

The drain currents of M1 and M2 are related by the voltage difference across their gates.

$$ID_1 - ID_2 = f(\Delta v_{GS}) \quad (2)$$

Transistors M3 and M4, together with M5 and M6, form active loads on the drains of M1 and M2. These active loads improve the gain of the differential amplifier.

$$ID_1 \approx IM_3 + IM_4$$
$$ID_2 \approx IM_5 + IM_6 \quad (3)$$

The output of the amplifier is taken from the node between transistors M5 and M6. Then the output voltage is described as Eq (4).

$$V_{OUT} = VDD - R_{OUT} ID_2 \quad (4)$$

$$I_{SS} = ID_1 + ID_2 = I_b \quad (5)$$

M5 and M6 form a unity-gain inverting amplifier, transferring the generated voltage through Req to the output node. The *W/L* ratio of transistors M5 and M6 should be sufficiently large to ensure a low output impedance.

It is evident that the second proposed design requires fewer transistors in its variable resistance structure and also does not need a separate voltage source to bias the non-ideal current source. A simple node analysis of the circuit in Fig. 2 concludes:

$$V_{out} = (I_1 - I_2) R_{eq} \quad (6)$$

For a differential input $I_{id} = I_1 - I_2$, the differential mode gain (A_d) of the proposed amplifier is obtained as follows:

$$A_d = \frac{V_{out}}{I_{id}}\bigg|_{I_1 = -I_2} = R_{eq} \quad (7)$$

The R_{eq} can be adjusted by the parameters of four MOS transistors and the control voltages V_C and $-V_C$, which provides the highly desirable feature of electronic adjustability. Furthermore, the proposed amplifier is suitable for integration due to the

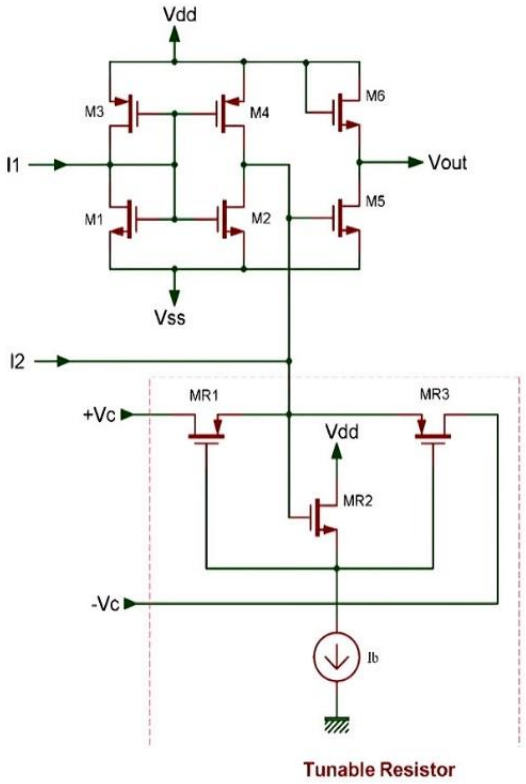


Fig. 1. First proposed IA.

ease of implementing the grounded resistance. Assuming that MR_1 and MR_2 have equal ratios, the equivalent resistance is expressed as follows [17]:

$$R_{eq} = \frac{L}{2\mu C_{ox} W (V_C - V_{TH})} \quad (8)$$

In this context, W and L represent the width and length of the transistor channel, respectively. The equivalent resistance R_{eq} can be adjusted by varying the control voltages $+V_C$ and $-V_C$, which modulate the resistance of the MOS transistors operating in the linear region. This electronic adjustability is a significant advantage as it allows fine-tuning the amplifier's performance without requiring physical changes to the circuit components.

As evident from Eq (1), for a common-mode input I_{icm} = 0.5 (I_1+I_2), the common-mode gain (A_C) of the proposed instrumentation amplifier in Fig. 2 is derived as shown in Eq (9).

$$A_c = \frac{V_{out}}{\frac{I_1+I_2}{2}}|_{I_1=I_2} = 0 \quad (9)$$

As can be inferred from Equ (4), the common-mode gain of the proposed amplifier in an ideal state is equal to zero. Consequently, Eq (5) indicates that the proposed amplifier has a very high intrinsic CMRR [18].

$$CMRR = \left|\frac{A_d}{A_c}\right| = \infty \quad (10)$$

However, if the non-ideal gains of current mirrors and inverting amplifiers are considered as unity, the output is assumed as Eq (11):

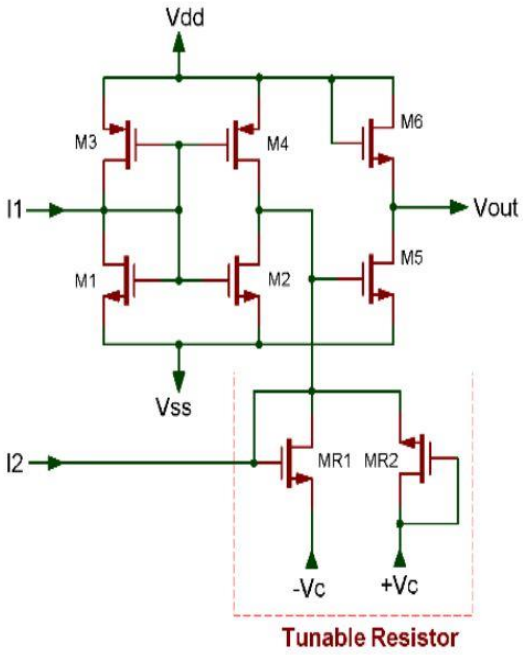


Fig. 2. Second proposed IA.

$$V_{out} = \beta(\alpha I_1 - I_2)R_1 \quad (11)$$

Here, α and β represent the non-ideal gains of current mirrors and the inverting voltage amplifier. Therefore, considering that $I_1 = I_{icm} + I_{id}/2$ and the differential gain (A_d), the common-mode gain (A_C), and the *CMRR* in the proposed amplifier, Eqs (12) to (14) can be calculated.

$$A_d = \frac{R_1}{2}\beta(\alpha + 1) \quad (12)$$

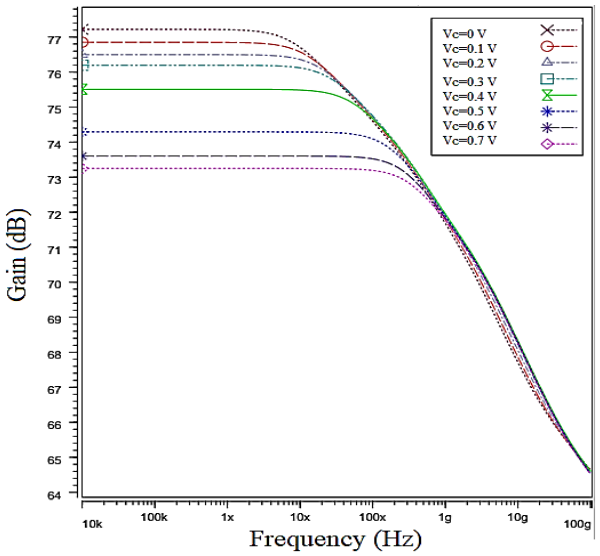
$$A_c = \beta R_1(\alpha - 1) \quad (13)$$

$$CMRR = \frac{1}{2}\left|\frac{\alpha + 1}{\alpha - 1}\right| \quad (14)$$

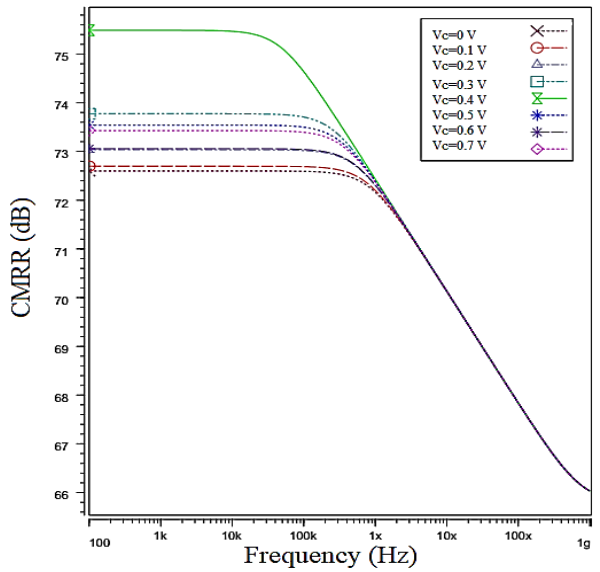
Eq (9) shows that the inverting voltage amplifier's non-ideal gain does not significantly affect the CMRR. On the other hand, if α is close to 1, a very high CMRR can be achieved [17,118].

3. SIMULATION RESULTS OF THE PROPOSED CIRCUITS

The first proposed design, utilizing 180 nm CMOS technology, was simulated under a supply voltage of ±0.7 V and at a default temperature of 25 °C. The threshold voltage (V_{TH}) for the NMOS transistors is approximately 0.4 V. All transistors operate in the saturation region, and a 10 kΩ load resistance is connected to the output. In the proposed circuit, the value of Vc was varied from zero to 0.7 V to achieve different differential mode gains. Fig. 3(a) shows that the differential mode gain of the proposed circuit varies from 75.9 dB to 77.9 dB with a -3dB bandwidth ranging from 76.2 MHz to 345 MHz. The proposed instrument amplifier's minimum and maximum power



(a)



(b)

Fig. 3. (a) Frequency response (b) CMRR variations in the first proposed IA.

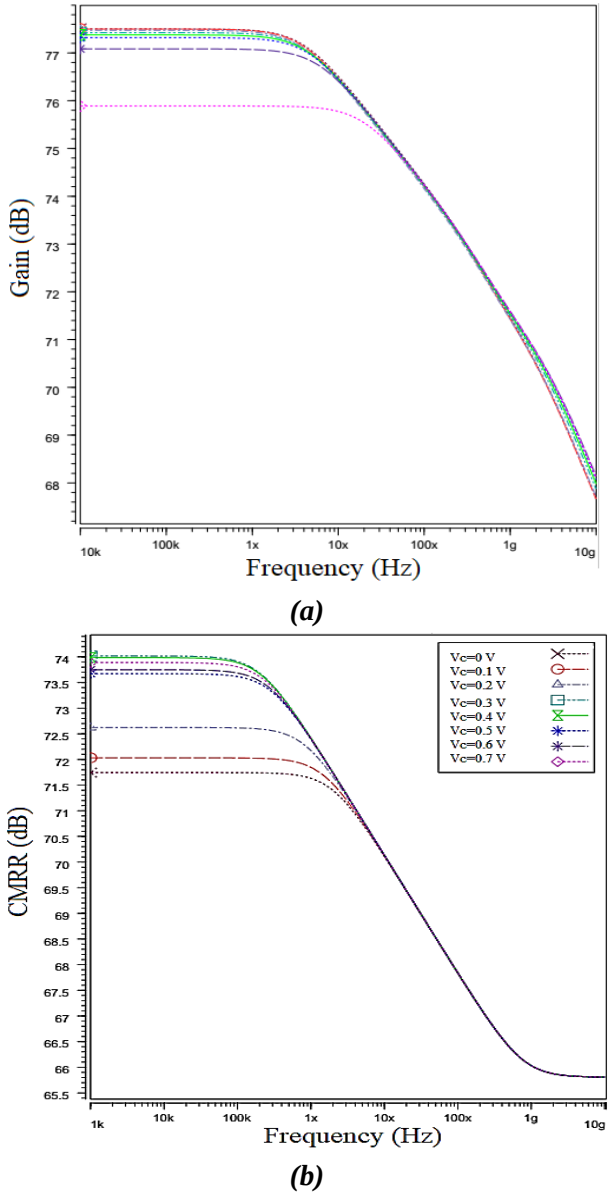
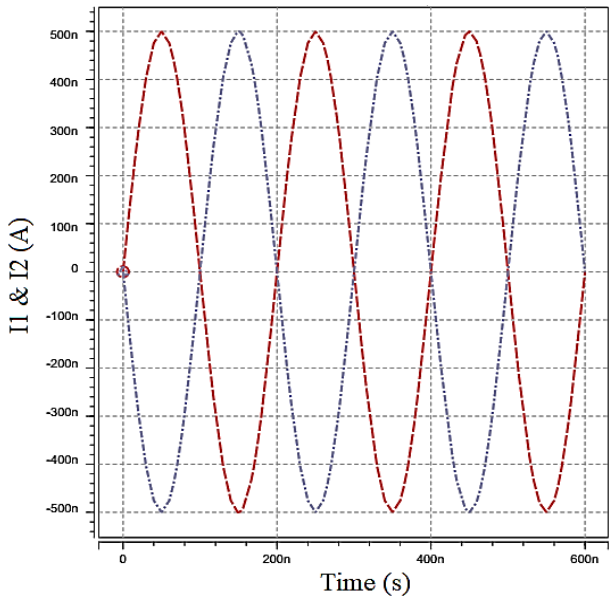


Fig. 4. (a) Frequency response (b) CMRR variations in the second proposed IA.

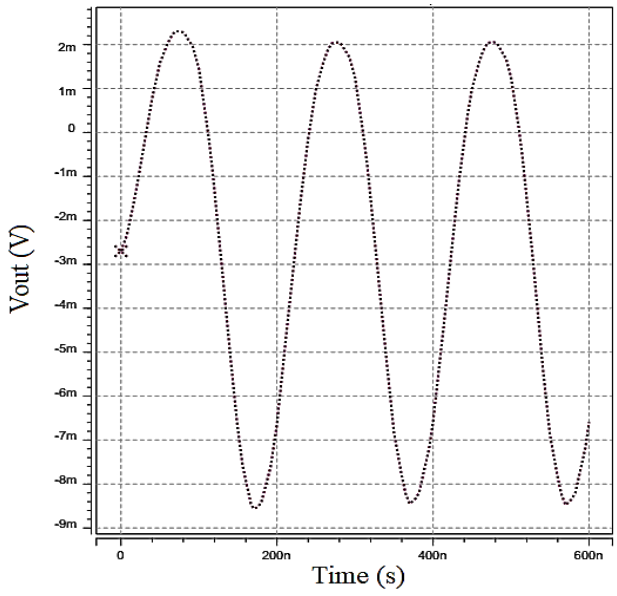
consumption in the adjustable range are 203.33 µW and 372.77 µW, respectively. The changes in CMRR in the proposed amplifier relative to frequency for different Vc values are shown in Fig. 3(b). As observed, the CMRR value of the proposed circuit varies from 72.6 dB to 75.7 dB, with a -3dB bandwidth ranging from 0.916 MHz to 16.4 MHz. It can be inferred that the proposed structure can effectively reduce unwanted common-mode signals while having a straightforward structure consisting of ten transistors.

In the proposed second circuit, the value of V_c was varied from 0 to 0.7 V to achieve different differential mode gains. Fig. 4(a) shows that the differential mode gain of the proposed circuit varies from 73.2 dB to 77.2 dB, with a -3dB bandwidth ranging from 148 MHz to 3.23 GHz. The proposed

instrumentation amplifier's minimum and maximum power consumption within the adjustable range are 157.15 µW and 338.73 µW, respectively. Changes in CMRR relative to frequency for different values of V_c are shown in Fig. 4(b). As observed, the CMRR value of the proposed circuit ranges from 71.7 dB to 74 dB, with a -3dB bandwidth ranging from 4.34 MHz to 40.8 MHz. It can be inferred that the proposed structure can effectively reduce unwanted common-mode signals while having a simple structure composed of eight transistors.



(a)



(b)

Fig. 5. Transient response of the 1st proposed IA. (a) differential input currents, (b) output voltage.

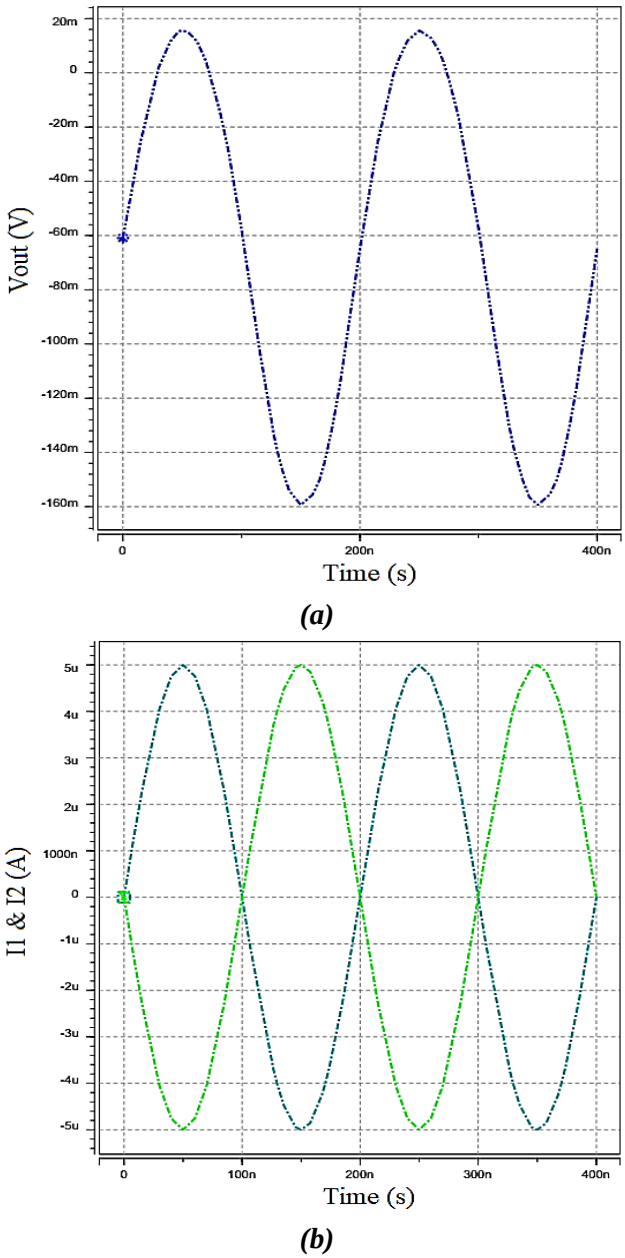


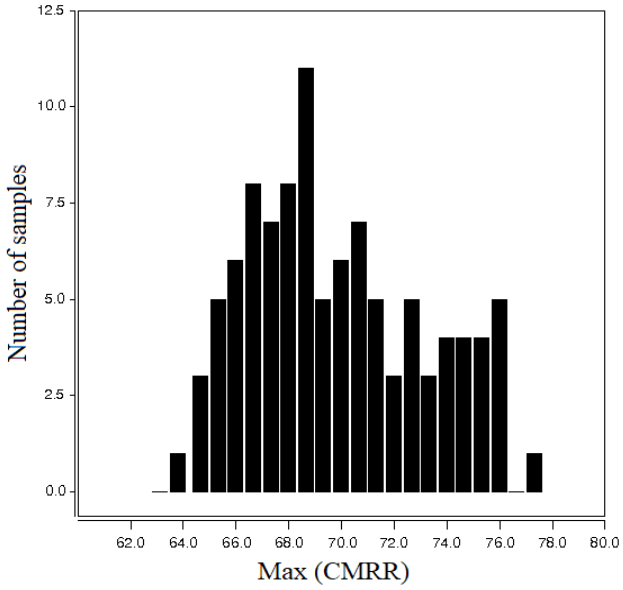
Fig. 6. Transient response of the 2nd proposed IA. (a) differential input currents, (b) output voltage.

To evaluate the time-domain response of the first proposed amplifier, a differential-mode sinusoidal input (I_1-I_2) with a peak-to-peak amplitude of 20 µA at a frequency of 5 MHz was applied to the inputs. The control voltage was set to 0.5 V. Fig. 5 shows that the amplified output voltage is approximately 11 Mv(p-p), with a differential-mode gain of 77.2 dB and a Total Harmonic Distortion (THD) of 3.37 percent. Additionally, the THD value remains below 3% for various frequencies.

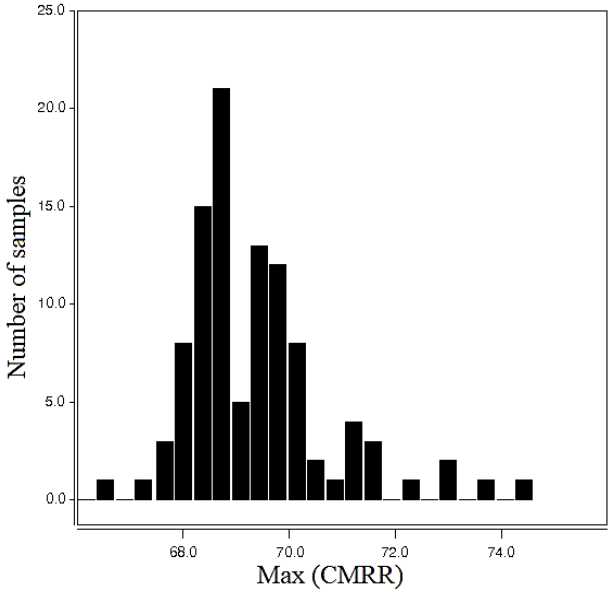
To examine the proposed second amplifier's time-domain response, a differential-mode sinusoidal input with a peak-to-peak amplitude of 20 µA at a frequency of 5 MHz was applied to the inputs. The control voltage V_c was set to 0.5

V. Fig. 6 shows that the amplified output voltage is approximately 170 mV(p-p), with a differential mode gain of 77.2 dB and a Total Harmonic Distortion (THD) of 2.13%. Additionally, the THD value remains below 0.5% for different frequencies.

To investigate the changes in CMRR for the first proposed design under mismatch conditions, a Monte-Carlo simulation considering Process, Voltage, and Temperature (PVT) variations for the transistors was carried out across 100 runs with Vc = 0.5 V. The statistical distribution of CMRR in the presence of mismatch is shown in Fig. 7(a). As observed from the Monte Carlo simulation results, the first proposed structure displays a CMRR value of 69 dB with the highest probability.



(a)



(b)

Fig. 7. Transient response of the 1st proposed IA. (a) differential input currents, (b) output voltage.

Table 1. ***Comparison between the simulation results of the first and second proposed IAs.***

parameter	First proposed circuit	Second proposed circuit
Technology (nm)	180	180
Supply voltage (V)	±0.7	±0.7
power consumption (µw)	203.33 ~ 372.77	157.15 ~ 338.73
Differential mode gain (dB)	75.9 ~ 77.5	73.2 ~77.2
f_{-3dB} (MHz)	76.2 ~ 345	148 ~ 323
CMRR (dB)	72.6 ~ 75.7	71.7 ~ 74
Output-referenced noise at 10 kHz (pA/$\sqrt{Hz}$)	64.6	77.8
Output Impedance (**Ω**)	779 ~ 1190	860 ~ 1640
Linearity percentage @ 5 MHz and 1 µA (p-p)	3.37	2.13
Chip area (µm^2)	1030.2	861

A similar Monte Carlo analysis was conducted to examine the changes in CMRR. Table 1 compares the results of the first and second proposed designs. Both proposed designs have similar differential mode gain and common-mode rejection ratio values. The disadvantages of the first proposed design include high power consumption, low -3dB cutoff frequency, large occupied area, and worse linearity. Therefore, for comparison with previous works, the second proposed design is considered.

The second proposed design is considered under mismatch conditions. The statistical distribution of CMRR in the presence of mismatch is illustrated in Fig. 7(b). According to the simulation results, the second proposed structure indicates a CMRR value of approximately 68.75 dB with the highest probability. Both outcomes demonstrate robust performance against PVT variations.

A comparison of the proposed instrumentation amplifier with some other reported works is presented in Table 2. The transistor characteristics, including the technology node, and applied power supply are specified to ensure a fair comparison with similar reported works. It is observed from Table 2 that the proposed instrumentation amplifier exhibits lower power consumption, fewer transistors, and electronic adjustability, demonstrating superior performance compared to previous works.

4. CONCLUSION

This article introduces two precision IAs with 10 and 8 transistors. The second IA is more suitable for integration due to its simple structure achieved by having only two transistors between the power supply lines, resulting in a very low supply voltage. The differential gain of the proposed precision

Table 2. ***Comparison between the proposed instrumentation amplifier and some reported works.***

	Year	●	Active Elements Used	■	◊	# R&C	CMRR (dB)	f_{-3dB} (MHz)	☼	Power diss. (mW)	Area (mm^2)
[2]	2013	180	--	✓	17	0	91	-	±0.8	0.219~0.446	-
[7]	2020	180	DDCC (#1)	×	40	0	146	1	±0.8	0.492	-
[11]	2023	130	IA, Op-Amps, OTAs	✓	4 Op-Amps & OTAs,	Multi.	120	83	3.3	0.77	-
[12]	2022	130	OTAs-	✓	3 OTAs	0	54	Varied	1.8	90	-
[13]	2023	-	LM324/741, Op-Amps, ESP-32	×	-	Multi.	96	0.5-250 Hz	±5	-	-
[14]	2023	180	SQI Amplifier and Transistors	✓	-	Multi.	117.7	0.2-10 kHz	0.2, 0.8	0.00047	0.083
[15]	2023	180	gm-boosted OTA	×	-	Multi.	110	-	0.8	0.55	-
[16]	2024	130	Switched-capacitor filter, SCR, PR	×	-	Multi.	-	0.0739	-	-	0.16
[17]	2017	180	COA (#2)	✓	29	2	36~54.2	0.359~0.383	±0.9	0.76	-
[18]	2018	180	COA (#2)	✓	30	1	51.2	0.068	±0.9	0.864	-
[19]	2018	180	CFDITA (#2)	✓	34	0	52.8~64.7	3.76~46.2	±0.9	1.15~1.3	-
[20]	2009	350	CCCCTA (#2)	✓	34	0	94	-	±1.5	4.43	-
[21]	2023	180	DVTA (#3)	✓	24	1	146.8	30	±0.9	0.368	0.0095
*	-	180	-	✓	8	0	71.7~74	4.34~40.8	±0.7	0.157~0.338	0.00086

● = Technology (nm) ; ■ = Adjustability ; ◊ = #Transistors & Active Comp. ; ☼ = Power Sup. (V) ; * = Proposed

instrumentation amplifier can be electronically adjusted by changing the control voltages. Furthermore, a high CMRR is achieved using only eight MOS transistors, eliminating the need for resistance matching. The proposed amplifier was simulated using 0.18 µm CMOS technology with a ±0.7 V supply voltage. Simulation results indicate that the CMRR of the proposed precision instrumentation amplifier can vary from 71.7 to 74 dB with control voltage adjustments. The f3dB for the CMRR varies between 4.34 ~ 40.8 MHz. The power consumption of the proposed design varies from 234.57 µW to 338.73 µW during adjustment. Time-domain analysis revealed that for an input signal with

a 10 µA peak, the maximum THD is 0.21%. Additionally, the Rout of the proposed precision IA can vary between 860 ~ 1640 Ω with control voltage adjustments.

REFERENCES

[1] T. A. Baghi-Rahin, V. Baghi-Rahin, "A 0.5 V operational transconductance amplifier based on dynamic threshold-voltage MOSFET and floating gate MOSFET inverters in 180 nm CMOS technology," Journal of Intelligent Procedures in Electrical Technology (JIPET), Vol. 15, no. 60, pp. 1-18, March 2025 (in Persian).

[2] Safari, L., & Minaei, S. (2013). A novel resistor-free electronically adjustable current-mode instrumentation amplifier. *Circuits, Systems, and Signal Processing*, *32*, 1025-1038.

[3] Yuce, E. (2010). Various current-mode and voltage-mode instrumentation amplifier topologies suitable for integration. *Journal of Circuits, Systems, and Computers*, *19*(03), 689-699.

[4] Baghi Rahin, A., & Baghi Rahin, V. (2019). A new 2-input CNTFET-based XOR cell with ultra-low leakage power for low-voltage and low-power full adders. *Journal of Intelligent Procedures in Electrical Technology*, *10*(37), 13-22.

[5] Zanjani, S. M. A., & Parvizi, M. (2021). Design and simulation of a bulk driven operational trans-conductance amplifier based on CNTFET technology. *Journal of Intelligent Procedures in Electrical Technology*, *12*(45), 65-76.

[6] Pertijs, M. A., & Kindt, W. J. (2010). A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping. *IEEE Journal of Solid-State Circuits*, *45*(10), 2044-2056.

[7] Ettaghzouti, T., Bchir, M., & Hassen, N. (2020). High CMRR voltage mode instrumentation amplifier using a new CMOS differential difference current conveyor realization. *International Journal of Electrical and Electronic Engineering & Telecommunications*, *9*(3), 132-141.

[8] Maheshwari, S. (2003). High CMRR wide bandwidth instrumentation amplifier using current controlled conveyors. *International Journal of Electronics*, *89*(12), 889-896.

[9] Rahin, A. B., & Kanani, Z. D. K. (2014). A Low-Voltage and Low-Power Programmable Gm-C Filter for Wireless Applications. *Journal of Intelligent Procedures in Electrical Technology (JIPET)*, *5*(19), 3-10.

[10] Zanjani, S. M. A., Dousti, M., & Dolatshahi, M. (2018). High-precision, resistor less gas pressure sensor and instrumentation amplifier in CNT technology. *AEU-International Journal of Electronics and Communications*, *93*, 325-336.

[11] Sharma, D., Shylashree, N., Prasad, R., & Nath, V. (2023). Analysis of Programmable Gain Instrumentation Amplifier. *Int. J. Microsyst. Iot*, *1*, 41-47.

[12] Gajare, M., & Shedge, D. K. (2022). CMOS trans conductance based

instrumentation amplifier for various biomedical signal analysis. *NeuroQuantology*, *20*(5), 53.

[13] Raptan, S., Bhattacharyya, A., Das, N., Pandey, I., & Bhattacharjee, S. (2023, March). "Cardioxy"–A Novel and Portable Instrumentation Amplifier based and IoT enabled ECG device. In *2023 2nd International Conference for Innovation in Technology (INOCON)* (pp. 1-5). IEEE.

[14] Pham, X. T., Kieu, X. T., & Hoang, M. K. (2023). Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications. *Journal of Low Power Electronics and Applications*, *13*(2), 37.

[15] Gupta, S. K., Ahmad, R., Singh, P., Boolchandani, D., & Kar, S. K. (2023, March). A Low-Power Low-Noise Current-Feedback Instrumentation Amplifier based on g m boosted OTA for ECG Acquisition. In *2023 10th International Conference on Signal Processing and Integrated Networks (SPIN)* (pp. 733-738). IEEE.

[16] Xu, H., Liu, Y., Duan, Y., Li, T., Zhang, J., Li, Z., & Zhang, H. (2024). A PVT-Robust and 73.9 mHz High-Pass Corner Instrumentation Amplifier with an SCF-SCR-PR Hybrid Feedback Resistor. *Electronics*, *13*(2), 366.

[17] Safari, L., & Minaei, S. (2017). A novel COA-based electronically adjustable current-mode instrumentation amplifier topology. *AEU-International Journal of Electronics and Communications*, *82*, 285-293.

[18] Safari, L., Minaei, S., Ferri, G., & Stornelli, V. (2018). Analysis and design of a new COA-based current-mode instrumentation amplifier with robust performance against mismatches. *AEU-International Journal of Electronics and Communications*, *89*, 105-109.

[19] Chaturvedi, B., & Kumar, A. (2018). Electronically tunable current-mode instrumentation amplifier with high CMRR and wide bandwidth. *AEU-International Journal of Electronics and Communications*, *92*, 116-123.

[20] Chanapromma, C., Tanaphatsiri, C., & Siripruchyanun, M. (2009, February). An electronically controllable instrumentation amplifier based on CCCCTAs. In *2008 International Symposium on Intelligent Signal Processing and Communications Systems* (pp. 1-4). IEEE.

[21] Raj, N., Dutta, S., Ranjan, R. K., Singh, D. K., & Kuntman, H. (2023). VDTA Based Transadmittance Mode Instrumentation Amplifier with Experimental results.