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Evolutionary QCA Universal and Testable Gate

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Abstract

Quantum-dot Cellular Automata (QCA) with properties such as high density and low power consumption is a promising technology for VLSI future. But high error rate is a disadvantage of this technology, hence it is necessary to design circuits with testability. In this paper a new universal and testable 3×3 gate is designed. This gate is a kind of intelligent systems; because the possible system error can be distinguished by the output values. This gate is designed in a way that it has always 2 ones and one zero in its outputs. When the gate works properly the majority of the outputs must be one and the logical AND operation of the outputs must be zero. Thus in the presence of any transient and permanent fault such as single missing cell the majority and AND of the outputs are not equal to those in fault free operation. Then the performance of this gate is compared with useful testable Fredkin gate and is shown that for implementing logic functions this gate has a better performance in terms of complexity and delay in comparison with Fredkin gate.

Keywords: QCA; Defect; Fault Tolerant; intelligent system; Testable gate
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1. Introduction

CMOS have some limitations to provide future nanotechnology requirements. Reducing feature size in CMOS transistors at nano scale will meet problems like power dissipation, lithographic problems and some other limitations. Quantum dot cellular automata can eliminate these problems somewhat. In QCA, unlike CMOS, flow of electrons is not used to propagate binary information. Rather, binary values are shown by state of the polarizations and columbic interactions can propagate information. Therefore, power dissipation can be reduced significantly [1-3]. Despite these advantages, some problems must be solved to improve the performance of QCA. High error rate is one of the fundamental problems in QCA. So it is necessary to detect errors in the circuits. Some woks focus on testing QCA circuits. Deposition defects were analysed in QCA combinational circuits in [4], and single missing and additional cell defect was characterized for QCA devices such as majority voter, inverter, L-shaped wire, fan-out and cross wire. In [5] concurrently testable latches for QCA were designed by using Fredkin gate. Fredkin is a conservative gate in which the number of one's in the output and input are equal. So the parity in the inputs must be equal to the parity of the outputs. D latch, T latch, JK latch and SR latch by using Fredkin gate was designed and showed that any transient or permanent defect causes parity mismatch between inputs and outputs. A new conservative QCA gate was designed in [6] and showed that any transient and permanent fault can be detected by using conservative logic. Also it was shown that the designed gate has the better performance in implementing logic functions in comparison with Fredkin gate. In [7] reversible gates were used to design testable structures. 1-D array of reversible gates was proposed and testability of these structures was investigated under single faults. In [8] fault tolerant designs were proposed by using triple modular redundancy. Defect tolerance of QCA sequential devices was analysed in [9] and the effect of the single missing/additional cell defect on the behaviour of the SR flip-flop was investigated. QCA tile structures were proposed in [10] and the defect

tolerance of such structures were analysed. It was also shown that tile based QCA devices are less sensitive to deposition defects. In [11] a test generation frame work for QCA was proposed and it was shown that stuck at fault test set is not enough to detect all the defects, and additional test vectors are needed. As mentioned before, Fredkin gate is a testable gate that can implement logic functions. This gate is a parity-preserving gate so a fault can be detected by comparing parity of the inputs and outputs [12]. In this paper, a new testable gate (NR gate) is designed with two ones and one zero at the output. So the logic AND and majority of the outputs must be zero and one respectively. Any single transient and permanent fault can be detected by computing majority and logic AND of the outputs. This paper is organized as follows. Section 2 presents a review of QCA and explanation of its concept, clocking and basic elements. In section 3 QCA defects are proposed. Section 4 proposes new testable gate and shows the method of testing. In section 5, simulation of the gate NR is done and the results are shown. Section 6 analyses the manufacturing defects in the gate NR, and finally section 7 concludes the work.

2. Review of QCA

A) concept of QCA

Quantum-dot cellular automata is a new technology that uses the state of polarization to encode the binary information. Each quantum cell has four quantum dots and two mobile electrons. Due to columbic repulsion the electrons occupy the farthest dots in cell that results in lowest energy state. So each cell has just two stable states that correspond to polarizations p=-1 and p=+1 and a third null state that corresponds to p=0. Polarization p=-1 equals to binary zero and p=+1 equals to binary one. The null state shows no binary information. There are two types of QCA cell: 90° cell and 45° degree cell [13-15]. These cells with two possible charge configurations and the equivalent binary information are shown in Fig. 1 and Fig. 2 respectively.

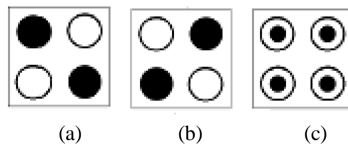

Fig. 1. 90° QCA cell. (a) binary zero. (b) binary one. (c) null state

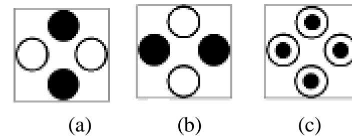

Fig. 2. 45° QCA cell. (a) binary zero. (b)binary one. (c) null state

B) Basic logic elements in QCA

The majority gate is shown in Fig. 3. This gate results in the majority of the 3 inputs in the output. By setting one input to +1 or -1 logic OR/AND of the other inputs will be resulted in the output. Also inverter gate is also shown in Fig. 3.

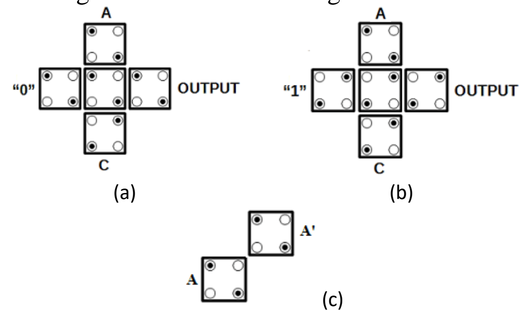

Fig. 3. Digital gates with QCA. (a) AND gate (b) OR gate (c) inverter gate

C) Clocking QCA

The electrons in the potential wells require high potential energy to tunnel between quantum dots. This energy is provided by QCA clock. When the clock is high, the potential barriers are low so the electrons are allowed to move between dots. When the clock is low the potential barriers are high so the electrons are trapped in the dots. Clock in QCA has four phases. As well as for power supplement, QCA clock is used for logic synchronization.

The four phases are switch, hold, release and relax as it is shown in Fig. 4(a). In switch phase the potential barriers between quantum dots are rising up and a QCA cell is getting a polarization according to its neighbor cell polarization. In hold phase potential barriers are high and tunneling between quantum dots is suppressed. Hence the QCA cell has a fix polarization. In release phase potential barriers are decreasing and in the relax phase the barriers enough so electrons can tunnel freely between quantum dots, and QCA cell has no special polarization. According to the four clock phases, there are four clock zones. In QCA circuit, each cell must be assigned to a zone. The arrangement of clock zones determines the direction of information flow [16-18]. Clock zones are shown in Fig. 4(b).

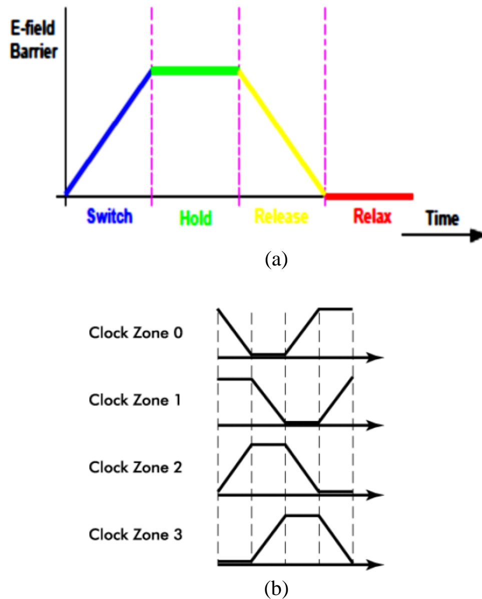

Fig. 4. (a) four phases of clock. (b) clocking zones

3. Manufacturing defects in QCA

There are four major groups of defect that can be produced during manufacturing process. (1) cell displacement, (2) cell misalignment, (3) missing cell, and (4) additional cell. Incorrect deposition process causes these defects. Cell displacement refers to the defect that a cell is displaced from its original position. Cell misalignment refers to the defect that direction of a cell is misplaced with respect to the other cells. Missing cell occurs when a cell is omitted in the layout and additional cell defect occurs when there is an unwanted cell in the layout [19]. This paper focuses on single missing cell defect. In Fig. 5 a majority gate under this defect is shown.

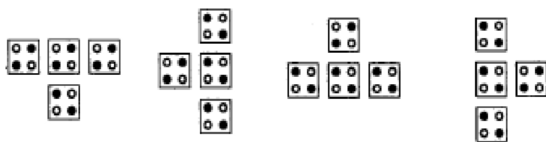

Fig. 5. Majority gate with single missing defect

4. New testable gate

A) Designing testable gate

Here a new method is introduced to design a testable gate. Assume two outputs are one and the other is zero. Under these conditions the majority of the outputs must be one and the logic AND operation must be zero. In the presence of a fault at outputs the majority and the logic AND will be not equal to those in fault free operation. So it is possible to test the gate by computing outputs majority and AND. To design an appropriate gate another major point must be considered. The applicable gate must be able to implement logic functions with low complexity and delay. To design the desired gate, function $P = AB + \bar{A}\bar{C}$ is applied here as the firs gate output. This function can provide NOT, AND, NAND, NOR and NOR easily. So applying this function is very useful to implement logic functions [20]. In order to obtain two other functions for the remained outputs all other cases that produce two one's and one zero in the output must be considered. Each obtained gate then is applied to implement the 13 standard logic functions and finally the one that implements these functions with the lowest complexity and delay will be chosen. The gate is shown in Fig. 6, and has the best performance to implement 13 standard functions. Its truth table is shown in Table 1.

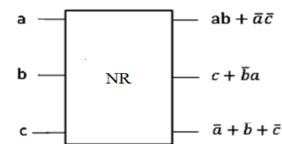

Fig. 6. Testable gate NR

Table.1.
Truth table of testable NR gate

a	*b*	*c*	*p*	*q*	*r*
0	0	0	1	0	1
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	0

B) Testing NR gate

Presence of two ones and one zero can detect any single fault at output. As mentioned in previous section, under these conditions and in fault free operation the majority of the outputs must be one and the logic AND must be zero. If a fault occurs in the output that in fault free operation is zero, the logic AND will be one and if a fault occurs in the output that in fault free operation is one, the majority of the outputs will be zero. Outputs of the NR gate are 011, 101 and 110. Table 2 shows all the faults that can occur for each output and the testing result for each fault. As shown in the table when there is a fault in the output, logic AND or the majority of outputs is not equal to that in fault free operation. Testable block of this gate is shown in Fig. 7. When there is no fault in the output, majority and logic AND must be complementary, so two pair two rail checker can be used to test more blocks as shown in Fig. 8.

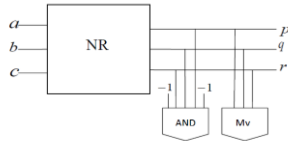

Fig. 7. Testable block

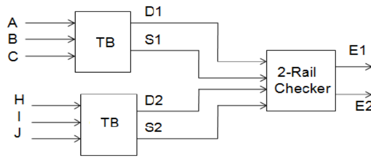

Fig. 8. Checking two testable blocks by two pair two rail checker

Two pair two rail checker has four inputs. When D1/S1 and D2/S2 are complement, the outputs E1 and E2 will also be complement [21]. In Fig. 8 TB is testable block shown in Fig. 7 and D1/S1 and D2/S2 are the outputs of the test circuits of each testable block. If the E1/E2 are complementary, it can be concluded that D1/S1 and D2/S2 are also complement. It means two blocks work correctly and there is no fault in the gates.

C) *Simulation Results*

The bistable approximation engine is used for the simulation and set the number of samples = 180000. All other parameters are set to default values. The layout of the gate is shown in Fig.9. As it can be seen, the layout has six clock zones. Simulation result is shown in Fig. 10.

5. Fault detection

QCA circuits suffer from transient and permanent faults. Permanent faults occur during manufacturing process. Thermodynamic effects, radiation and other effects, cause transient faults [22]. Any transient and permanent fault can be detected in the NR gate by applying a majority gate and logic AND gate in the output as a test circuit as shown in pervious sections. Here, single missing cell defect is induced in the majority voter, inverter, L-shaped wire, fan-out and crosswire to show how this defect can be detected in gate NR. In other words, in each step one cell is omitted and the obtained circuit, simulated by QCA Designer and simulation results are analysed. Table 3 shows the simulation results after omitting a cell in the circuit. In this table F.F refers to fault free output, FPi refers to the faulty output and ai is a 3 bit pattern that has an equivalent decimal value of I, for example a5 represents 101. As it is obvious in the table, when a fault occurs in the output due to single missing cell defect majority or logic AND of the outputs is not equal to those in fault free operation. For example, input a1 results in a3. According to the column 3 in the presence of a defect, this input results a7. a3 has the majority of one and the logic AND of zero. However, a7 has the majority of one and the logic AND of one.

6. Implementing 13 standard functions

In this section, 13 standard functions are implemented by gate NR and the number of required gates for each function is compared with the number of Fredkin gates for each function. Fredkin is a very useful testable gate and can produce many logic functions easily. Results are in Table 4 and show that gate NR has better performance than Fredkin gate in implementing standard functions in term of the required gate for each function. QCA layout of testable Fredkin gate is shown in Fig. 11. Comparison between Fredkin gate and the NR gate shows that the NR gate in terms of number of cell and area is better than Fredkin gate. The results are shown in Table 5.

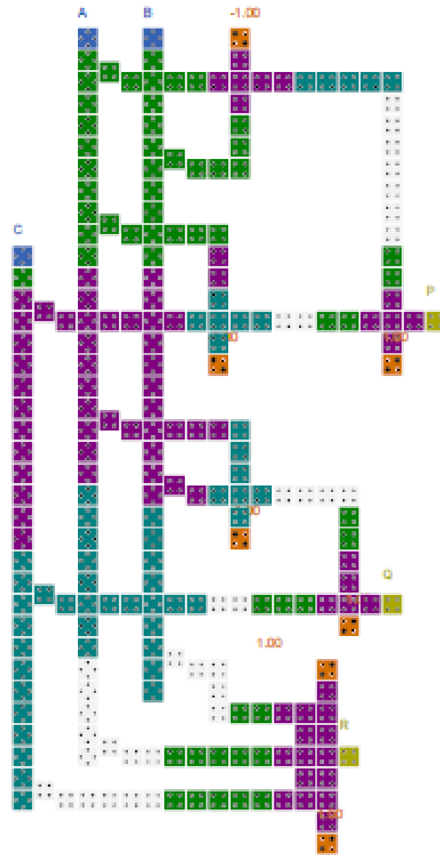

Fig. 9. Layout of gate NR in QCADesigner

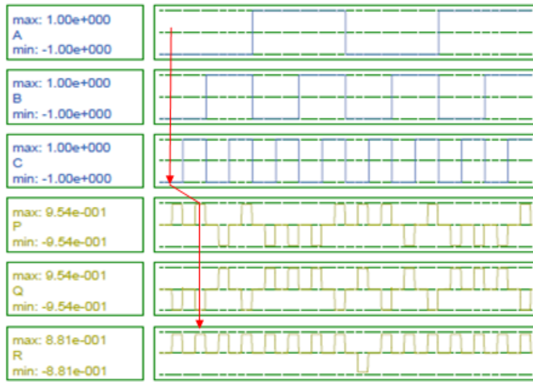

Fig. 10. Simulation results of gate NR

Table.2.
Fault patterns in gate NR

Input vector	F.F	FP1	FP2	FP3	FP4	FP5	FP6	FP7	FP8	FP9	FP10
a0	a5	a5	a5	a5	a5	a1	a5	a7	a5	a7	a7
a1	a3	a3	a3	a3	a7	a3	a7	a3	a3	a3	a3
a2	a5	a5	a5	a5	a5	a1	a5	a5	a5	a5	a7
a3	a3	a3	a7	a3	a7	a3	a7	a3	a3	a3	a3
a4	a3	a3	a3	a7	a7	a3	a3	a3	a1	a1	a3
a5	a3	a3	a3	a7	a7	a3	a3	a3	a3	a3	a3
a6	a5	a1	a5	a5	a1	a5	a5	a5	a5	a5	a5
a7	a6	a2	a6	a6	a2	a6	a6	a6	a6	a6	a6

FP11	FP12	FP12	FP13	FP14	FP15	FP16	FP17	FP18	FP19	FP20
a7	a5	a5	a5	a5	a5	a5	a5	a7	a5	a5
a3	a3	a3	a3	a3	a3	a3	a1	a3	a1	a3
a7	a5	a5	a5	a5	a5	a5	a5	a7	a5	a5
a3	a1	a3	a2	a3	a3	a3	a3	a3	a3	a3
a3	a3	a3	a3	a3	a3	a3	a3	a1	a3	a7
a3	a3	a2	a3	a3	a3	a2	a3	a3	a3	a7
a7	a7	a5	a5	a4	a5	a4	a5	a7	a5	a1
a6	a6	a6	a6	a6	a7	a6	a4	a6	a4	a2

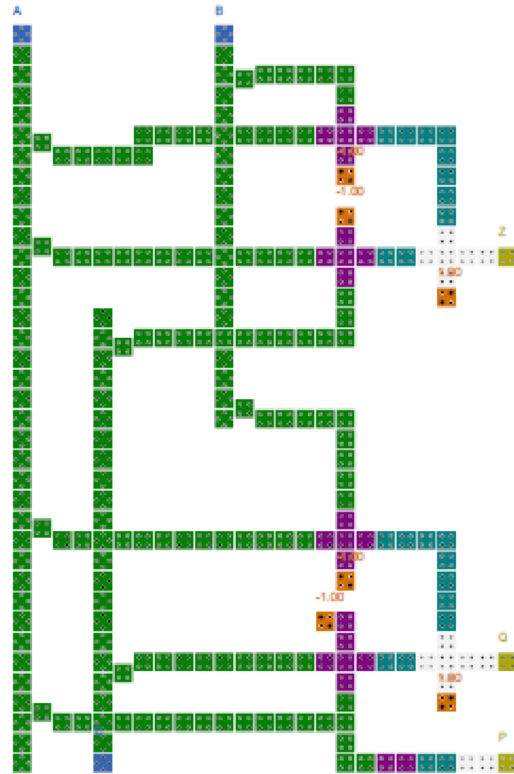

Fig. 11. Layout of testable Fredkin gate

Table.3.
Implementing 13 standard functions

Standard functions	# of NR gate	# of fredkin gate
$F_1 = A\bar{B}C$	2	2
$F_2 = AB$	1	1
$F_3 = \bar{A}BC + \overline{ABC}$	2	3
$F_4 = \bar{A}BC + A\overline{BC}$	2	4
$F_5 = \bar{A}B + B\bar{C}$	2	2
$F_6 = A\bar{B} + \bar{A}BC$	3	4
$F_7 = \bar{A}BC + AB\bar{C} + \overline{ABC}$	4	4
$F_8 = A$	1	1
$F_9 = AB + BC + AC$	3	4
$F_{10} = \bar{A}B + \bar{B}C$	2	2
$F_{11} = \bar{A}B + BC + A\overline{BC}$	2	3
$F_{12} = \bar{A}B + A\bar{B}$	2	2
$F_{13} = AB\bar{C} + \bar{A}\overline{BC} + A\bar{B}C + \bar{A}BC$	2	4

Table.4.
Comparison between Fredkin and NR gate

	Fredkin	***NR***
# cell	260	225
area (μm^2)	0.41	0.31

7. Conclusion

In this paper, a new gate is designed with special property at output by which testing is possible. This gate has two ones and one zero at the output. So the majority and logic AND of the outputs must be one and zero respectively. This method is

applicable to detect both transient and permanent faults. The ability of this gate was investigated by implementing 13 standard functions, which showed that this gate has better performance in comparison with Fredkin gates.

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