Performance Analysis of InAs/AlGaSb Heterojunction Electron-Hole Bilayer Tunnel Field Effect Transistor for Low-Power High-Speed Digital Computing

Zahra Ahangari

Department of Electronic, Yadegar- e- Imam Khomeini (RAH) Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.
z.ahangari@gmail.com

Abstract

In this paper, a novel device, namely heterojunction electron-hole bilayer tunnel field effect transistor (HJ-EHBTFET), is proposed which outperforms conventional tunnel field effect transistor (TFET) in terms of electrical performance. The use of lattice matched InAs/$Al_{0.6}Ga_{0.4}Sb$ material combination results in a broken band gap configuration, making it highly suitable for high speed ultra-low applications, as it requires smaller gate bias for the onset of tunneling. The impact of critical design parameters on the device performance is comprehensively investigated. The proposed device utilizes electrical doping instead of physical doping for the creation of tunneling junction, which effectively addresses the problem of low solubility of dopants in heavily doped III-V materials. The top gate and bottom gate workfunction are critical design parameters that effectively modulated the electrically induced charges at the tunneling junction and consequently, affect the tunneling rate. In order to obtain the lowest possible transition voltage for the onset of tunneling, a variation matrix of threshold voltage variation is computed as a function of gate electrode workfunction. Through this process, a step-like behavior from off-state to on-state has been achieved, with a subthreshold swing of 3 mV/dec and on/off current ratio of 5.8×10^{12}, thereby paving the way for the design of low-power high-speed digital computing systems.

Keywords: Band to band tunneling; Electron-hole bilayer Tunnel field effect transistor; Heterojunction; Workfunction
Article history: Received 29-Jan-2020; Revised 19-Feb-2021; Accepted 02-Mar-2021, Article Type: Research paper

https://doi.org/10.30495/ijsee. 2023.1988303.1268

1. Introduction

In recent times, there has been a significant increase in the performance and density of integrated circuits (ICs) to meet the growing demands of electronic devices for computing, communication, smart phones, and other applications. Such improvements have been made possible through continuous improvements in speed, cost, and power consumption. The process of scaling the dimensions of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) as the basic building block of integrated circuits, following Moore's Law, has been instrumental in achieving these goals. Nevertheless, the scaling of MOSFET in the nanoscale regime has almost reached the fundamental physical boundaries [1-4]. The underlying principle of the conventional MOSFET operation is predicated upon the manipulation of a gate-modulated potential barrier, whereby carriers are able to diffuse beyond the said barrier at the interface of the source and channel regions. The Boltzmann limit serves as the basis for determining the minimum gate voltage required to increase the current by one order of magnitude at room temperature in a conventional MOSFET. This value is established to be at least 60 mV. To address this limitation, the Tunnel Field Effect Transistor (TFET) has emerged as a potential alternative to the conventional MOSFET. Fundamentally, a conventional TFET operates as a gated p-i-n reverse biased diode, wherein carriers tunnel from source to channel through the band to band tunneling process. This device exhibits the characteristics of an efficient electronic switch with a subthreshold swing of less than 60 mV/dec [5-8]. In principle, it can be posited that band to band tunneling, as the primary current transport mechanism of tunnel FET, results in low on-state current. This, in turn, restricts the device performance, particularly with respect to

competitive electrical features when compared to ITRS requirements. One of the primary factors that contributes to the reduction of the BTBT current is the limited tunneling area at the interface of the source and channel. The introduction of the electron-hole bilayer TFET presents a potential alternative to the conventional TFET, with the capability to effectively enhance the tunneling current. This is achieved through the extension of the tunneling window along the channel thickness in the intrinsic channel. The creation of the bias induced p^+-n^+ tunneling region is facilitated by the polarity of the top and bottom gates. Ionescu et.al proposed an initial device structure, in which the biases of the top (V_{TG}) and bottom gate (V_{BG}) differ [9-12]. In the off-state, the bottom gate voltage leads to the accumulation of charges in the bottom layer of the channel. Nonetheless, since the tunneling junction with opposite charges is not formed in the channel, the tunneling barrier width is not sufficiently narrow for the onset of tunneling. Nevertheless, through the implementation of opposite bias to the top gate (with respect to the polarity of the bottom gate), carriers of opposite charges accumulate in the uppermost layer of the channel. Upon elevating the voltage of the top gate beyond a necessary magnitude, vertical band-to-band tunneling arises throughout the thickness of the channel. It should be mentioned that applying different bias to the top and bottom gate is challenging.

In this paper, we examine the electrical properties of a p-type heterojunction electron-hole bilayer that exhibits significant improvements in on-state current through material and structural engineering. The proposed configuration eliminates the bottom gate bias and utilizes distinct materials with varying work functions in the top and bottom gate electrodes. Essentially, due to the disparity in work function between the bottom gate electrode and the channel, electrons accumulate in the lower layer of the channel. By applying an appropriate bias to the top gate, a steep p^+-n^+ tunneling junction is established along the channel thickness, resulting in vertical band-to-band tunneling along the channel depth. The selection of the appropriate material for the bottom gate electrode is critical. Furthermore, it can be defined that band to band tunneling occurs when there is alignment between the electronic energy bands at the tunneling junction. It is apparent that the band alignment configuration can be altered by the materials present in the source, channel, and drain regions [13-15]. This research paper introduces the use of an InAs/$Al_{0.6}Ga_{0.4}Sb$ heterojunction, which provides a broken band gap configuration. The proposed materials have a limited lattice mismatch that significantly reduces interface traps and defects. The impact of critical design parameters on device performance is thoroughly investigated, and the optimal design parameters for efficient device performance are determined.

The present manuscript is structured in the following manner: in section two, a comprehensive explication of the device structure and simulation models is meticulously presented. The performance of the device is exhaustively evaluated with respect to critical design parameters. Ultimately, the paper is summarized in the concluding section.

2. Device structure and simulation models

The proposed heterojunction electron hole bilayer TFET (HJ-EHBTFET), whose schematic is presented in Fig.1, possesses an n-i-p doping profile extending from the source to the drain. The InAs material constitutes the source region and channel bottom layer, whereas the top layer channel and drain region are composed of $Al_{0.6}Ga_{0.4}Sb$. The InAs/$Al_{0.6}Ga_{0.4}Sb$ heterojunction features a negligible lattice mismatch and a small carrier effective mass, thereby enhancing the tunneling rate. The pertinent device parameters for the HJ-EHBTFET and conventional heterojunction TFET are presented in Table. 1. To evaluate the electrical characteristics of the device, numerical simulations are conducted through the ATLAS device simulator [16], and the following models are activated:

Nonlocal Band to Band Tunneling: The present study considers a nonlocal band to band tunneling model for the computation of tunneling current from the conduction band minima of the bottom layer channel to the valence band maxima of the top layer.

Bandgap Narrowing: The tunneling rate, a crucial parameter, may be significantly influenced by the band gap energy. To evaluate the bandgap shrinkage in regions with high impurity density and additional impurity sates due to the overlap of multiple dopant states, the band gap narrowing model is activated.

Quantum Confinement Models: In the proposed device, the tunneling junction is established in a quantum well structure that is formed along the channel thickness. It is noteworthy that the energy of sub-band may increase while scaling the channel thickness, which in turn may modify the density of states. Therefore, models considering quantum confinement effects are employed to address this phenomenon.

Mobility Models: The activation of mobility models that consider the impact of high electric field and doping density on carrier velocity has been initiated.

Generation/Recombination Models: In order to compute the excessive tunneling current that arises

from the presence of traps and defects, the Shockley-Read-Hall (SRH), Auger recombination model, and trap assisted tunneling models are assumed.

Table.1.
Initial physical and structural design parameters for HJ-EHBTFET and conventional TFET.

Parameter	*HJ-EHB TFET*	*Conventional TFET*
Channel length (nm)-L_{ch}	150	150
Gate overlap length (nm)-L_{ov}	50	50
Channel thickness (nm)-T_{ch}	10	10
Top-gate workfunction	4.9	4.9
Bottom-gate workfunction	4.5	4.9
Source doping conc. (cm^{-3})	5×10^{18}	5×10^{18}
Channel doping conc.(cm^{-3})	intrinsic	intrinsic
Drain doping conc.(cm^{-3})	5×10^{18}	5×10^{18}
Gate oxide thickness (nm)- HfO_2	1	1
Drain Bias (V)- V_{DS}	1	1

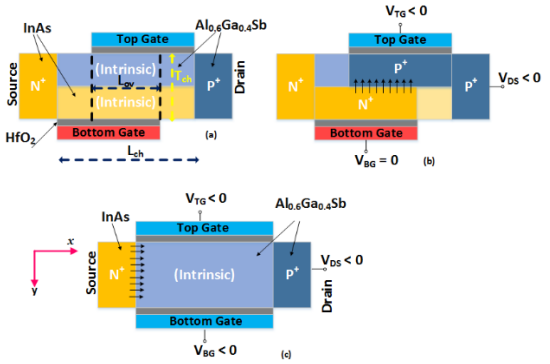

Fig. 1. (a) Schematic of a double gate HJ-EHBTFET with n-i-p doping profile. (b) on-state operation of HJ-EHBTFET in which BTBT occurs along the channel length in the vertical direction. (c) on-state operation of conventional TFET with horizontal BTBT from source into the channel.

3. Results and Discussions

The creation of a steep p^+-n^+ tunneling junction is a crucial element for the manifestation of band to band tunneling, as well as to attain a step-like behavior in the transfer characteristics. The proposed HJ-EHBTFET exploits the carrier vertical line tunneling through an electrically doped electron–hole bilayer in order to achieve improved switching speed and higher drive current when compared to a conventional lateral p–i–n junction TFET. Figure 2(a) visually depicts the concentration of electrons and holes in the channel thickness during the off and on states. In the off-state, when the top gate bias is absent (V_{TG}=0V, V_{DS}=1V), electrons accumulate in the lower layer channel owing to the disparity in work function between the underlying channel and the bottom gate electrode. The density of holes within the channel is heavily contingent upon the top gate bias, particularly in the upper layer of the channel. It is evident that during the off-state, the density of holes decreases. However, a significant increase in hole density is anticipated as the top gate bias progresses towards a sufficiently negative value. Figure 2(b) depicts the energy band diagram of the device in the tunneling direction during both the off and on states. It is observed that the tunneling window is extended along the channel thickness. During the off-state, the width of the barrier is insufficiently thin for the onset of band-to-band tunneling. Nevertheless, as the top gate bias exceeds the transition voltage, the tunneling barrier becomes adequately thin for the carriers to tunnel through, vertically. The subthreshold swing (SS) in HJ-EHBTFET can be approximately defined as:

$$SS \approx \frac{\ln(10)}{q}\Delta\varphi = \frac{\ln(10)}{q}(E_C^{bottom\ layer} - E_V^{top\ layer}) \quad (1)$$

in which q is the basic electric charge, $\Delta\varphi$ is defined as the energy difference between conduction band minima of the InAs bottom layer, $E_C^{bottom\ layer}$ and valence band maxima of the Al0.6Ga0.4Sb top layer, $E_V^{top\ layer}$. Essentially, when the upper gate bias is elevated to an adequate negative level, the width of the tunneling barrier, denoted as $\Delta\varphi$, is fundamentally diminished. This phenomenon is indicative of the onset of tunneling and a significant decrease in the subthreshold swing.

The transfer characteristics of both the HJ-EHBTFET and the conventional TFET can be seen in Fig. 3. The obtained results illustrate a noteworthy improvement of approximately 5.5 times in the on-state current of the HJ-EHBTFET when compared to the conventional TFET device. This improvement stems from the line-tunneling phenomena present in the proposed structure. Additionally, the HJ-EHBTFET structure exhibits a remarkably low off-state leakage current and an on/off current ratio of 5.8×10^{12}. Furthermore, the electrically induced tunneling junction in the EHBTFET leads to an enhanced transition behavior from the off-state to the maximum drive current with a subthreshold swing of 3mV/dec and a low threshold voltage. In contrast, the lateral n-i-p TFET yields a subthreshold swing of 10mV/dec with a higher threshold voltage.

The threshold voltage is a crucial parameter in the study of electronic devices. It is regarded as the value of the top gate voltage that initiates the transition of the drain current from its lowest possible off-state current to higher values. This can be interpreted as the minimum top gate bias necessary for the onset of tunneling in the device. Figure.4 displays the transfer characteristics of HJ-EHBTFET while the drain voltage is varied from V_{DS}=0.05 V to V_{DS}=1V. It is evident that the off-

state current and threshold voltage remain unaffected by the drain voltage variation, which highlights the device's exceptional resistance to short channel effects such as Drain Induced Source Tunneling (DIST). As the drain bias approaches its maximum value, the on-state current increases due to the carrier drift velocity enhancement.

The impact of the workfunction of the bottom gate on the current of band-to-band tunneling is assessed by means of calculating the transfer characteristics of HJ-EHBTFET, depicted in Fig.5. The bottom gate workfunction is parameterized from WF_{BG}=4.3eV to 4.9eV. It should be noted that the top gate workfunction value remains constant at WF_{TG}=4.9eV.

The variation of the bottom gate workfunction modulates the electrically induced electrons in the bottom layer, which in turn affects the width of the tunneling barrier. It is evident that the decrease in WF_{BG} value results in an increase in electron density, thereby pushing the threshold voltage towards positive values. However, the increase in the amount of electrons induced by the bottom gate coupling over the channel, deteriorates the subthreshold swing of the device. Furthermore, the augmentation of the difference in workfunction between the bottom gate and the channel provides higher negative top gate voltages for the onset of carrier tunneling.

The determination of the top gate workfunction value is a significant design parameter that may affect the device performance. This parameter has a direct effect on the gate electric field coupling over the channel, which in turn can modulate the width of the tunneling barrier. The transfer characteristics of the device are depicted in Fig.6, while maintaining a constant bottom gate workfunction. The threshold voltage of HJ-EHBTFET is evidently reliant on the band bending in the tunneling region and has a strong correlation with the electrically induced charge density in the p^+-n^+ junction. Evidently, an increase in the top gate workfunction leads to an increment in the hole density in the top layer channel, thereby reducing the threshold voltage and influencing the transition voltage towards positive values.

The workfunction of the top and bottom gates are crucial design parameters that possess the potential to significantly influence the carrier density. Consequently, they can effectively modulate the tunneling rate. A 2D variation contour map depicting the threshold voltage has been computed to adjust the initiation of carrier tunneling through gate work function engineering, as illustrated in Fig. 7.

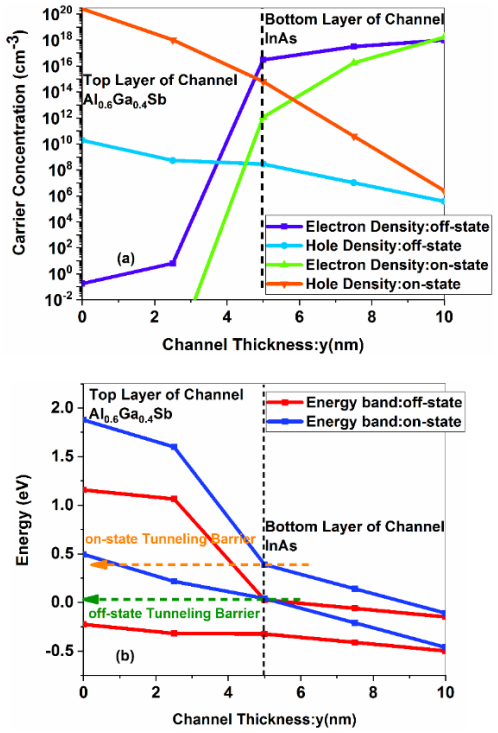

Fig. 2. (a) Carrier density along the channel thickness, and (b) Energy band diagram from the channel bottom layer to the top layer of the channel in the off-state and on-state.

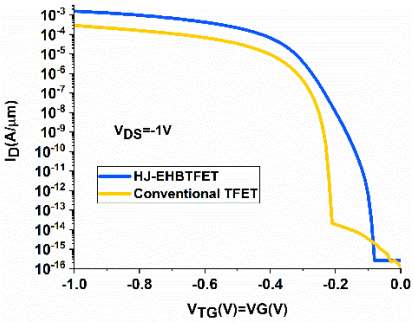

Fig. 3. Transfer characteristics of HJ-EHBTFET and conventional TFET, VDS=1V.

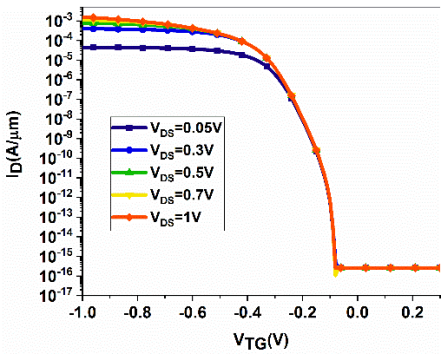

Fig. 4. ID-VTG curves of HJ-EHBTFET as a function of drain bias.

The threshold voltage's maximum negative value is visibly observed in the top-left corner of the variation matrix. This phenomenon occurs due to the

workfunction value of the top and bottom gate materials inducing a wide tunneling barrier. On the other hand, the onset of carrier tunneling shifts towards positive values, resulting in the maximum positive threshold voltage appearing in the bottom-right corner of the contour. In this area, the related values of gate workfunction increase the electrically induced carrier density in the top and bottom layer of the channel. The accumulation of charge carriers at the tunneling junction provides barrier width narrowing even at zero top gate bias. For low power efficient p-type operation of the device, the lowest possible negative value of top gate bias (absolute value) is required. This can be achieved by the proper combination of top and bottom gate workfunction, mainly in the central part of the variation contour.

The output characteristics of the HJ-EHBTFET have been calculated and depicted in Fig.8, both in linear and logarithmic scale as the top gate voltage is varied from V_{TG}= -0.3V to -1V . A distinct and significant increase in the drain current is observed as the gate voltage increases beyond the transition voltage, indicating a change in the channel conductance in relation to the gate voltage. It is a well-established fact that the gate voltage has the ability to modify the induced hole density in the top layer channel and alter the band to band tunneling rate.

Source doping serves as a critical design measure in conventional TFETs as it can effectively modulate the tunneling barrier at the interface of the source and channel regions. However, simulation results (not depicted) reveal that the performance of the heterojunction electrically biased tunnel field-effect transistor (HJ-EHBTFET) is highly insensitive to the source doping density as the tunneling junction is created electrically within the channel thickness. The proposed structure's main advantage with electrical doping is that III-V materials have a low solubility of dopants, and the formation of thin film heavily doped regions in these materials is experimentally challenging.

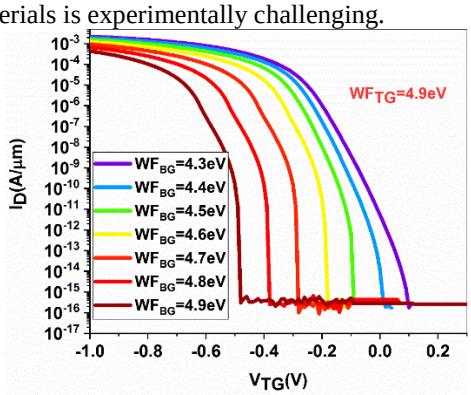

Fig. 5. Transfer characteristics of HJ-EHBTFET, considering the effect of bottom gate workfunction on device performance. The top gate workfunction value is constant at WFTG=4.9eV.

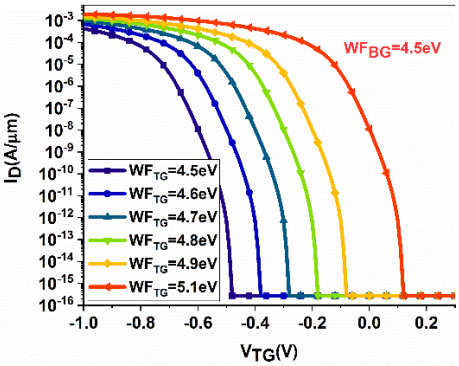

Fig. 6. The effect of top gate workfunction variation on the electrical characteristics of HJ-EHBTFET. The bottom gate workfunction value is constant at WFBG=4.5 eV.

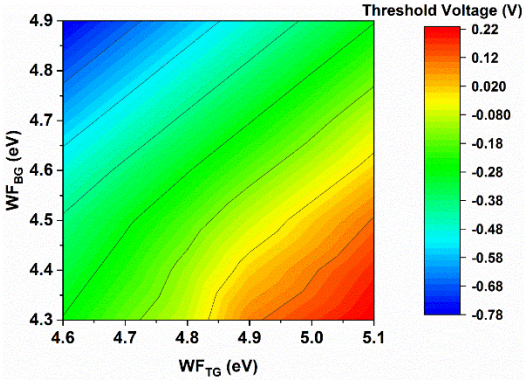

Fig. 7. 2D variation contour of threshold voltage versus top and bottom gate workfunction values.

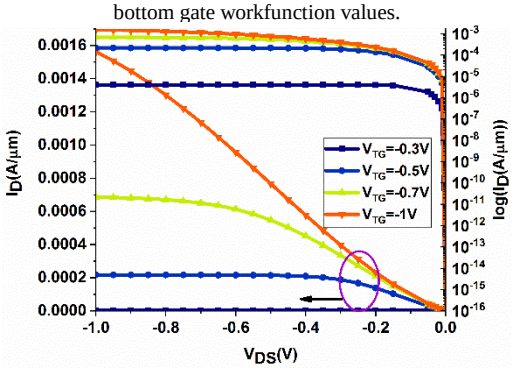

Fig. 8. Output characteristics of the HJ-EHBTFET for different top gate voltage values.

4. Conclusion

In this paper, a thorough investigation is carried out to examine the electrical characteristics of a broken band gap heterojunction electron-hole bilayer TFET. In contrast to the conventional TFET, where the band to band tunneling current is primarily controlled by the point tunneling in a narrow area at the interface of the source and channel region, the tunneling current in the proposed device is significantly enhanced by expanding the band to band generation area that is governed by line tunneling mechanism. The HJ-EHBTFET device exhibits improved performance in comparison to the conventional TFET device. The findings of the study indicate that the workfunction of both the top

and bottom gate electrodes can effectively alter the electrically induced charges of the tunneling junction, thus impacting the necessary voltage for the onset of tunneling. As such, it is imperative to determine the optimal value for these electrodes. Furthermore, due to the specific design of the proposed device, the tunneling rate remains unaffected by the drain electric field, resulting in a high immunity towards short channel effects. This research on electrically doped TFET resolves the challenge of low dopant solubility in nanoscale III-V devices and paves the way for the development of low-power, high-speed digital circuits.

References

[1] Khanna, Vinod Kumar, and Vinod Kumar Khanna. "Short-channel effects in MOSFETs." Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies (2016): 73-93.

[2] Pandey, Nilesh, Huang-Hsuan Lin, Ashutosh Nandi, and Yuan Taur. "Modeling of short-channel effects in DG MOSFETs: Green's function method versus scale length model." IEEE Transactions on Electron Devices 65, no. 8 (2018): 3112-3119.

[3] Avci, Uygar E., Daniel H. Morris, and Ian A. Young. "Tunnel field-effect transistors: Prospects and challenges." IEEE Journal of the Electron Devices Society 3, no. 3 (2015): 88-95.

[4] Navi, Keivan, Neda Ghoreishi, Reza Sabbaghi-Nadooshan, and Mohammad Esmaeildoust. "Design of Multiple-Valued Interconnection Networks with Gate all Around Transistor for Smart Computer Networks." International Journal of Smart Electrical Engineering 12, no. 01 (2023): 11-21.

[5] Nazir, Ghazanfar, Adeela Rehman, and Soo-Jin Park. "Energy-efficient tunneling field-effect transistors for low-power device applications: challenges and opportunities." ACS Applied Materials & Interfaces 12, no. 42 (2020): 47127-47163.

[6] Badgujjar, Soniya, Girish Wadhwa, Shailendra Singh, and Balwinder Raj. "Design and analysis of dual source vertical tunnel field effect transistor for high performance." Transactions on Electrical and Electronic Materials 21 (2020): 74-82.

[7] Nakamura, Keigo, Naoka Nagamura, Keiji Ueno, Takashi Taniguchi, Kenji Watanabe, and Kosuke Nagashio. "All 2D heterostructure tunnel field-effect transistors: impact of band alignment and heterointerface quality." ACS Applied Materials & Interfaces 12, no. 46 (2020): 51598-51606.

[8] Tamersit, Khalil, Abdellah Kouzou, Hocine Bourouba, Ralph Kennel, and Mohamed Abdelrahem. "Synergy of electrostatic and chemical doping to improve the performance of junctionless carbon nanotube tunneling field-effect transistors: Ultrascaling, energy-efficiency, and high switching performance." Nanomaterials 12, no. 3 (2022): 462.

[9] Lattanzio, Livio, Luca De Michielis, and Adrian M. Ionescu. "The electron–hole bilayer tunnel FET." Solid-State Electronics 74 (2012): 85-90.

[10] Alper, Cem, Livio Lattanzio, Luca De Michielis, Pierpaolo Palestri, Luca Selmi, and Adrian Mihai Ionescu. "Quantum mechanical study of the germanium electron–hole bilayer tunnel FET." IEEE transactions on electron devices 60, no. 9 (2013): 2754-2760.

[11] Liu, Hu, Wenting Zhang, Zaixing Wang, Yao Li, and Huawei Zhang. "OFF-State Leakage Suppression in Vertical Electron–Hole Bilayer TFET Using Dual-Metal Left-Gate and N+-Pocket." Materials 15, no. 19 (2022): 6924.

[12] Wang, Xueke, Yabin Sun, Ziyu Liu, Yun Liu, Xiaojin Li, and Yanling Shi. "Design optimization of nanotube tunnel field-effect transistor with bias-induced electron-hole bilayer." Silicon 14, no. 14 (2022): 9071-9082.

[13] Chen, Chin-Yi, Hesameddin Ilatikhameneh, Jun Z. Huang, Gerhard Klimeck, and Michael Povolotskyi. "Impact of body thickness and scattering on III–V triple heterojunction TFET modeled with atomistic mode-space approximation." IEEE Transactions on Electron Devices 67, no. 8 (2020): 3478-3485.

[14] Pindoo, Irfan Ahmad, Sanjeet Kumar Sinha, and Sweta Chander. "Performance analysis of heterojunction tunnel FET device with variable temperature." Applied Physics A 127 (2021): 1-10.

[15] Chen, Shupeng, Shulong Wang, Hongxia Liu, Tao Han, and Hao Zhang. "A high performance trench gate tunneling field effect transistor based on quasi-broken gap energy band alignment heterojunction." Nanotechnology 33, no. 22 (2022): 225205.

[16] ATLAS User Manual, Santa Clara, USA: Silvaco International, (2015).