Design and Implementation of Tile-shaped Fault-tolerant XOR/XNOR Gates Based on Intercellular Interactions

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Abstract

Over the years, the design and implementation of fault-tolerant circuits have been one of the main concerns of the designers of electronic devices. Quantum Dot Cellular Automata (QCA) is a low-power, compact technology that is prone to various defects due to its small size. We can categorize these defects into three main groups: operational defects, manufacturing defects, and clocking defects. Using redundant cells, fault-tolerant gates, or changing the structure of the gates can improve the overall fault-tolerance of the circuit in some cases. However, increasing the fault-tolerance would lead to an increase in the occupied area and the delay of the gates. Therefore, designing a gate based on intercellular interactions with a minimum number of cells and maximum efficiency, which is also fault-tolerant, is a challenging task. In this paper, we present a new tile-shaped design for XOR and XNOR gates that is robust to the Missing cell, Extra cell, and Rotated cell defects by 25%, 55%, and 25%, respectively. That is why we call these gates TFXOR and TFXNOR, respectively.

Keywords: Quantum-dot Cellular Automata, Fault-tolerant XOR gate, Fault-tolerant XNOR gate, Tile-shaped Fault-tolerant XOR, Tile-shaped Fault-tolerant XNOR
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1. Introduction

CMOS technology has been used in the manufacturing of integrated circuits for years. The transistors used in this technology has become smaller and smaller to provide faster circuits with less power consumption. However, these micro-scale transistors have created new challenges such as small current behaviors, quantum effects, design complications, and power consumption, which has stunted the development and advancement of microelectronic technology.

However, there have been numerous efforts to develop an applicable technology that can be used in the design and implementation of nano-scale low-power circuits. Quantum-dot Cellular Automata (QCA) is one of the emerging technologies that was first introduced by Lent et. al. in 1993 [1]. In QCA, an electronic circuit is divided into cells, and the binary data is stored as the electric charge of the cell. The rules governing a QCA mean that the state of a cell is affected by its adjacent cells, and the intercellular coulombic forces would cause the flow of information. In QCA, the basic gates are used in the implementation of more complex circuits. To increase the reliability of extended circuits, one must increase the reliability of their components so that even if there are some defects, the circuit can produce the correct output. Increasing the fault-tolerance of a circuit requires all its components to be fault-tolerant. Therefore, we decided to design a fault-tolerant XOR/XNOR gate.

In the rest of this paper, we first review the basic related concepts in section 2. In section 3, we discuss the reliability of QCA circuits. The previous designs of XOR and XNOR gates are discussed in section 4, and the proposed fault-tolerant TFXOR and TFXNOR gates are presented in section 5. Finally, the results are provided and compared in section 6, and the conclusion is presented in section 7.

2. The Basic Concepts

A common QCA cell consists of four quantum-dots and two electrons. The dots are located at the corners of a square-shaped cell, and the two

electrons can move between these dots. The most stable state of a cell occurs when the electrons are positioned at the furthest points to one another. In other words, on the diagonals of the square [1], [2]. Thus, a cell has two stable states with polarization P = -1 (logic 0) and P = +1 (logic 1) [1]. Figure 1 and Figure 2 show a cell in standard configuration and with 45°rotation, respectively.

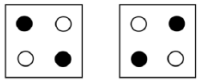


Fig. 1. Position of electrons in a 90° cell in a) P = -1 (logic 0), and b) P = +1 (logic 1).

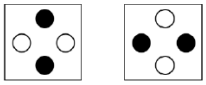


Fig. 2. Position of electrons in a 45° cell in a) P = -1 (logic 0), and b) P = +1 (logic 1).

A) wire

According to the definition of cell-to-cell response, a cell can be affected by the polarization of its neighboring cells. The interaction between the cells causes the information to be transferred from one cell to the next. It means that one can arrange cells into a row to create a wire [1]. In general, there are two types of wiring. In the first method, the standard cells are used to create the wire, and the input information itself is transferred to the output. In the second method, 45° rotated cells are used to create the wire, and one can transfer the input or its inverted value to the output by using an even or odd number of cells [3].

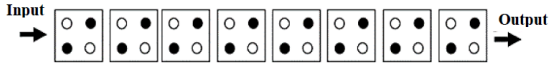


Fig. 3. A QCA binary wire with 90° cells.

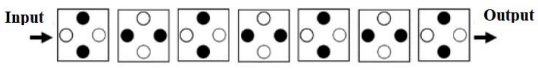


Fig. 4. A QCA inverted chain with 45° cells.

B) Basic logical elements

All QCA circuits can be implemented using majority gates and inverters [4]. We will discuss these two gates in the following sub-sections.

– *Majority Gate*

The majority gate is one of the most fundamental gates in QCA circuits. The output of this gate is determined based on the majority voting on the polarization of the inputs and it can be used to implement the AND and OR logical operators [1], [2], [4].

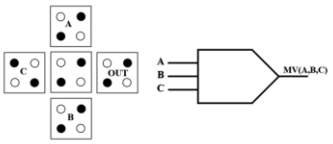


Fig. 5. The architecture of a majority gate with three inputs in QCA.

– *Inverter*

Another useful QCA gate is the inverter [1]. There are various methods with different designs, occupied areas, and reliability levels for the implementation of the inverter gates [5]. A standard inverter gate is presented in Figure 6 [1].

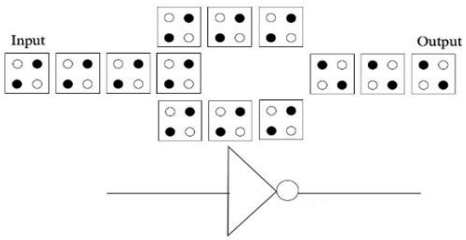


Fig. 6. A standard inverter gate [1].

C) Clock

In QCA, the clock has a significant role in the movements of electrons. It is generated by an electrical field and can increase or decrease the potential barrier between the dots. The clock in QCA has four phases: switch, hold, release, and relax [6]. In the switch phase, the ascending edge of the clock signal, the coulombic forces of the neighboring cells would cause the electrons to transfer to their stable states, which forces the cell to take a specific value. In the hold phase, when the clock signal has the highest value, the QCA cell would maintain its current state. In the release phase, the descending edge of the clock, the tunneling of electrons occurs due to the attraction of the clock plane. When the clock is at its lowest value, the relaxing phase of the clock, the cell would completely lose its polarization and would be in a neutral state. There are two proposed clocking design for QCA circuits: Landauer [6] and Bennett [6]. In QCADesigner software, four different clock signals are defined, which have a 90° phase difference with one another.

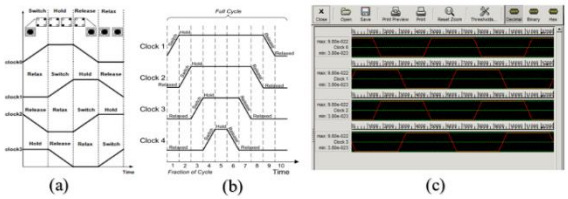


Fig. 7. A typical clock signal that is usually used in QCA circuits a) Landauer clocking waveform [6] b) Bennett clocking waveform [6] c) clocking wave form in QCADesigner[6].

D) Kink Energy

In order to obtain the optimal value for parameters such as quantum dot dimensions, dot spacing, cell spacing, and cell dimensions, in the construction of QCA circuits, kink energy is used; This energy is expended for cells i and j as polarized, and is obtained through eq 1. Values of ε_0 and ε_r are the vacuum permittivity and the relative permittivity, respectively. Kink energy is calculated from the difference in electrostatic energy between the opposite and similar polarization of cells [7].

$$E_{i.j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\frac{q_i q_j}{|r_i - r_j|} \quad (1)$$

E) QCA Designer

In order to simulate QCA circuits, we must implement and design a series of basic factors and functions. This was achieved by QCA Designer version 2.0.3. As shown in Figure 4, all values are applied using the default parameters and the Bistable simulation model.

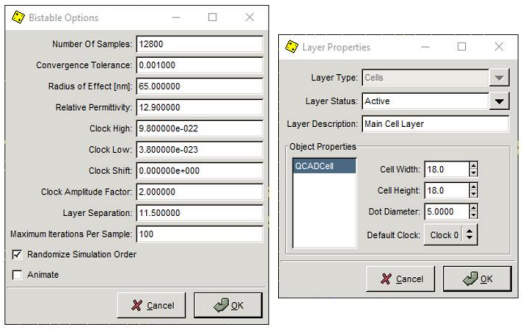


Fig. 8. Default parameters in QCA Designer

3. Reliability in QCA circuits

Every system encounters some form of fault, and they would inevitably affect the systems and their outputs. Therefore, it is imperative to create a system that is fault-tolerant and reliable. In QCA circuits, this is especially important because of their small size and increased sensitivity. Numerous research works have studied the various types of errors and defects of QCA circuits [8-14]. Figure 9 shows a summary of these defects. Also, different solutions have been proposed to increase the fault-tolerance of these circuits. Some of these solutions include using redundant cells or fault-tolerant gates. Another proposed solution is ensuring that at least three cells are present in each clock region [13]-[17] Fault injection method in QCADesigner was used in order to simulate and evaluate the tolerance of QCA circuits against cell omission and cell addition defects in a gate which will be studied in the following.

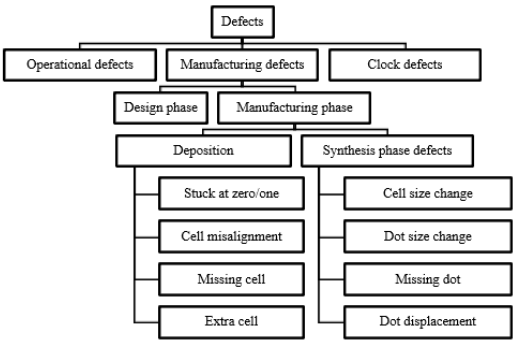


Fig. 9. Categorizing different defect types in QCA circuits.

A) Missing Cell

If for some reason a cell was missing, the neighboring cells cannot have their ideal performance, and the lack of effect on these cells, which is due to the missing cell, is not negligible. If the normal distance of the cells is relatively high, the circuit cannot work properly with a missing cell [18].

B) Rotated Cell

This defect is due to the rotation of the quantum cell with respect to other cells in the array [18].

C) Extra Cell

This defect occurs when an extra cell is placed next to the original cells of the gate on the bed by mistake [19]. Figure 10 shows a schematic diagram of the missing cell, rotated cell, and extra cell defects in a majority gate

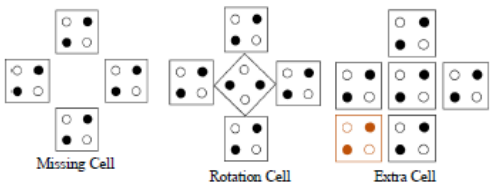
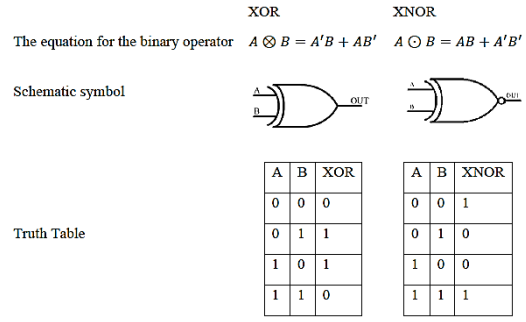


Fig. 10. A schematic diagram of the missing cell, rotated cell, and extra cell defects in a majority gate

4. XOR and XNOR gates

The exclusive OR and exclusive NOR gates are used in conjunction with other gates like AND,

OR, NAND, and NOR to design and implement various integrated circuits such as adders, comparators, Gray code decoders, as well as even and odd parity generators, and many more circuits. These two gates count the number of 1s in the input and generate the appropriate output. In the XOR gate, if the number of 1s in the input is odd, the output would be 1. Therefore, XOR is an odd function, while XNOR is an even function. Figure 11 shows the equations, schematic symbols, and truth tables of the binary XOR and XNOR gates.



A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

A	B	XNOR
0	0	1
0	1	0
1	0	0
1	1	1

Fig. 11. An overview of XOR and XNOR gates.

A) The previous designs

The first XOR gate using QCA technology was designed and implemented in 1993 [1]. It was based on Boolean functions, and the majority voting and inverter gates were used in its design. However, using such gates in extended and more complex structures would increase the delay and area of the integrated circuit. Therefore, it is preferred to use gates that are based on intercellular interactions rather than Boolean functions. Such a design not only reduces the complexity of the design but also provides a more efficient structure with fewer cells and minimum delay for use in an extended circuit. The design of such gates is discussed in [20]-[25]. Figure 12 shows several examples of such designs.

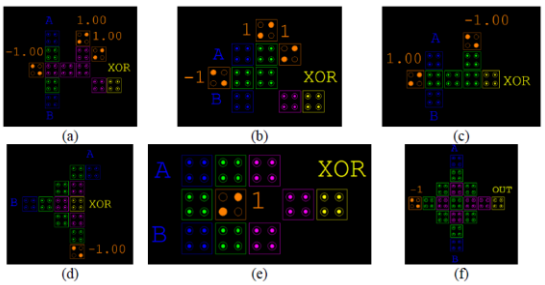


Fig. 12. The XOR gates designed based on intercellular interactions. (a) introduced in [20], (b) introduced in [21], (c) introduced in [22], and (d) introduced in [23], (e) introduced in [24], (f) introduced in [25].

B) The proposed TFXOR and TFXNOR gates

As discussed above, the QCA circuits are very sensitive to defects. Therefore, designing fault-tolerant gates is imperative for the success of this technology. In exclusive gates designed based on intercellular interactions, the fewer number of cells and configuration of the cells can lead to significant errors and defects. That is why designing fault-tolerant exclusive gates based on intercellular interactions is very important. The proposed fully tiled XOR/XNOR gates, which are called TFXOR / TFXNOR in the remainder of this paper, have a fully tiled structure, work based on intercellular interactions, and are robust to some defects. The proposed gate consists of a 3 × 3 tile and 12 cells, and its occupied area is 0.02 μm^2. The delay of this gate is half a clock cycle, and one of its main advantages is the flexibility of its output cell. The simple schematic diagram and Physical verification for the output of TFXNOR gate are shown in Figure 13 and Table 1.

Comparison of results revealed that the output cell electrons are positioned in Figure 13 (a) has lower kink energy which is more stable and. Thus, the output cell polarity is equal to '0' and it had been obtained correctly. this process repeated for all inputs' state.

Also, the schematic diagram and simulation results of TFXOR and TFXNOR gates in QCADesigner are shown in Figure 14.

C) Comparing the Results

As stated before, the gates that work based on intercellular interactions are very sensitive to defects. Therefore, presenting a fault-tolerant gate that is also structurally simple can significantly increase the reliability of more extensive and complex circuits. The simulation results indicate that our proposed gates are robust to the missing cell, rotated cell, and extra cell defects by 25%, 25%, and 55%, respectively. Table 2 compares the structural properties of the proposed gate with those of the six gates shown in Figure 12. Also, the tolerance of the gates against the extra cell, rotated cell, and missing cell defects are shown in Figure 15.

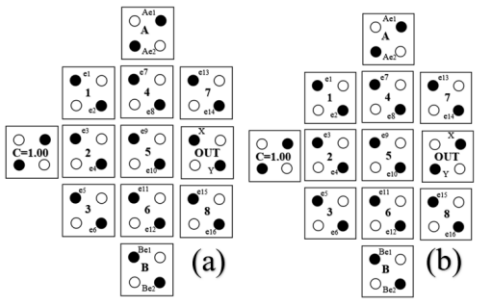


Fig. 13. TFXNOR gate with AB=10 a) if out=0, b) if out=1

Table.1.
Physical verification for the output cell in Figure 13

Electron	State (a)		State (b)	
	Applied Kink energy to ex	Applied Kink energy to ey	Applied Kink energy to ex	Applied Kink energy to ey
e3	$\frac{2.03\times10-29}{40\times10^{-9}}$ =5.075E-22	$\frac{2.03\times10-29}{60.72\times10^{-9}}$ =3.3432E-22	$\frac{2.03\times10-29}{40\times10^{-9}}$ = 3.5E-22	$\frac{2.03\times10-29}{43.86\times10^{-9}}$ = 4.62E-22
e4	$\frac{2.03\times10-29}{28.42\times10^{-9}}$ =7.1428E-22	$\frac{2.03\times10-29}{40\times10^{-9}}$ =5.075E-22	$\frac{2.03\times10-29}{43.86\times10^{-9}}$ = 4.62E-22	$\frac{2.03\times10-29}{22\times10^{-9}}$ = 9.22E-22
e7	$\frac{2.03\times10-29}{28.28\times10^{-9}}$ =7.1782E-22	$\frac{2.03\times10-29}{53.74\times10^{-9}}$ =3.7774E-22	$\frac{2.03\times10-29}{42.94\times10^{-9}}$ = 4.72E-22	$\frac{2.03\times10-29}{42.94\times10^{-9}}$ = 4.72E-22
e8	$\frac{2.03\times10-29}{2.82\times10^{-9}}$ =7.1985E-21	$\frac{2.03\times10-29}{28.28\times10^{-9}}$ =7.1782E-22	$\frac{2.03\times10-29}{20.09\times10^{-9}}$ = 1.01E-21	$\frac{2.03\times10-29}{20.09\times10^{-9}}$ = 1.01E-21
e9	$\frac{2.03\times10-29}{20\times10^{-9}}$ =1.015E-21	$\frac{2.03\times10-29}{42.04\times10^{-9}}$ =4.8287E-22	$\frac{2.03\times10-29}{38\times10^{-9}}$ = 5.34E-22	$\frac{2.03\times10-29}{26.9\times10^{-9}}$ = 7.54E-22
e10	$\frac{2.03\times10-29}{18.11\times10^{-9}}$ =1.1209E-21	$\frac{2.03\times10-29}{20\times10^{-9}}$ =1.015E-21	$\frac{2.03\times10-29}{26.9\times10^{-9}}$ = 7.54E-22	$\frac{2.03\times10-29}{2\times10^{-9}}$ = 1.01E-20
e11	$\frac{2.03\times10-29}{28.28\times10^{-9}}$ =7.1782E-22	$\frac{2.03\times10-29}{38.05\times10^{-9}}$ =5.335E-22	$\frac{2.03\times10-29}{42.94\times10^{-9}}$ = 4.72E-22	$\frac{2.03\times10-29}{20.09\times10^{-9}}$ = 1.01E-21
e12	$\frac{2.03\times10-29}{40\times10^{-9}}$ =5.3350E-22	$\frac{2.03\times10-29}{28.28\times10^{-9}}$ =7.1782E-22	$\frac{2.03\times10-29}{42.94\times10^{-9}}$ = 4.72E-22	$\frac{2.03\times10-29}{20.09\times10^{-9}}$ = 1.01E-21
e13	$\frac{2.03\times10-29}{20\times10^{-9}}$ =1.015E-21	$\frac{2.03\times10-29}{42.04\times10^{-9}}$ =4.8287E-22	$\frac{2.03\times10-29}{26.9\times10^{-9}}$ = 7.54E-22	$\frac{2.03\times10-29}{38\times10^{-9}}$ = 5.34E-22
e14	$\frac{2.03\times10-29}{18.11\times10^{-9}}$ =1.12093E-21	$\frac{2.03\times10-29}{20\times10^{-9}}$ =1.015E-21	$\frac{2.03\times10-29}{2\times10^{-9}}$ = 1.01E-20	$\frac{2.03\times10-29}{26.9\times10^{-9}}$ = 7.54E-22
e15	$\frac{2.03\times10-29}{20\times10^{-9}}$ =1.015E-21	$\frac{2.03\times10-29}{18.11\times10^{-9}}$ =1.1209E-21	$\frac{2.03\times10-29}{26.9\times10^{-9}}$ = 7.54E-22	$\frac{2.03\times10-29}{2\times10^{-9}}$ = 1.01E-20
e16	$\frac{2.03\times10-29}{42.04\times10^{-9}}$ =4.82873E-22	$\frac{2.03\times10-29}{20\times10^{-9}}$ =1.015E-21	$\frac{2.03\times10-29}{38\times10^{-9}}$ = 5.34E-22	$\frac{2.03\times10-29}{26.9\times10^{-9}}$ = 7.54E-22
	U_{TX} = $\sum_{i=1}^{12} U_i$=1.6E-20	U_{TY} = $\sum_{i=1}^{12} U_i$=8.3E-21	U_{TX} = $\sum_{i=1}^{12} U_i$=1.6E-20	U_{TY} = $\sum_{i=1}^{12} U_i$=2.7E-20
	$U_T=U_{TX}+U_{TY}$ =2.4E-20 J		$U_T=U_{TX}+U_{TY}$ =4.4E-20 J	

Table.2.
Comparing the structural properties of the proposed gate with those of the gates presented in [20]-[25] (shown in Figure 11)

XOR	Cell count (complexity)	Area (in um²)	Latency (clock cycle)	accessible I/O
a	13	0.02	0.5	yes/yes
b	10	0.01	0.5	yes/yes
c	9	0.02	0.25	yes/yes
d	12	0.02	0.5	yes/yes
e	10	0.01	0.5	yes/yes
f	17	0.03	0.5	yes/yes
proposed	12	0.02	0.5	yes/yes

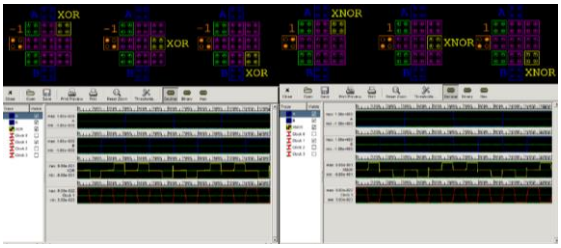


Fig. 14. The structure of the TFXOR and TFXNOR gates and its simulation results.

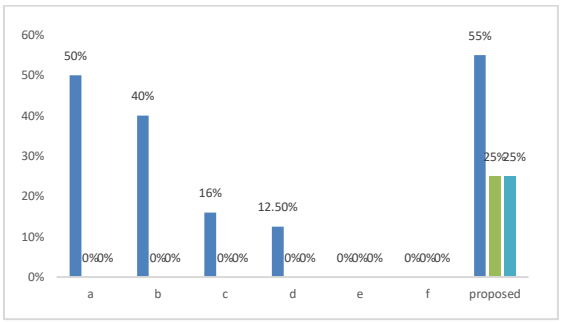


Fig. 15. Comparing the tolerance of the proposed gates against defects with those of the gates presented in [20]-[25] (shown in Figure 12)

D) 3-inputs Tile-shaped XOR gate

In CMOS technology, two binary XOR gates needed to be connected serially to create a ternary XOR gate, in which the output of the first two inputs would be XORed with the third input. Furthermore, in the past, designing a ternary XOR gate seemed to be difficult in QCA [26]. However, by using the intercellular interactions in this technology, the design and implementation of ternary gates have become very simple and efficient [23], [25]. An interesting feature of the TFXOR gate is that it can be used as a ternary gate as well, which means that it can be used in the circuits that have been mentioned earlier. This gate and its simulation are shown in Figure 16.

Figure 17 shows a full-subtractor that is designed using the TFXOR, together with its simulation results. The full-subtractor has 41 cells and is designed and implemented using a fault-tolerant XOR gate, a fault-tolerant majority gate as presented in [27], and robust-wires that have been enhanced by redundancy. The results show that, on average, the circuit is robust against the missing cell and rotated cell defects by 81.5%, and against the extra cell defect by 83%.

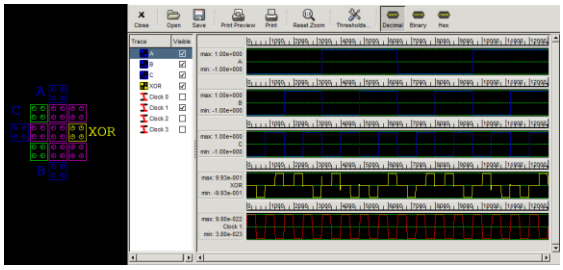


Fig. 16. Figure 16. The structure of the 3-inputs Tile-shaped XOR gate and its simulation results

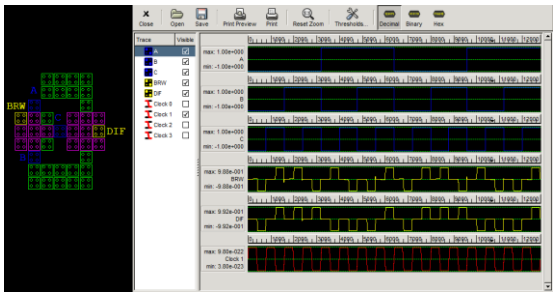


Fig. 17. The structure of the full-subtractor and its simulation results

5. Conclusions

It is well-known that CMOS technology has various limitations. There have been numerous efforts to introduce an appropriate alternative for this technology. QCA is one of the candidates and has its own advocates. Due to its high density and speed, low power consumption, and small size, QCA is one of the most prominent alternatives for CMOS. However, despite these advantages, just like any other technology, it has some problems too. The most notable of those is its relatively high fault-rate. Therefore, the design and implementation of highly reliable integrated circuits while keeping the complexity at a minimum level is imperative for this technology. Since XOR/XNOR gates are commonly used in extended circuits, we decided to provide an alternative design and implementation for these gates with less complexity and more fault-tolerance. The proposed TFXOR / TFXNOR gates are based on intercellular interaction and have a dense tile-shaped structure, which helps them to be more tolerant against some types of defects compared to the other gates. The simulation results indicate that we have achieved both of our goals, namely less complexity and more fault-tolerance. Also, as the gate is designed based on intercellular interactions, it has been used as a 3-inputs gate as well. Finally, to show the correct performance of the gate, it has been used in a fault-tolerant full-subtractor, in this paper.

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