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Single Spiking Neuron as Direct Digital Frequency Synthesizer

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Abstract

Studies on third generation of neural networks, called spiking neural networks (SNN), have been developed recently according to the neuroscience. SNNs are used to model natural computing of the brain. Spike train-based networks investigated as signal processing of the brain is an objective. This paper proposes a digital hardware implementation of a single spiking neuron. The neuron is used as a direct digital frequency synthesizer. The proposed architecture uses leaky integrate and fire (LIF) neuronal model which is easy to implement. Inter spike interval (ISI) of the input and the output spikes are used as coding scheme. A FPGA platform is utilized due to its flexibility and real time applications. The simulation results of both Matlab and Quartus II indicate acceptable accuracy of the proposed design compared to the related works. The Verilog language is used for hardware simulation. The maximum operating frequency of 250 MHz is reached on Cyclone III device.

Keywords: Spiking neural network. Direct digital frequency synthesizer, Leaky integrate and fire.

1. INTRODUCTION

In a spiking neural network, neurons are in contact and transmit information by a sequence of spikes called spike trains. SNNs are similar to the biological neurons of the brain, hence they are used to analyze the brain functionality. A wide range of engineering applications could be solved by spiking models, like controlling a motor, feature recognition and signal processing. Versus non-spiking neural models, like Perceptrons, SNNs are computationally more efficient [1]. Recently SNNs become more interesting branch of neural sciences. SNNs are the third generation of neural networks. They use accurate firing time of spikes for

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information coding. In this case, pulse stream solutions for data coding have been introduced [2]. Spiking neural networks have two significant benefits, very fast decoding of sensory information like visual system of human brain and the ability of multiplexing such information like combination of the amplitude and the frequency of an auditory system. As an implement of the SNNs, both analog and digital designs have been presented. The FPGA platforms are widely used because of their flexibility and real time processing ability [3]. A hippocampus inspired spiking neural network is implemented on an FPGA by M. Mokhtar, et al [4]. Izhikevich spiking neurons in a pipelined manner on FPGA is presented by K.L Rice, et al [5] . E L Grass, et al have considered another FPGA based approach for high speed simulation of conductance-based neuron model [6].

A spiking neural network architecture for non- linear function approximation is presented. It uses several simple LIF neuron to estimate each point of corresponding value separately [7,8]. One of the most significant functions is the sine function suitable for our purpose in order to its natural behavior. This paper presents a single neuron of the Leaky Integrate, and Fire model could be used to estimate the sine function. The LIF model is the simplest model of spiking neurons that could be beneficially implemented. The most common method of generating analog signals by digital operations is Direct Digital Frequency Synthesizer (DDFS), that is mostly concerned with sinusoidal waveforms. The DDFS has many advantages in comparison with other methods, like micro Hz frequency resolution, including fast hopping, remote controlling ability, and wide frequency range [9]. Applying digital model of the LIF single neuron to generate sine wave of various frequencies will gain a DDFS which can be biologically inspected. In this paper, a single LIF neuron acts as a direct digital frequency synthesizer. At the rest of this paper, in section 2, the SNN and the LIF model are discussed. Section 3 describes the main components of a conventional DDFS briefly. Section 4 depicts the sine wave approximation algorithm, the network architecture and digital implementation of the LIF neuron. Section 5 represents the simulation results and finally section 6 is the conclusion.

2. SPIKING NEURAL NETWORKS

2.1. Review

The structure and the function of the brain have been studied by details recently. The heart of the brain's processing unit are neurons in contact together through a complex structure. Three main parts of the neuron are called soma, dendrites and axon. Each of them has different functionality. Act of collecting the input signals from other neurons is done by the dendrite. The soma is the central processing unit of the neuron. The output signals are transmitted to other neurons via the axons. A link between two neurons is called a synapse. Pre-synaptic cell is referred to the neuron sends signals. The neuron which receives signals, is called post-synaptic neuron. The brain cortex consists of axons starched over several centimeters. Each single neuron may be connected to more than 10^{14} post synaptic neurons. In a spiking neural system, a pulse stream

including signals of 100mV amplitude and 1-2 ms duration is called spikes. It is used to transmit information. A series of consecutive spikes which may have various time intervals are called spike train. Since the spikes have the same shape, time intervals between them are noticeable and should be accounted as a significant parameter of data coding. When a pre-synaptic neuron sends spikes, the post-synaptic neuron which receives the spikes with specific inter spike time interval will be affected. The incoming spikes cause a potential change which can be measured by placing a fine voltmeter. Potential difference between interior of the cell and the surrounding is called membrane potential. When there is no input spike the cell is at rest potential due to the difference of the ions concentration. When a spike arrives, the membrane potential is increased or decreased in order to excitatory or inhibitory spikes. As the membrane potential reaches a certain value called threshold, the output spike is generated and the membrane potential backs to its initial value [10].

2.2. Leaky Integrate and Fire (LIF) Model

LIF is one of the spiking neural models, that is easy to implement. Integrate and fire model are used for large scale VLSI and massively parallel networks implementation. At this model, input current is integrated till it reaches to the threshold voltage, then the neuron is fired and the output spike is generated [11]. Figure 1 illustrates a single neuron schematic and it's LIF model. Assume the pre-synaptic neuron j sends spikes toward neuron i at the specific times (f=1,2,…). It is shown by $t_j^{(f)}$. Each spike

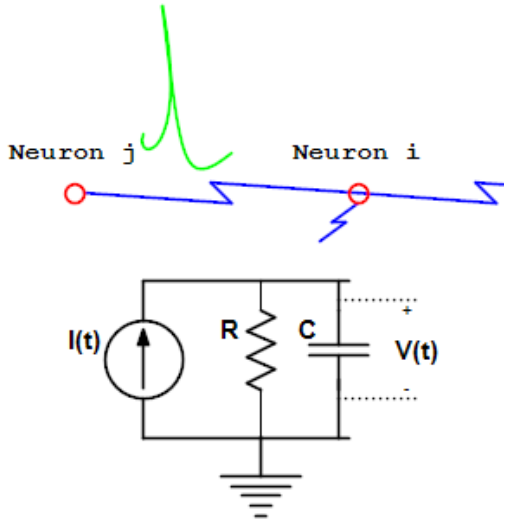

Fig.1. LIF model of SNN.

evokes a post-synaptic potential (ε_{ij}), total change of the membrane potential can be estimated by Eq.1. The LIF model comprises of three main parameters (Eq.2). R is used to model resistive path from the inside of the cell toward the outside. Interior of the cell is separated from the surrounding by a membrane which resembles a capacitor modeled by C. Total input spike is modeled by a current source I(t).

$$vi(t) = \sum_j \sum_f \varepsilon_{ij}(t - t_j^{(f)}) + v_{rest} \quad (1)$$

$$C\frac{dV}{dt} = -\frac{V}{R} + I(t) \quad (2)$$

3. DIRECT DIGITAL FREQUENCY SYNTHESIZER

Conventional DDFSs consist of three main units. A phase value generator, a phase to amplitude converter and finally a digital to analog converter. Simply a phase accumulator may be used to prod- uce phase values, then a Look Up Table converts the phase to its corresponding value [12]. Quarter symmetry of the sine function may be used as

a compression technique so that ,0-π/2, values of the sine could be stored instead of the whole [13,14] (Fig.2). There are various area reduction and frequency improvement techniques that are not concerned in this work. The output frequency of the DDFS depends on FCW (frequency control word), fs (system clock) and the size of the phase accumulator (N) by the following equation:

$$f_{out} = FCW.\frac{f_s}{2^N} \quad (3)$$

The frequency resolution of the output wave will be clearly attained by choosing FCW=1, so the resolution is $fs/2^N$. It is deduced that the maximum output frequency and the frequency resolution have direct relation with the clock frequency. Due to the phase truncation, Spurious free dynamic range (SFDR) of the output wave is determined by equation 4 that parameter I denotes number of bits which are used for ROM addressing. To reach higher SFDR more area consumption is unavoidable although some area reduction techniques can be employed [9].

$$SFDR = 6.02(I) \quad (4)$$

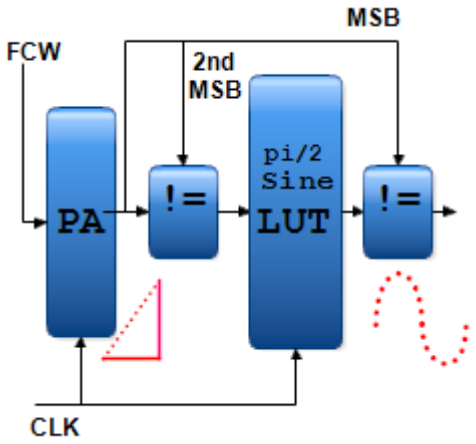

Fig.2. Direct digital frequency synthesizer.

4. SINGLE LIF NEURON ARCHITECTURE FOR DDFS APPLICATION

4.1. Proposed Architecture

Biological neurons receive many spikes as infor- mation to be processed (neural codes) [15]. A temporal encoding scheme is defined. The inter spike interval (ISI), the temporal distance between two successive spikes represents a real-valued quantity (x_i) as in equation 5. $T_i(1)$ and $T_i(2)$ are the arrival times of the first, and the second spikes to neuron i. Δ_i is used to denote the ISI [7].

$$x_i = T_i(2) - T_i(1) = \Delta_i \quad (5)$$

The proposed architecture comprises of two input lines that one of them has τ_d delay, as input unit. A LIF single neuron is also included as the activation unit. There are two output lines. One of them is delayed by an adjustable value named Q (Figure 3). Assuming U(t) is fed to the activation unit through the line has no delay, total input can be simulated as Eq.6. Accordingly, noting to the LIF mathematical equation (Eq.2.), membrane potential is calculated, where τ_m= 1/RC is the activation unit's time constant. As the membrane potential reaches the threshold value, activation unit fires and the output spike pair are generated. The Phase Accumulator (PA) generates all phase values and updates τ_d. Each τ_d(input) should be converted to its corresponding amplitude. For this end, a single LIF neuron network is pre-trained and all Q values are stored in a ROM (LUT). To apply the quadratic symmetry, two MSB bits of the phase value are used to determine first half cycle or second. Simple

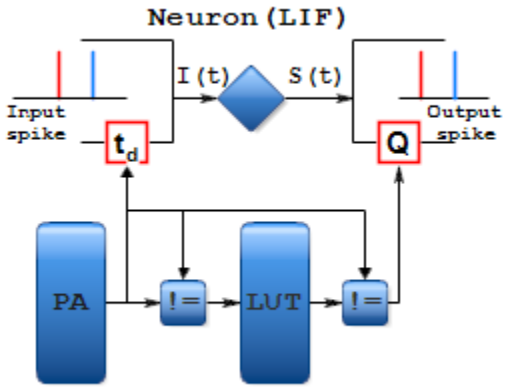

Fig.3. Proposed single LIF neuron DDFS.

gradient descent algorithm (Eq.7) is used to train the network. Each Q initially is set to a random value then the difference of the basic sine function and the approximated value is used to determine final Q [7]. The threshold value of the activation unit is set to fire with maximum τ_d , so for all input values spikes will be generated.

$$I(t) = U(t) + U(t - \tau_d) \quad (6)$$

$$\Delta Q = 0.7(F(x_i) - Q) \quad (7)$$

$$Q = \Delta Q + Q \quad (8)$$

4.2. Digital Implementation of LIF Neuron

Lower cost, flexibility, availability and digital precision make FPGA a good choice for implementation of neuromorphic systems [16]. To overcome analog neuromorphic circuits problems like area and power consumptions, a pure digital implementation is performed in this work [17,18]. Digital implementation of LIF neuronal model can be performed using Euler's equation (Eq.9) So that two separated blocks are used as synapse and neuron core (membrane) blocks. Each block consists of a counter starts counting from initial value to an adjustable value named w or th. When input spike reaches to the synapse core, the counter starts counting and the output of the core feeds the neuron core which is set to be high. When value of counter reaches to the weight(w) value, the counter is reset and the output backs to logic zero. Similarly, the core block acts as a up/down counter in order to Exc/!Inh (excitatory or inhibitory input spike); when the input pulse is logic one . To model leaky current, when there is no input pulse to the membrane counter (i.e. no counting due to the input spikes), the membrane counter value is decremented with an adjustable step called leak period [19]. According to the proposed DDFS architecture, synaptic weight should be set to have approximate constant firing intervals for all possible input values and all spikes assumed to be excitatory.

$$v(i+1) = v(i) + \frac{\Delta t}{C}\left(-\frac{1}{R}v(i) + I_{Leak}\right) \quad (9)$$

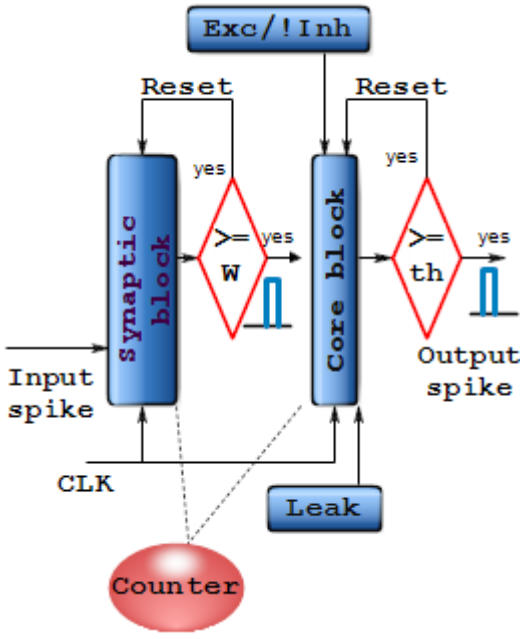

Fig.4. Digital LIF neuron model.

5. SIMULATION RESULTS

The LIF neuronal model is implemented where all input spikes are assumed to be excitatory with a constant synaptic weight. When the membrane potential reaches the threshold, the output spike is generated. Figure 5 shows the simulation result. In the proposed DDS, optimization of the phase accumulator and the phase to amplitude converter are not considered. The proposed structure incl- uses a 8 bits phase accumulator to generate the phase values with an adjustable step called FCW. A 256 bytes memory is also included to store quarter of the sine function values (each byte: 6 bits fraction 2 bits integer). Two 8 bits counters are used as the core block and the synaptic block of the LIF neuron. According to the phase values input, spike is delayed and feeds the synaptic core. Pre-trained values of the sine function stored in the LUT specifying the output spike's inter spike intervals (ISI). As the membrane potential reaches the threshold value, the output spikes pair are generated with an adaptive time interval dictated by the pre-trained values. Figure 6 and 7 show the simulation results of Quartus II and MATLAB consequently, where the sine is scaled to have better point of view. This structure is simulated on Cyclone III FPGA of Altera family using Verilog HDL language. The maximum operating frequency of 250 MHz is reached. The spurious free dynamic range (SFDR) of 71 dB is obtained. Table 1 shows the proposed work which could improve both the maximum operating frequency and the SFDR comparing to [21] and [22]. Figure 6 is the simulation result that is graphed by Modelsim EDA tool. The simulation shows the proposed architecture contains 37 logic elements, 2048 memory bits and 28 dedicated logic registers (Table 2).

6. CONCLUSION

Consideration of neuro-biological signal processing systems imply translation of spiking neural models to hardware implementation. As performance and flexible point of view, FPGAs are suitable platforms to this end. Using direct digital frequency synthesizers, high accuracy sinusoidal waveforms contribute in data transmission which could be generated and mixed

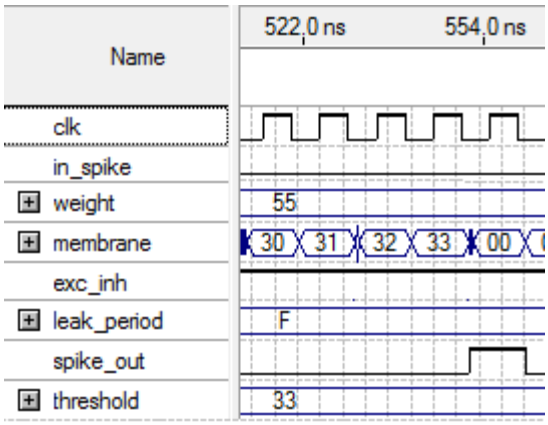

Fig.5. Quartus II simulation result of digital implementation of the LIF neuronal model.

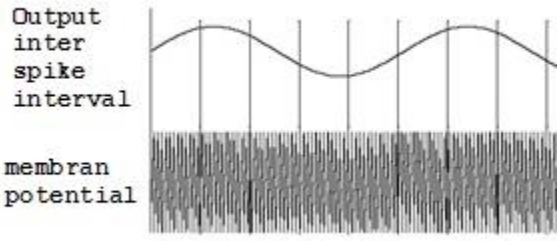

Fig.6. Quartus Modalism simulation of the proposed single neuron (LIF neuronal model) DDS.

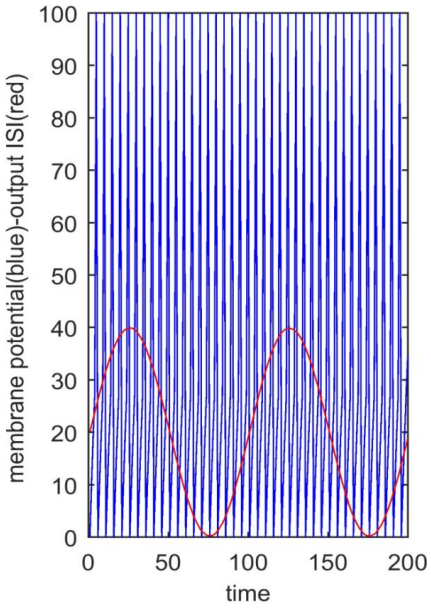

Fig.7. Matlab simulation of the proposed single neur- on (LIF neuronal model) DDS.

Table 1. ***Comparison of f_{max} and SFDR.***

	f_{max} (MHz)	SFDR (dB)
Proposed work	250	71
[21]	100	68.4
[22]	200	-

Table 2. ***Device utilization summary.***

Device utilization summary		
Logic utilization	Used	Utilization
Total logic elements	37	<1%
Total registers	28	<1%
Total memory bits	2048	<1%

together. This paper represents single neuron of leaky integrate and fire model used for DDFS applications. There are various area reduction techniques like COO- RDIC algorithm [20] and trigonometric relations of the sine function. Instead of LUT based single neuron model that is implemented in this paper, multi neurons structures that have the ability of estimating one point by each neuron could be utilized. Increasing the maximum operating frequency is an objective although area reduction techniques can be used as further works.

REFERENCES

[1] Ponulak, F. Kasinski, A.: Introduction to spiking neural networks: Information processing, learn- ing and applications. Acta neurobiological experimentalis 71(4), 409-433 (2010)

[2] Maass, W.: Networks of spiking neurons: the third generation of neural network models. Neural Netw, 10 (9), 1659–1671 (1997)

[3] Shayani, H., Bentley, P., Tyrrell, A.M.: A cellular structure for online routing of digital spiking neuron axons and dendrites on FPGAs. In: Evolvable Syste ms: From Biology to Hardware, pp .273–284. Springer, Berlin (2008)

[4] Mokhtar, M., Halliday, D., Tyrrell, A. Hippoca- mpus-inspired spiking neural network on FPGA. Evolvable Systems: From Biology to Hardware, 362-371.(2008)

[5] Rice, K. L., Bhuiyan, M. A., Taha, T. M., Vutsi- n as, C. N.,Smith, M. C.:FPGA implementation of Izhikevich spiking neural networks for character recognition. In Reconfigurable Computing and FPGAs, 2009. ReConFig'09. International Conference on (pp. 451-456). IEEE. (2009).

[6] Graas, E. L., Brown, E. A., Lee, R. H.: An FPGA-based approach to high-speed simulation of conductance-based neuron models. Neuro-informatics, 2(4), 417-435. (2004)

[7] Iannella, N., Back, A.D.: A spiking neural network architecture for nonlinear function approximation. Neural Netw. 14(6), 933–939(2001)

[8] Farsa, E. Z., Nazari, S., Gholami, M.: Function approximation by hardware spiking neural network. Journal of Computational Electronics, 14(3), 707-716. (2015)

[9] Soleimani Abhari, P.Dosaranian Moghadam, M.: Design and Simulation of a Modified 32-bit ROM-based Direct Digital Frequency Synthesizer on FPGA .: AUT Journal of Electrical Engineering , 47(1), 23-29 (2015)

[10] Gerstner, W. Kistler, W.: Spiking Neuron Mode- ls Cambridge University Press.(2002)

[11] 8 . Indiveri, G., et al.: Neuromorphic silicon neu- ron circuits. Front. Neurosci. 5, 1 (2011)

[12] Vankka, D. J.: Digital Synthesizers: Theory, Design and Applications.(2000)

[13] Yang, B. D. Kim, L. S. Yu, H. K..: A high speed direct digital frequency synthesizer using a low power pipelined parallel accumulator.: In Circuits and Systems, 2002. ISCAS 2002. IEEE International Sy- mposium on, Vol. 5, . (2002)

[14] 14.Symons, P. R.: DDFS phase mapping technique Electronics Letters, 38(21), 1291-1292. (20- 02)

[15] Shadlen, M.N., Newsome, W.T.: Noise, neural codes and cortical organization. Curr. Opin. Neuro- biol. 4(4), 569–579 (1994)

[16] Li, W.X., Cheung, R.C., Chan, R.H., Song, D., Berger, T.W.: Real-time prediction of neuronal population spiking activity using FPGA. IEEE Trans. Biomed. Circuits Syst. 7(4), 489–498 (2013)

[17] Nazari, S., Faez, K., Amiri, M., Karami, E.: A novel digital implementation of neuron-astrocyte interactions. J. Comput. Electron., 1–13 (2014)

[18] Nazari, S., Amiri, M., Amiri,M.: Multiplier-less digital implementation of neuron-astrocyte Signalling on FPGA. Neurocomputing (2015)

[19] Joubert, A. Belhadj, B. Temam, O. Héliot, R. .: Hardware spiking neurons design: Analog or digital?. In Neural Networks (IJCNN), The 2012 International Joint Conference on (pp.1-5) .(20- 12).

[20] Kang, C. Y, Swartzlander, E. E.: Digit-pipelined direct digital frequency synthesis based on diff- erential CORDIC. IEEE Transactions on Circuits and Systems I: Regular Papers, 53(5), 1035-1044 .(2006).

[21] Wang, Chua-Chin, Hsiang-Yu Shih, and Wei Wang. "High SFDR Pipeline ROM-less DDFS Design on FPGA Platform Using Parabolic Equations." 2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT). IEEE, pp 1-4 (2018).

[22] Wang, Pu, Yuming Zhang, and Jun Yang. "Design and Implementation of Modified DDS Based on

FPGA." Procedia computer science 131, pp 261-266. (2018)