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Research Paper

A Non-isolated Quadratic High-Gain DC–DC Converter for Smart High-Intensity Lighting Systems in Multimedia and Intelligent Environments

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ABSTRACT

This paper introduces a novel non-isolated high step-up DC-DC converter topology that employs a dual-stage boost structure combined with diode–inductor voltage multiplier cells. By leveraging a quadratic boost mechanism, the converter achieves significant voltage amplification at moderate duty cycles, thereby enhancing overall efficiency and ensuring improved operational stability under various loading conditions. A primary advantage of the proposed topology lies in its capability to reduce voltage stress on semiconductor components, which not only prolongs device lifespan but also minimizes switching losses and thermal stress during operation. The incorporation of two coupled inductors ensures continuous input current, effectively reducing electromagnetic interference (EMI) and input current ripple, which contributes to stable performance and improved power quality. In addition to delivering high power density, the proposed converter offers a lightweight and cost-effective solution suitable for modern power-electronic applications. The shared common ground between the source and the load further simplifies its integration into practical systems, facilitating safer implementation. The voltage ratio of the proposed converter has been extracted for both ideal and non-ideal operating modes to provide a clearer understanding of its behaviour. Moreover, the practical voltage ratio of the converter has been obtained, analyzed, and compared with the result derived from the non-ideal voltage-gain relationship. Finally, the simulation results have been detailed and compared with the corresponding experimental results to validate the theoretical analysis. The PLECS software is the simulation engine used in this study to verify the performance of the proposed topology.

NOMENCLATURE

f_s	Switching frequency	I_{Li}	The current of the i-th inductor
D	Duty cycle	V_{Si}	The voltage of the i-th switch
V_{in}	Input Voltage	I_{Si}	The current of the i-th switch
V_o	Output Voltage	V_{Di}	The voltage of the i-th diode
I_{Li}	The current of the i-th inductor	I_{Di}	The current of the i-th switch
V_{Ci}	The voltage of the i-th capacitor		

I. Introduction

Nowadays, power electronics has significantly transformed modern life, influencing power generation, transportation, and numerous industrial processes. Among these technologies, DC–DC converters are widely employed across various industrial applications [1]–[5]. DC–DC converters can be categorized into two main types: isolated converters, which utilize high-frequency transformers, and non-isolated converters, which do not incorporate any high-frequency transformer within their topology. The core loss, saturation of the transformer core, EMI, high stress of the switches, increase of the volume and cost , and decrease of the efficiency in isolated DC-DC converters, have caused the popularity of the non-isolated DC-DC converters [6]-[9].

Among the conventional non-isolated DC-DC converters, the boost converter can operates as a step-up converter for all value of the duty cycle in its ideal mode. To have a high voltage ratio, the duty cycle have to approach to unity. However, such a decision can cause some challenges that prevents the achieve of the high voltage ratio. In other words, the high value of the duty cycle reduces the conduction time of the diode in a way that approaches to zero. However, the reverse recovery time of the diode prevents the mentioned result. Moreover, the high value of the duty cycle concludes high stress of semiconductors. Consequently, the efficiency decrease. To increase the voltage ratio of the non-isolated DC-DC converters, some techniques such as Luo's converters and cascade technique have been introduced. The complexity of the Luo's converters to achieve high voltage ratio, has caused the increase of the Components number, power loss, and dimension. The cascade of the simple typologies to increase the voltage ratio can cause the decrease of the efficiency. In other words, the efficiency of the whole topology is the production of its consisting simple typologies. Therefore, the efficiency of the whole topology is lower than the consisting ones [6]-[9]. Moreover, the incorporation of parasitic elements in inductors and switching elements imposes a serious constraint on the practical realization of high-gain capabilities. These parasitic resistances dissipate power in switching transitions and limit the effective current rise in the inductor, resulting in system efficiency and stability degradation [10].

In [11], a combination of the boost and cuk converter has been proposed. The voltage ratio of the proposed converter is the square of the buck-boost converter voltage ratio. Consequently, for 50 percent as the value of the duty cycle, it operates in pass through mode. In other words, its voltage ratio is unity. Moreover, the voltage stress of the switches is high which can decrease the efficiency. In [12]-[13], other types of the quadratic buck-boost converters have been proposed. The voltage ratio becomes unity as the duty cycle becomes 50 percent. In [13]-[14], other types of the step-up converters have been proposed. As the duty cycle becomes 50 percent, the voltage ratio of the proposed converter in [14]-[15] becomes 2. In other words, their voltage ratio is as same as boost converter. However, the number of the components is more than boost converters components. Consequently, the high voltage ratio, requires high value of the duty cycle which decrease the efficiency by increase of the loss. An improved cascaded boost converter with voltage multiplier cells [16] uses a voltage lift technique that does not depend on the VMC and connects the input source and output capacitor with a diode to increase the voltage gain. However, the parallel and series connections of the capacitors cause inrush current issues that increase conduction loss and current stress. Another proposed converter [17] does not use the voltage lift technique and combines two boost converters. The voltage gain is less than [17], [18], [19], [20], but it does not have inrush current issues. However, the voltage stress of the second diode is higher than the output voltage, which is caused by the replacement of the first capacitor and diode in the first part. The proposed converter in [21] combines the conventional buck-boost and boost converters to provide a voltage gain that is the summation of the consisting parts. The output capacitor voltage is divided between two capacitors to reduce the output capacitor voltage stress. However, the input current ripple is increased, and the common ground of the input source and load is lost. Another proposed topology [22] is an improved boost converter with two VMCs that uses quadratic converters and voltage lift features to increase the voltage gain. The appeared inrush currents have less effect than previous ones, but the input current ripple is increased. The proposed topology in [23] is a combination of an improved boost converter with a VMC and a super lift Luo converter that improves the voltage gain but increases conduction loss and current stress due to inrush currents. A proposed topology [24] eliminates the common ground of the input source and load to increase the voltage gain but increases the input current ripple and the number of diodes, which decreases reliability.

The main contributions of this paper can be summarized as follows:

• Proposing a new non-isolated quadratic DC–DC converter topology that achieves a high voltage gain at moderate duty cycles without using transformers or coupled inductors.

• Reducing voltage and current stresses on semiconductor devices by distributing the output voltage across multiple capacitors and employing diode–inductor voltage multiplier cells.

• Providing a comprehensive non-ideal analysis that explicitly considers parasitic resistances of inductors, switches, and diodes, and investigates their impact on voltage gain and efficiency.

• Demonstrating the suitability of the proposed converter for high-intensity discharge (HID) lighting applications

through detailed PLECS simulations, including ignition and steady-state operating phases.

The remainder of this paper is organized as follows. Section 2 introduces the proposed converter, while Section 3 presents the analysis of its operation under ideal conditions. Section 4 examines the converter's performance under non-ideal conditions. Section 5 provides the simulation results, and finally, Section 6 concludes the paper by summarizing the key findings.

II. Proposed Converter

The non-isolated DC-DC converter is designed using two stages: a boost stage and a dual voltage multiplier (VM) stage with diode-inductor cells. The input current is maintained continuously using the boost topology, while the square voltage boost is achieved through the dual-boost configuration. The use of the diode-inductor cell at the converter's input results in lower ripple current and reduced losses by distributing the current across two inductors. Additionally, the VM cells enhance voltage boosting through a capacitor charging-discharging mechanism. The sub-converters are stacked, allowing the output voltage to be shared between two capacitors instead of one, simplifying the selection of capacitors for high-voltage applications and reducing the voltage stress on individual components.

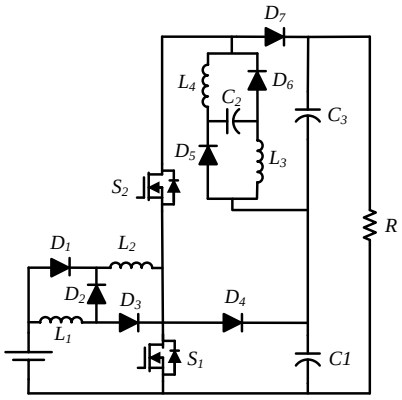


Fig. 1. The proposed converter.

III. Converter's function in the ideal mode

The analytical study is conducted under the assumption of continuous conduction mode (CCM), which is the dominant operating mode for high-power and high-gain applications. The CCM operation ensures reduced current ripple, improved efficiency, and lower stress on power components. The boundary conditions between CCM and DCM are analytically derived and illustrated to clarify the valid operating region of the proposed converter.

In steady-state operation, the equivalent circuit diagrams for both the first and second operating modes are shown in Fig. 2 Based on these equivalent circuits, the equations governing the inductor voltage and capacitor current can be expressed as follows:

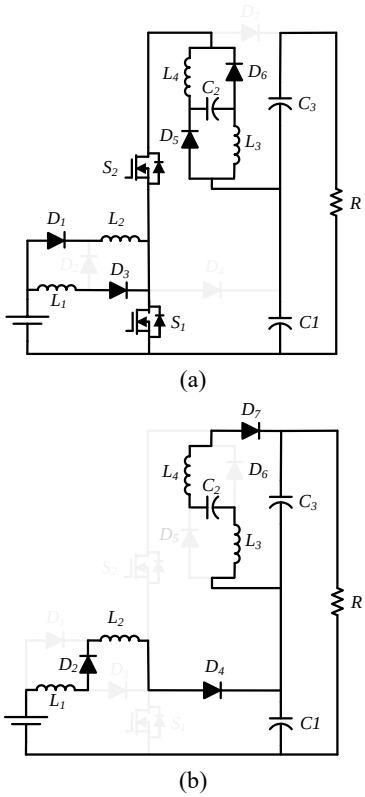


Fig. 2. (a) the equivalent circuit of the first mode, (b) the equivalent circuit of the second mode.

In the first operating mode, the first and third diodes are activated due to their forward bias as the switches begins to conduct. Meanwhile, the inductors become magnetized, and their voltages are positive. The circuit schematic of the proposed converter is shown in Fig. 2 (a). In the second operating mode, the switches are OFF. At the same time, the first and third diodes are in reverse bias. On the other hand, the second and fourth diodes begin to conduct the current. The circuit schematic of the converter is illustrated in Fig. 2 (b). The equations describing the inductor voltage and capacitor current are written as follows:

$$\begin{cases} V_{L_1} = D\left(V_{in}\right)+\left(1-D\right)\left(V_{in}-V'\right) \\ V_{L_2} = D\left(V_{in}\right)+\left(1-D\right)\left(V'-V_{C_1}\right) \\ V_{L_3} = D\left(V_{C_1}\right)+\left(1-D\right)\left(2V_{C_1}-V''\right) \\ V_{L_4} = D\left(V_{C_1}\right)+\left(1-D\right)\left(V''-V_o\right) \end{cases} \quad (1)$$

$$\begin{cases} i_{C_1} = D\left(-I_o-i_{L_3}-i_{L_4}-i_2\right)+\left(1-D\right)\left(i_{L_1}-I_o\right) \\ i_{C_2} = D\left(i_2\right)+\left(1-D\right)\left(-i_{L_3}\right) \\ i_{C_3} = D\left(-I_o\right)+\left(1-D\right)\left(i_{L_3}-I_o\right) \end{cases}$$

According to the voltage second balance, the average voltage of the inductors is zero. Moreover, according to the

current second balance, the average current at the capacitors is zero. Applying these facts to inductors' voltage and capacitors' current equations leads to capacitors' average voltage and average current of the inductors and inrush currents as follows:

$$\begin{cases} V_{C_1} = V_{C_2} = \dfrac{1+D}{1-D} V_{in} \ , \ V' = \dfrac{1}{1-D} V_{in} \\ V_{C_3} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \ , \ V'' = \dfrac{(1+D)(2-D)}{(1-D)^2} V_{in} \\ V_o = \dfrac{2(1+D)}{(1-D)^2} V_{in} \end{cases} \quad (2)$$

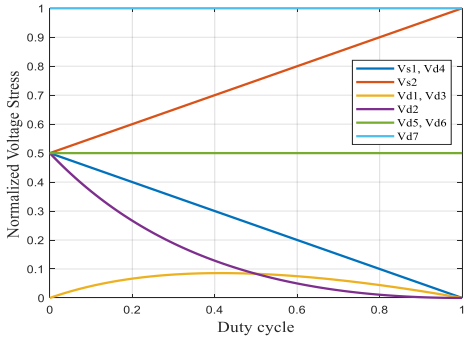
$$\begin{cases} i_{L_1} = i_{L_2} = \dfrac{2}{(1-D)^2} I_o \\ i_{L_3} = i_{L_4} = \dfrac{1}{1-D} I_o \\ i_2 = \dfrac{1}{D} I_o \end{cases}$$

Extracting the average voltage of the capacitors and the average value of the inductors and capacitors' inrush currents helps to define the semiconductor voltage/current stresses as follows:

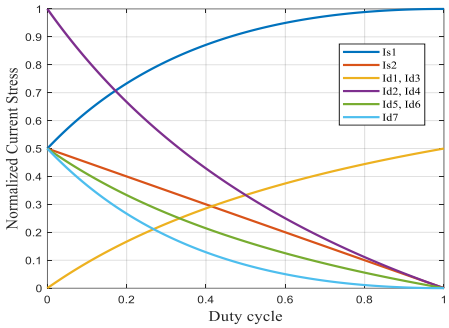
$$\begin{cases} V_{D_1} = V_{D_3} = \dfrac{D}{1-D} V_{in} \ , \ V_{D_2} = V_{in} \\ V_{S_1} = V_{D_4} = \dfrac{1+D}{1-D} V_{in} \ , \ V_{S_2} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ V_{D_5} = V_{D_6} = \dfrac{1+D}{(1-D)^2} V_{in} \ , \ V_{D_7} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \end{cases} \quad (3)$$

$$\begin{cases} I_{S_1} = \dfrac{1+4D-D^2}{(1-D)^2} I_o \ , \quad I_{S_2} = \dfrac{1+D}{1-D} I_o \\ I_{D_1} = I_{D_3} = \dfrac{2D}{(1-D)^2} I_o \ , \ I_{D_2} = I_{D_4} = \dfrac{2}{1-D} I_o \\ I_{D_5} = I_{D_6} = \dfrac{1}{1-D} I_o \ , \ I_{D_7} = I_o \end{cases}$$

Fig. 3 illustrates the normalized voltage and current stresses experienced by the semiconductor devices. It is important to note that the input current is considered as the reference base current, while the output voltage serves as the reference base voltage. From this figure, it can be clearly observed that all normalized stress values remain below unity, indicating that the semiconductors are operating within acceptable limits.



(a)



(b)

Fig. 3. Semiconductors normalized: (a) voltage stress, (b) current stresses.

The simplified form of the inductor's current ripple and capacitor's voltage ripple are as follows:

$$\begin{cases} \Delta V_{C_1} = \dfrac{\left(1+2D-D^2\right) I_o}{(1-D) C_1 f_s} \\ \Delta V_{C_2} = \dfrac{I_o}{C_2 f_s} \ , \ \Delta V_{C_3} = \dfrac{D I_o}{C_3 f_s} \end{cases}$$

$$\begin{cases} \Delta i_{L_1} = \dfrac{D V_{in}}{L_1 f_s} \ , \ \Delta i_{L_2} = \dfrac{D V_{in}}{L_2 f_s} \\ \Delta i_{L_3} = \dfrac{D(1+D) V_{in}}{(1-D) L_3 f_s} \ , \ \Delta i_{L_4} = \dfrac{D(1+D) V_{in}}{(1-D) L_4 f_s} \end{cases} \quad (4)$$

where the f_s refer to switching frequency. The inductors' minimum value to keep the continuous conduction mode is as follows:

$$\begin{cases} L_1, L_2 \geq \dfrac{D(1-D)^4 R}{8(1+D) f_s} \\ L_3, L_4 \geq \dfrac{D(1-D)^2 R}{4 f_s} \end{cases} \quad (5)$$

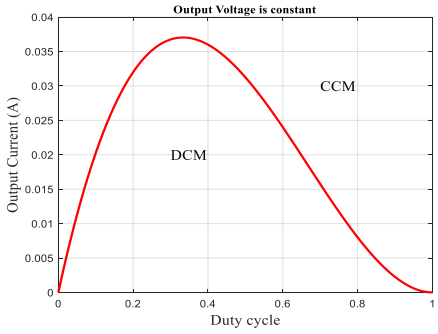
where R refers to the load value. Fig. 4 presents the converters' behavior in the continuous conduction mode (CCM) and discontinuous conduction mode (DCM)

according to the average output current and the duty cycle. Fig. 4 (a) shows the constant output voltage according to the equation below.

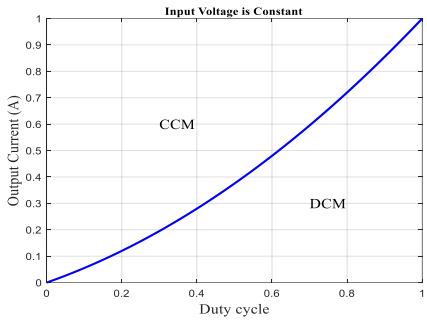
$$I_o = \frac{V_o}{4L_4 f_s} D(1-D)^2 \tag{6}$$

Fig. 4 (b) is for the constant input voltage according to the below equation.

$$I_o = \frac{V_{in}}{2L_4 f_s} D(1+D) \tag{7}$$



(a)



(b)

Fig. 4. Operational region of the converter among CCM and DCM according to the output current and duty cycle value, while: (a) the output voltage is constant, (b) the input voltage is constant.

IV. Converters operate in non-ideal mode

The expressed voltage gain in the second section is for the ideal mode of the circuit components. Considering the parasitic resistance at the inductors (r_L), switches (r_S), and diodes (r_D) the appropriate voltage gain of the practical mode is extracted as follows:

$$\begin{cases} \dfrac{V_o}{V_{in}} = \dfrac{2(1+D)}{(1-D)^2}\left\{1-\dfrac{r_L}{R}\left(\dfrac{1}{(1-D)^3}\right)-\dots\right. \\ \left.\dots-\dfrac{r_S}{R}\left(\dfrac{4+2D-2D^2}{(1-D)^4}\right)-\dfrac{r_D}{R}\left(\dfrac{2-D}{(1-D)^3}\right)\right. \end{cases} \tag{8}$$

where the r_L, r_S, and r_D refer to the equivalent series resistance of the inductors, equivalent series resistance of the switches, and voltage drop of the diodes respectively. According to this equation, Fig. 5 shows a comparison of the ideal and non-ideal voltage gain. The extracted curves are not compatible with all duty cycles. The compatibility interval width depends on the output power and component quality.

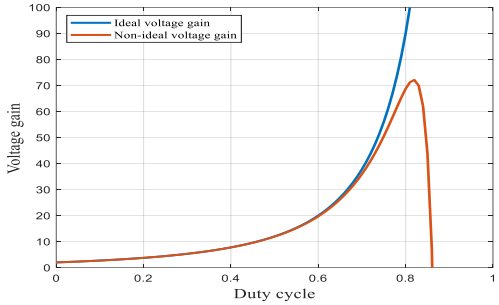
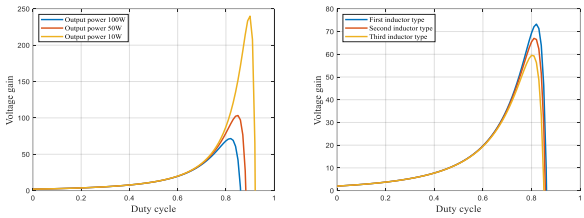


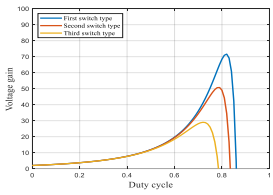
Fig. 5. Ideal and non-ideal voltage gains comparison.

Fig. 6 presents the behavior of the non-ideal voltage gain according to the change of output power, inductors' core type, which affects the conductors' length and resistance, switches' type, which involves the dynamic resistance, and diodes' type, which affects the voltage drop. According to this figure, changing the output power has the highest impact on voltage gain behavior. Consequently, the operation points and conditions must be chosen with a high obsession.

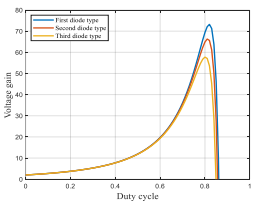


(a)

(b)



(c)



(d)

Fig. 6. Non-ideal voltage gain behavior according to the change of: (a) output power, (b) inductor core, (c) switch type, (d) diode type.

The input and output powers are not the same in the practical conditions. Notably, their difference is the same as the loss value. In other words, defining various types of losses leads to efficiency defining. Due to the accessible components' frequency limits, the switching frequency is not

high. Consequently, the frequency loss of the inductors' switches and diodes is ignored. Notably, the conduction loss of the inductors (P_L), switches (P_{SC}), and diodes (P_D) are considered as follows:

$$\begin{cases} P_L = \dfrac{r_L}{R} P_o \dfrac{2\left(5-2D+D^2\right)}{\left(1-D\right)^4} \\ P_{SC} = \dfrac{r_S}{R} P_o \dfrac{2+8D+12D^2-8D^3+2D^4}{D\left(1-D\right)^4} \\ P_D = V_{DF} I_o \dfrac{7-4D+D^2}{\left(1-D\right)^2} \\ \eta = \dfrac{P_o}{P_o + P_L + P_{SC} + P_D} \end{cases} \quad (9)$$

As same as the voltage gain in the practical conditions, the efficiency is a function of the duty cycle, output power, and component quality. In order to determine the import of the mentioned factors, Fig. 7 presents the efficiency behavior according to the change in output power and component quality. According to this figure, changing output power has the highest impact. For a 100 W output power and 50% duty cycle, the Pic chart of the efficiency and losses have been presented in Fig. 8. According to this figure, the conduction loss of the semiconductors is greater than the conduction loss of inductors.

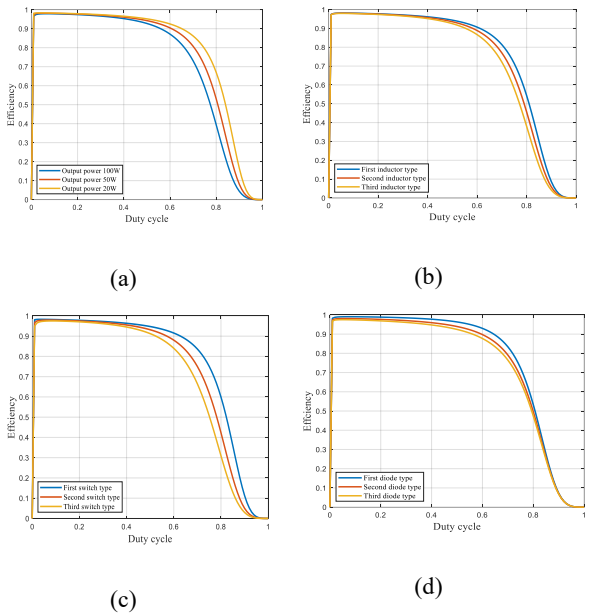


Fig. 7. Efficiency behavior according to the change of: (a) output power, (b) inductor core, (c) switch type, (d) diode type.

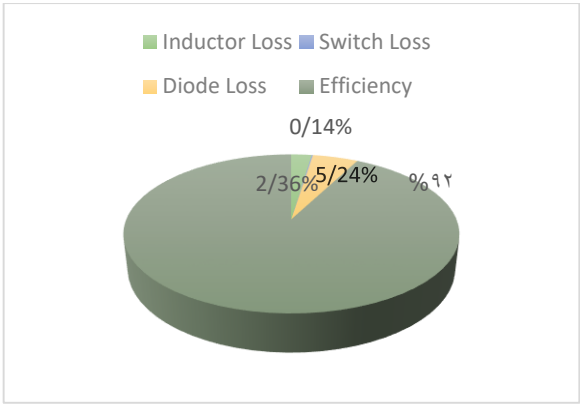


Fig. 8. Pie chart of loss and efficiency.

A comprehensive comparison highlighting the differences and improvements among the existing converter topologies—specifically in terms of the number of components used and their corresponding voltage gains—along with the performance of the proposed converter, is presented in Table 1. This comparison provides a clear overview of the enhancements achieved by the proposed design.

TABLE I : A comparative analysis between the proposed converter and those introduced in previous studies.

Reference	***L***	***S***	***D***	***C***	***Voltage Gain(D=0.5)***
[25]	2	2	5	5	6
[26]	3	2	4	5	10
[27]	2	1	6	5	10
[28]	2	2	2	2	1
[29]	2	2	3	3	7
Proposed	**4**	**2**	**7**	**3**	**12**

As shown in Table I, the proposed converter achieves a higher voltage gain at a moderate duty cycle compared to recent quadratic and high-gain converters, while maintaining a reasonable number of components. This trade-off between voltage gain and component count highlights the effectiveness of the proposed topology in achieving high performance without excessive circuit complexity.

V. Simulation result

Since the proposed study is based on circuit-level modeling and deterministic simulations rather than statistical data, performance validation is carried out through time-domain waveform analysis, voltage gain verification, and loss distribution assessment.

High-intensity discharge (HID) lighting systems require a power converter capable of providing high ignition voltage, controlled current during warm-up, and stable steady-state operation, making them a suitable application domain for evaluating high-gain DC–DC converters.

The proposed converter was simulated in the PLECS environment to precisely evaluate and validate the

theoretical predictions. The simulation parameters are listed in Table 2. In this setup, the duty cycle was fixed at 0.5, the switching frequency was set to 50 kHz, the input voltage was maintained at 20 V, and the converter delivered an output current of 0.41 A. Based on these operating conditions, the component values were selected to ensure appropriate functionality and satisfactory dynamic performance. The inductance values were determined considering an allowable inductor current ripple of 30%, while the capacitor values were chosen to maintain a voltage ripple of 5%.

TABLE II :Simulation parameters

V_{in}	f_s	ΔI_L	ΔV_C	D
40 V	50kHz	30%	5%	50%

As illustrated in Fig. 9, under the specified operating conditions, the simulation performed with an input voltage of 40 V resulted in an output voltage of 480 V. This corresponds to a voltage gain of 12 at the given duty cycle, which aligns precisely with the theoretical predictions. A comprehensive analysis of the practical simulation results for the proposed converter is provided in the subsequent section.

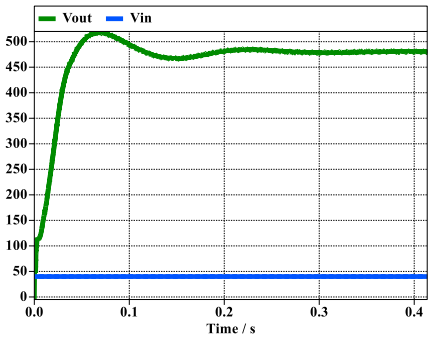


Fig. 9. Input and output voltage waveforms

High-intensity gas-discharge lamps are a class of electric-discharge lighting devices that, owing to their high efficiency, long operational lifetime, and desirable photometric characteristics, are widely employed in applications such as street lighting, stadium illumination, and automotive headlamps. These lamps generate light by establishing an electric arc between two electrodes within a pressurized gas environment. However, proper operation requires a power-supply stage capable of providing the specific electrical conditions demanded by the lamp. The corresponding subsystem was simulated in the PLECS environment. In this stage, a variable resistor (load) was used to model gas ionization and the transition of the inter-electrode path to a conductive state. The use of DC–DC converters in the power supply of HID gas-discharge lamps is highly advantageous due to several key characteristics. These converters can generate the high ignition voltage required for lamp startup by boosting a low input voltage—such as a 12 V battery—to significantly higher levels. Moreover, HID lamps demand stable and precisely regulated voltage and current to ensure optimal performance and to extend their operational lifetime; DC–DC converters equipped with appropriate control strategies are well suited to meet these requirements. Additionally, given that HID lamps are valued for their high luminous efficiency, it is essential that their power supply also operates with high efficiency to prevent unnecessary energy loss and to maintain overall system effectiveness.

The input voltage of the converter was set to 40 V, and the switching frequency was defined as 50 kHz. A PI controller was employed for voltage regulation. Based on the simulation strategy, the controller's reference voltage was increased to its final value using a linear ramp. After conducting the simulation under the specified conditions, the obtained results were analysed. The output voltage and current waveforms of the converter are illustrated below.

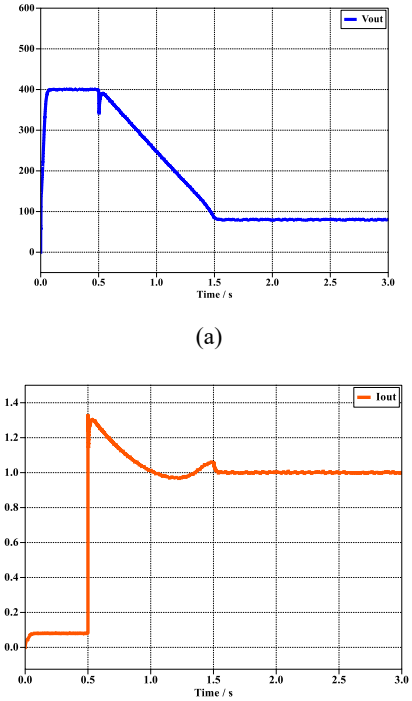


Fig. 10. Waveforms: (a) Output voltage, (b) Output current.

As illustrated in Fig. 10, at the initial stage of the simulation, the lamp has not yet entered the ignition phase; consequently, its equivalent resistance is modeled as a high value, representing the neutral gas condition in which no conductive path has been established. Under these conditions, the current remains negligible, and the primary objective is to gradually increase the converter's output voltage to establish the conditions required for ignition. At t=0.5s, designated as the ignition instant, two simultaneous changes occur in the circuit: (1) a rapid reduction in the lamp's equivalent resistance due to arc formation, and (2) a gradual decrease in the reference voltage from its initial value to the steady-state level of 80 V. This reduction is achieved by the voltage controller over an interval of approximately one second. During this period, the output voltage decreases from the initial 400 V to 80 V and

subsequently stabilizes at this steady-state value. The modelling approach aimed to capture the key operational characteristics of the lamp—namely, the high ignition voltage, the sharp drop in resistance following arc initiation, and the stabilization of output voltage and current—by structuring the simulation into three phases: pre-ignition, ignition, and steady-state.

VI. Conclusion

This paper presents a novel non-isolated high-gain DC-DC converter characterized by several key advantages. Firstly, it ensures the continuity of the input current, which contributes to improved efficiency and reduced electromagnetic interference. Additionally, the converter features a common ground shared between the load and the input source, simplifying the system design and enhancing safety.

One of the most significant benefits of the proposed topology is its ability to achieve a high voltage gain at relatively low duty cycle percentages, which optimizes switching performance and reduces losses. At a duty cycle of 0.5, the proposed converter achieves a voltage gain of 12 while keeping normalized voltage and current stresses below unity for all semiconductor devices. These characteristics confirm that the proposed topology is well-suited for high-gain and high-reliability power conversion applications. Furthermore, the converter design effectively minimizes voltage stress on semiconductor devices, thereby extending their operational lifespan and reliability. Similarly, the current stress on these components is also significantly reduced, enabling the use of smaller, cost-effective semiconductor devices without compromising performance. Another important advantage is the reduced voltage stress on the output terminal capacitors, which improves their longevity and reduces the overall size and cost of the energy storage elements.

All these improvements were clearly demonstrated through comprehensive simulation results. The strong agreement between the simulation data and the theoretical analysis confirms the accuracy and robustness of the proposed mathematical model. This compatibility not only validates the design methodology but also highlights the practical feasibility and effectiveness of the proposed converter in real-world applications.

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