Alternating Rectifier in SDLVA by Power Detector: A Novel Technique for Improved Chip Area and Power Consumption

Nader Javadifar[1], Massoud Dousti[1*], Hassan Hajghassem[2]

Abstract : A novel method to detect microwave signals power in successive detection logarithmic video amplifier (SDLVA) based on single metal-oxide semiconductor field effect transistor (MOSFET) is proposed. This is an alternative for the conventional method of rectifying that logarithmic amplifiers are being used to detect a RF signal power. A complete design and analysis of circuit functioning in saturation region of MOSFET operation is discussed. Simple structure, low power consumption, small chip area, excellent operation in microwave frequencies and low temperature variation makes it suitable for on-chip microwave signal power detecting. Design of detector is performed in standard 0.18μm RF TSMC CMOS process. The design layout and post layout simulation results in K band (18-26.5 GHz) are presented.

Keywords: SDLVA, logarithmic amplifiers, video amplifier, microwave signals

1. Introduction

Many of modern electronic applications such as test and measurement equipment, military and space technologies and advanced physics labs need to the circuit, which is able to detect signals power at microwave frequencies with acceptable accuracy.

In special application, detectors are utilized in SDLVA. Fig. 1 shows block diagram of a SDLVA. In a concise description, this is a logarithmic convertor for compressing wide dynamic range RF signals. As seen, it consists of number of successive limiting amplifying stages that each drives a rectifier (or detector) cell. When the signal passes through the successive amplifying stages, the amplified signal level gradually will become too large and therefore it forces the transistors in saturation region and consequently, the amplified signal will be limited at a certain level.

Once signal amplitude grows sufficiently in one of the stages, it could be detected using a rectifier cell as a rippled DC current. All of the output currents are summed together at the output node called logging (or video) output. A simple RC low-pass filter removes the ripple of the summed rectified currents and converts them into the voltage, as shown in Figure 1.

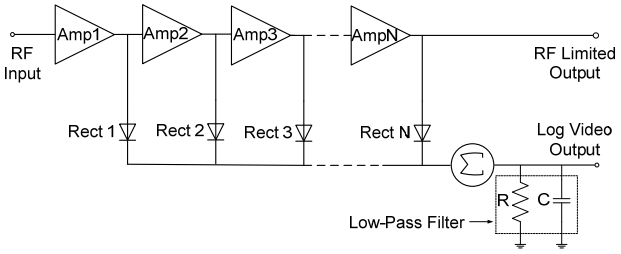

Figure 1. SDLVA functional block diagram

The logging output voltage then is a piecewise linear approximation of logarithmic response and is proportional to the power of RF input signal, as shown in Figure 2 [1].

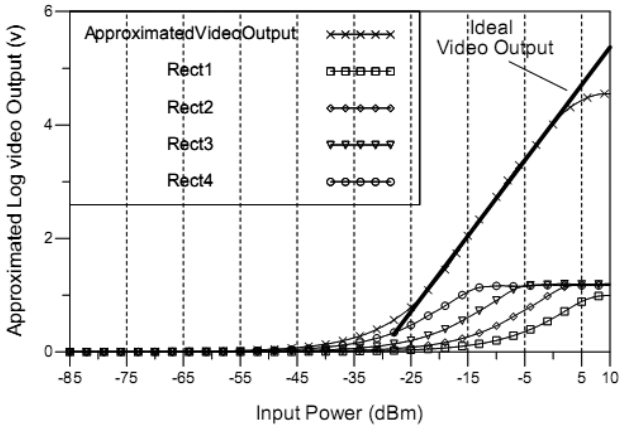

Figure 2. Piecewise linear approximation of video output by summing a rectifiers output in SDLVA

1* **Corresponding Author** : Department of Electrical Engineering, Science and Research branch, Islamic Azad University, Tehran, Iran, Email :m_dousti@srbiau.ac.ir

2 Department of Electrical Engineering, Science and Research branch, Islamic Azad University, Tehran, Iran.

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Traditional approaches to detect the power of signals, which have previously been reported in literature are Tunnel and Schottky diode [2-5] and unbalanced source-coupled pair as a full-wave rectifier [6-17]. The main drawback of the two first ones is that they require high power RF input signal due to their low sensitivity. Moreover, the standard CMOS process is not specified for the tunnel and Schottky contacts and therefore, adding them in any desired location on a CMOS-fabricated chip needs a post-CMOS process [18].

On the other hand, the design of full-wave rectifier is complicated and has high power consumption and large on-chip area compared to the proposed circuit.

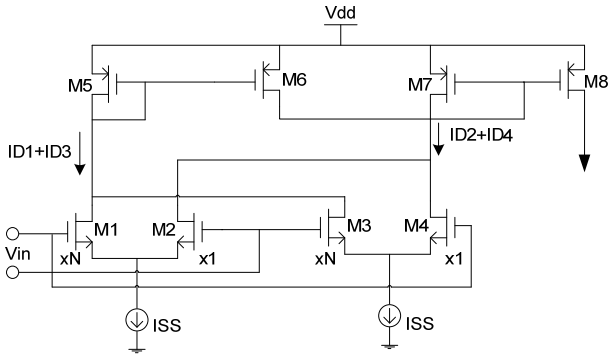


Figure 3. Full-wave rectifier circuit (a conventional method of rectifying in SDLVA)

Figure 3 shows the topology of full-wave rectifier using two unbalanced source-coupled pair. The operation of this circuit can be described by developing the study of the output current of a simple differential pair and then unbalancing the arms, either by a voltage offset or by unequal device sizes [8, 13].

In this paper, we introduce a novel method to detect a microwave signal power. The post layout simulation results along with the circuit's layout are presented.

The organization of this paper is as followed: section 2 discusses the principle of operation. The design analysis is presented in Section 3. Post-layout simulation results of the power detector are given in Section 4. Section 5 concludes the paper.

2. PRINCIPLE of OPERATION

The idea of using power detector instead of rectifier in SDLVA is a novel technique to generate the DC voltage proportional to microwave input power. In SDLVA, each rectifier cell produces a DC voltage from an AC sinusoidal output of its related amplifier. A power detector circuit can play the same role also, because it converts RF amplitude information into DC or low frequencies.

The number of useful researches to design a power detector circuit can be found in [19-28]. Most important specifications, which must be considered in a power detector circuit design, are simple robust architecture, minimum area, low power consumption and small input parasitic capacitance [29].

Here, we present a simple topology of a power detector suitable for microwave applications. Figure 4 shows the proposed power detector circuit configuration. As shown, a common drain topology with single MOSFET is used as a detector.

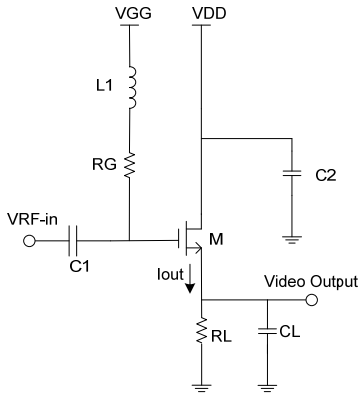


Figure 4. Proposed power detector circuit

The model of small signal silicon MOSFET used to analysis is as Figure 5. In this model, MOSFET is assumed unilateral, namely C_{gd} (the gate to drain capacitance) is neglected and the parasitic capacitances of bulk have been ignored to simplicity.

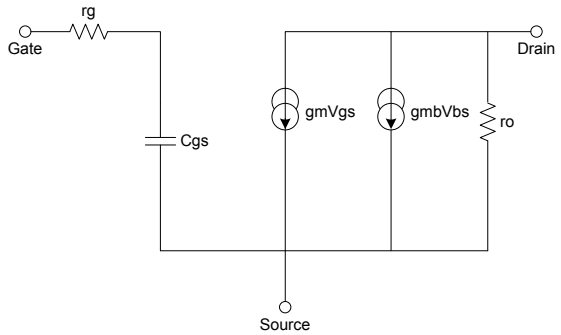


Figure 5. The simplified equivalent of the MOSFET transistor

Generally, the power detection process is performed in three stages: V/I (voltage to current) conversion, RF to DC conversion and finally I/V conversion [30-32].

In the proposed power detector, MOSFET converts voltage to current by the below relationship:

$$\Delta I_d = G_m \times \Delta V_g \quad (1)$$

Where ΔV_g equals to the detector voltage variation over the input dynamic range, ΔI_d is corresponding change in MOSFET current and G_m is the DC transconductance of MOSFET.

RF to DC conversion here stems from the non-linear properties of MOS transistor in saturation region. To achieve

higher sensitivity, it is better to keep the MOSFET in saturation region and close to the boundary of weak inversion. This helps the transistor to turn on immediately after receiving the positive cycle of microwave input.

Intuitively, during the positive cycle, AC current passes through the MOSFET. Accordingly, the parasitic capacitance at the gate of transistor (C_{gs}) is charged to the voltage higher than V_t (the threshold voltage of the MOSFET) and pushes it into the saturation region. The load resistor R_L then, converts current to the voltage. In addition, a load capacitor C_L eliminates the ripple of the output voltage (Figure 6(a)).

During the negative cycle, the current is extracted out of MOSFET, hence discharging the gate to source capacitance (C_{gs}) to the voltage lower than V_t and pushing it into the cut-off region (Figure 6(b)). This means, the MOSFET has just a current during a half of the input cycle and as a result, RF to DC conversion occurs.

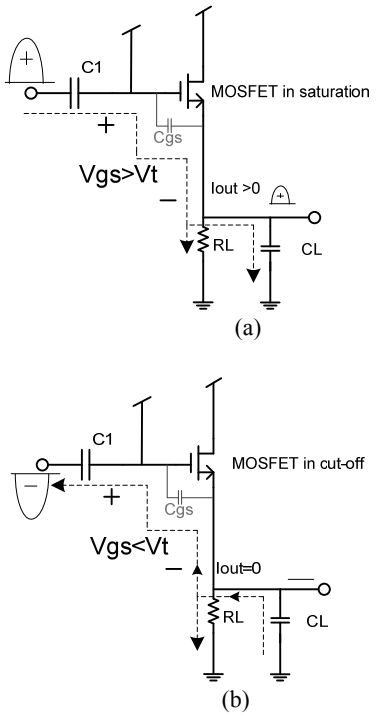


Figure 6. Proposed power detector functioning a) during the positive cycle and b) during the negative cycle

In continuation, the analysis of proposed circuit in saturation region of MOSFET operation will be presented and the RF to DC conversion will be proved and discussed.

3. Analysis OF Proposed Circuit

The drain current in a MOSFET by ignoring the channel length modulation parameter ($\lambda = 0$ or $r_o = \infty$) and considering $v_{BS} = 0$ (i.e., the body effect coefficient equal to zero) is as the following ideal relationship:

$$i_D = K(v_{GS} - V_t)^2 \tag{2}$$

In (2) v_{GS}, the instantaneous voltage of gate to source, is equal to $V_{GS} + v_{gs}$ where V_{GS} is the DC quiescent gate to source voltage and just affects on DC offset voltage of video output and v_{gs} ,the ac value of gate to source voltage, is equal to $v_i - v_o$ from proposed circuit schematic (Figure 4).

By considering the above equations and (2):

$$\begin{aligned} i_D &= K\left(V_{GS} + v_{gs} - V_t\right)^2 \\ &= K\left(V_{GS} - V_t\right)^2 + K\left[{v_{gs}}^2 + 2\left(V_{GS} - V_t\right)v_{gs}\right] \\ &= I_D + i_d \end{aligned} \tag{3}$$

Where:

$$I_D = K\left(V_{GS} - V_t\right)^2 \tag{4}$$

And,

$$i_d = K\left[{v_{gs}}^2 + 2\left(V_{GS} - V_t\right)v_{gs}\right] \tag{5}$$

From (3), the drain current of the detector is composed of the two parts that one (i.e. I_D), originates from biasing voltage by which an offset voltage in output is created and the other (i.e. i_d), results from microwave input power at the gate of the MOS transistor.

Substituting the $v_{gs} = v_i - v_o$ and $i_d = i_{out}$ into (5) gives:

$$i_{out} = K\left[\left(v_i - v_o\right)^2 + 2\left(V_{GS} - V_t\right)\left(v_i - v_o\right)\right] \tag{6}$$

At the last stage, current to voltage conversion is done using the load resistor (R_L) by the following equation:

$$v_o = R_L . i_{out} \tag{7}$$

A capacitor is paralleled to the load resistor to attenuate the ripples of video output of proposed circuit. The corresponding equation for the output voltage by replacing (6) into (7) is:

$$v_o = R_L K\left[\left(v_i - v_o\right)^2 + 2\left(v_i - v_o\right)\left(V_{GS} - V_t\right)\right] \tag{8}$$

Based on a small signal equivalent circuit of MOS transistor in Fig. 5, the voltage gain of a common drain derivates from a following equation [33]:

$$\frac{v_o}{v_i} = \frac{g_m R_L}{1 + g_m R_L} \times \left(\frac{1 - s/z_1}{1 - s/p_1}\right) \tag{9}$$

z_1 and p_1 are the Zero and Pole of the gain function respectively and are presented as below:

$$z_1 = -g_m \big/ C_{gs} \tag{10}$$

$$p_1 = -1 \big/ R_1 C_{gs} \tag{11}$$

With:

$$R_1 = \frac{r_g + R_L}{1 + g_m R_L} \tag{12}$$

Now by considering:

$$G = \frac{g_m R_L}{1 + g_m R_L} \times \left(\frac{1 - s/z_1}{1 - s/p_1} \right) \tag{13}$$

We have:

$$v_i - v_o = (1 - G) v_i \tag{14}$$

Substituting (14) in (8), the output voltage of the detector in saturation region is now determined in term of the input microwave signal as following:

$$v_o = R_L K \left[v_i^2 (1 - G)^2 + 2(V_{GS} - V_t)(1 - G) v_i \right] \tag{15}$$

It can be derived from above equation that if the second term is much smaller than the first, the v_o will be proportional to the power of input signal. In other word, the output voltage of power detector is approximately linear function of input power if:

$$v_i^2 (1 - G)^2 >> 2(V_{GS} - V_t)(1 - G) v_i \tag{16}$$

or

$$v_i >> 2(V_{GS} - V_t)/(1 - G) \tag{17}$$

This condition ensures that RF to DC conversion is achieved in a restricted range of microwave input power. Also, by approaching the gain to zero (i.e., $G \to 0$), the sensitivity closes to its limitation that is $2(V_{GS} - V_t)$. It is evidence that the lower overdrive voltage results in the lower detectable power signal and higher sensitivity.

4. POST LAYOUT SIMULATION RESULTS

Figure 7 is the layout of presented power detector. It has been designed in a standard 0.18µm RF TSMC CMOS technology with the active area of $0.075 \times 0.08\, mm^2$. The static power consumption of the power detector is about 1.3mW with a 1.8-V supply voltage.

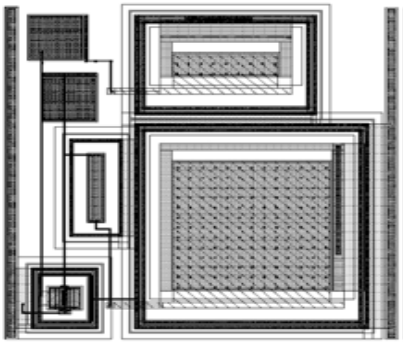
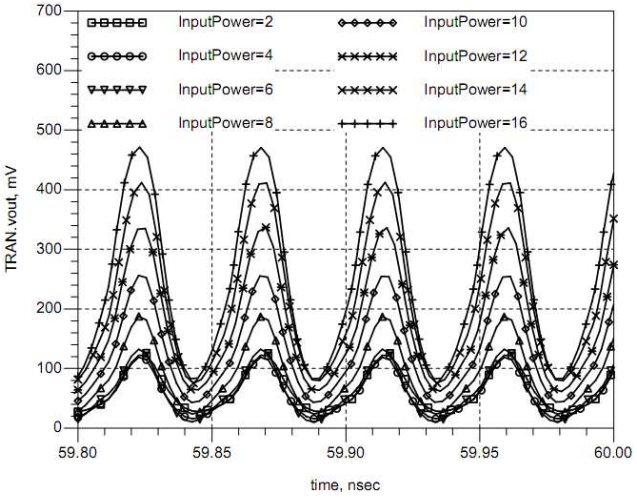
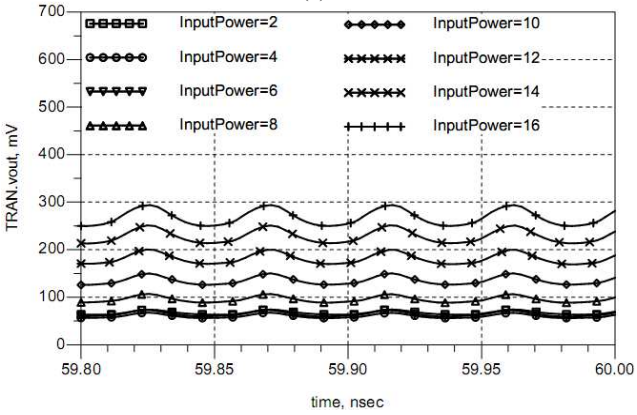


Figure 7. Layout of proposed power detector

Figure 8(a) depicts the transient response of the power detector. The RF to DC conversion is evidence from this figure. It clearly shows the DC voltage levels correspond to each input power. Figure 8(b) shows the same response for a larger load capacitor value (C_L). As shown, a larger C_L results in a lower ripple in DC output.



(a)



(b)

Figure 8. Transient response of proposed power detector for a) $C_L = 105fF$ and b) $C_L \approx 1pF$

Figure 9 shows the power detector response at two different frequencies at the edges of K band and the fitted line that indicates accurately the linear behavior of the detector in the dynamic range of 13 dB from -11 to 2dBm. This indicates that the detector's response varies with the input signal level proportionally and the two curve follow each other very closely. The slope of power detector response is $9.2\, {}^{mV}/_{dB}$.

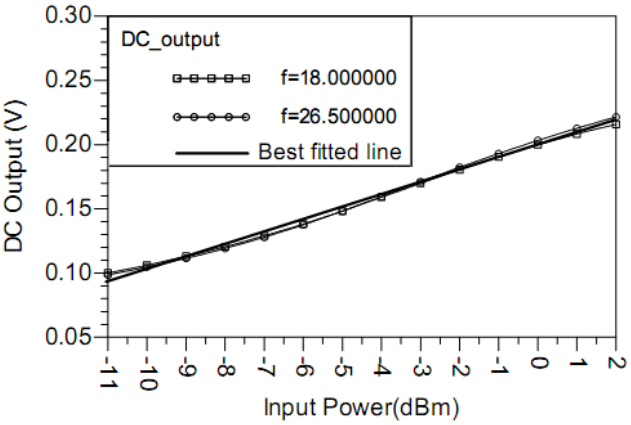
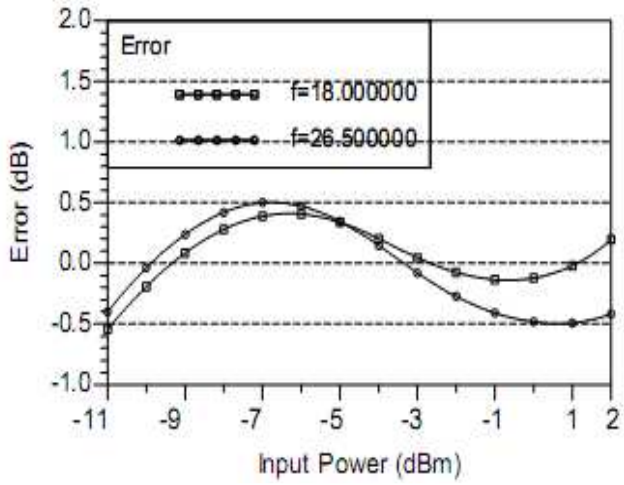
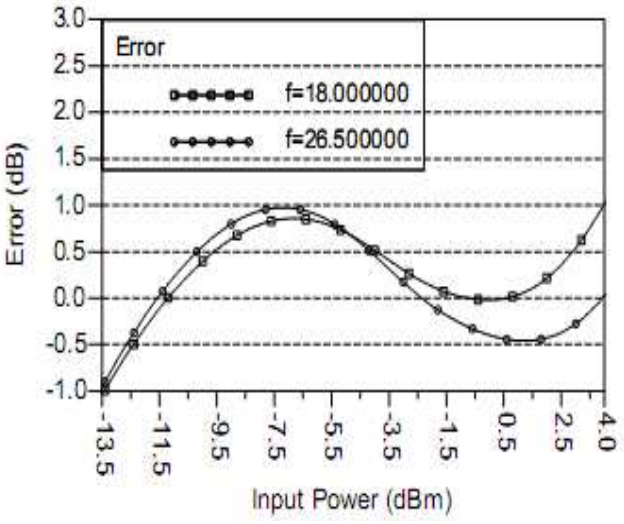


Figure 9. Power detector response over the dynamic range

Figure 10 illustrates the error of DC output as a function of input power over the dynamic range. This figure shows the error is less than ±0.5 dB from -11 to 2 dBm (Fig 10(a)) and ±1dB from -13.5 to 4 dBm (Fig 10(b)).



(a)



(b)

Figure 10. Error function of the designed power detector: a) over -11 to 2 dBm input power and b) over -13.5 to 4 dBm input power at 18GHz and 26.5GHz

The low variations of the proposed power detector over the entire operating temperature (-10 to 50 centigrade degree) can be seen from Fig. 11.

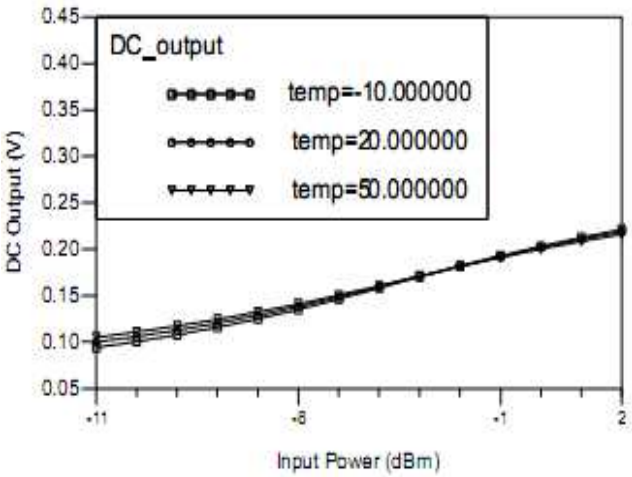


Figure 11. Response of the proposed power detector over the operating temperatures (-10°C, +20°C and +50°C)

Table 1 summarizes the post layout simulation results of this paper compared to the other previous work. As shown, the designed power detector has an enhanced chip area and very low power consumption compared to the other work referred in table1.

Table 1. Comparison of the post layout results of proposed power detector and previous works

Ref.	Technology	Frequency Range	Input Dynamic Range	Error	Power Consumption	Chip Area
[6]	0.18µm CMOS	From DC to 8GHz	40 dB	±1dB	Less than 70 mW	1.4×0.7 mm^2
[7]	0.18 µm CMOS	900 MHz to 1800 MHz	39 dB to 29 dB	±1dB	16 mW	1.02×0.47 mm^2
[19]	0.25 µm BiCMOSSiGe	Up to 6 GHz	45 dB	-	17 mW	-
[21]	0.13 µm CMOS	125 MHz to 8.5 GHz	20 dB to 18 dB	±0.5dB	0.18 mW	-
[23]	0.18 µm CMOS	3 to 10 GHz	40 dB	±3dB	Less than 8 mW	0.25 mm^2
This work	**0.18 µm CMOS**	**18 to 26.5 GHz**	**13 dB 17.5 dB**	**±0.5dB ±1dB**	**1.3 mW**	**0.075×0.08 mm^2**

5. CONCLUSION

An idea of utilizing a power detector instead of rectifier to detect the signal power of amplifiers in SDLVA is innovative. Moreover, the designed power detector itself is totally a new configuration. This novel cost-effective power detector occupies smaller chip size and consumes very low power, because it utilizes only one transistor compared to the previously method of full-wave rectifying which needs at least eight transistors. The sensitivity of the offered power detector might not seem so outstanding at first glance. However, it is sufficient for acceptable operation in SDLVA circuit because very low power signals are amplified successively and finally will be detected at the ending stages. Moreover, the sensitivity of this power detector is adjustable by choosing a proper overdrive voltage. The simplicity is most advantageous feature of this circuit. Dynamic range of the proposed circuit is about 17.5dBm with the ±1dB error and 13dBm with the ±0.5dB error. The total static power consumption is about 1.3mW and a total chip area is $0.075\times0.08\,mm^2$.

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